Silicon Storage Technology, Inc.

Flash Memory Data Book
July 1996

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Silicon Storage Technology, Inc.

Corporate Overview

Silicon Storage Technology, Inc. (SST) designs, manufacturers, and sells a variety of Electrically Erasable Programmable Read Only Memories (EEPROMs) manufactured with SST's proprietary SuperFlash EEPROM technology. These programmable nonvolatile memories retain data without power applied and are in-system alterable, using a single low current power supply.

SST's patented processes and designs allow the creation of high performance, high reliability, high density EEPROMs at competitive prices, when compared with alternate solutions. Founded in 1989, SST serves the manufacturers of personal computers, notebook computers, PC peripherals, PCMCIA cards, cellular telephones, and other commercial applications requiring low power and rugged reprogrammable nonvolatile memory.

SST has developed extensive partnerships with several major IC manufacturers. These partnerships provide SST with a guaranteed source of high quality, state-of-the-art wafers.

SST agreements with large users provide the information and demand for SST to maintain a leadership position in the cost and performance driven solid state storage market.

Design and product testing is performed at the company's headquarters in Sunnyvale, California and in Taiwan; wafer fabrication and package assembly are performed in Japan, Taiwan, and Korea.

SST's single power supply, i.e., 5.0V-only, 3.0V-only, or 2.7V-only, and small erase element EEPROMs provide the optimal solution for your reprogrammable nonvolatile memory applications.

SST is a publicly traded company. SST's stock is traded on Nasdaq under the symbol SSTI.

For additional information, please call your nearest authorized SST sales representative or distributor (see sections 33, 34, and 35 for listings), or contact SST directly at:

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Sunnyvale, CA 94086

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Important Information

Limited Warranty

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SST's products are not authorized fro use as critical component in life support devices or systems. Life support devices or systems are devices or systems that, (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

A critical component is any component of a life support device or system whose failure to perform can be expected to cause the failure of the life support device or system, or the affect its safety or effectiveness.

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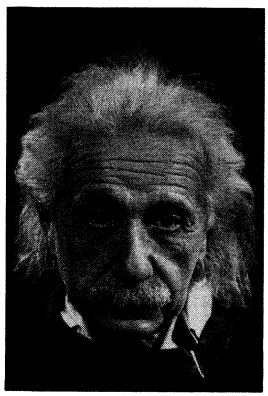
Patent Protection

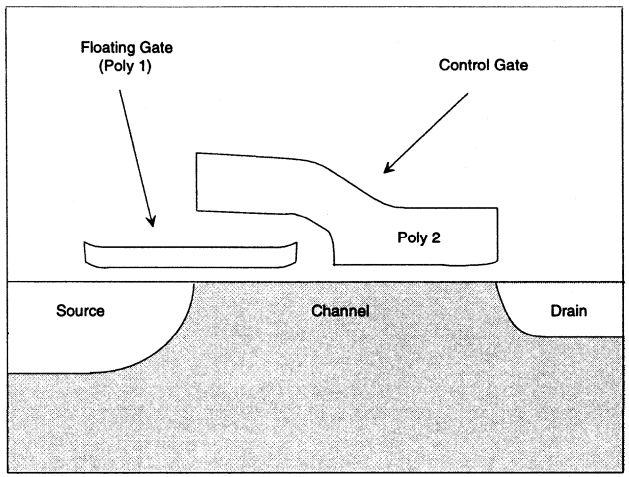
SST products are protected by assigned U.S. and foreign patents.



Everything should be made as simple as possible, but not simpler.

- Albert Einstein -

SST's E^2PROM cell



A 13 mask process, single power supply and small-sector erasable technology.

To learn more about
SST's SuperFlash Technology,
please see Sections 22-25.

SST products and technology are protected by the following U.S. patents, their foreign counterparts and other intellectual property rights.

U.S. Patent Number

5,029,130

5,045,488

5,067,108

5,181,187

5,191,232

5,202,850

5,226,006

5,242,848

5,278,087

5,289,411

5,359,570

5,369,609

5,373,467

5,386,158

5,432,748

5,475,634

5,479,609

5,500,826

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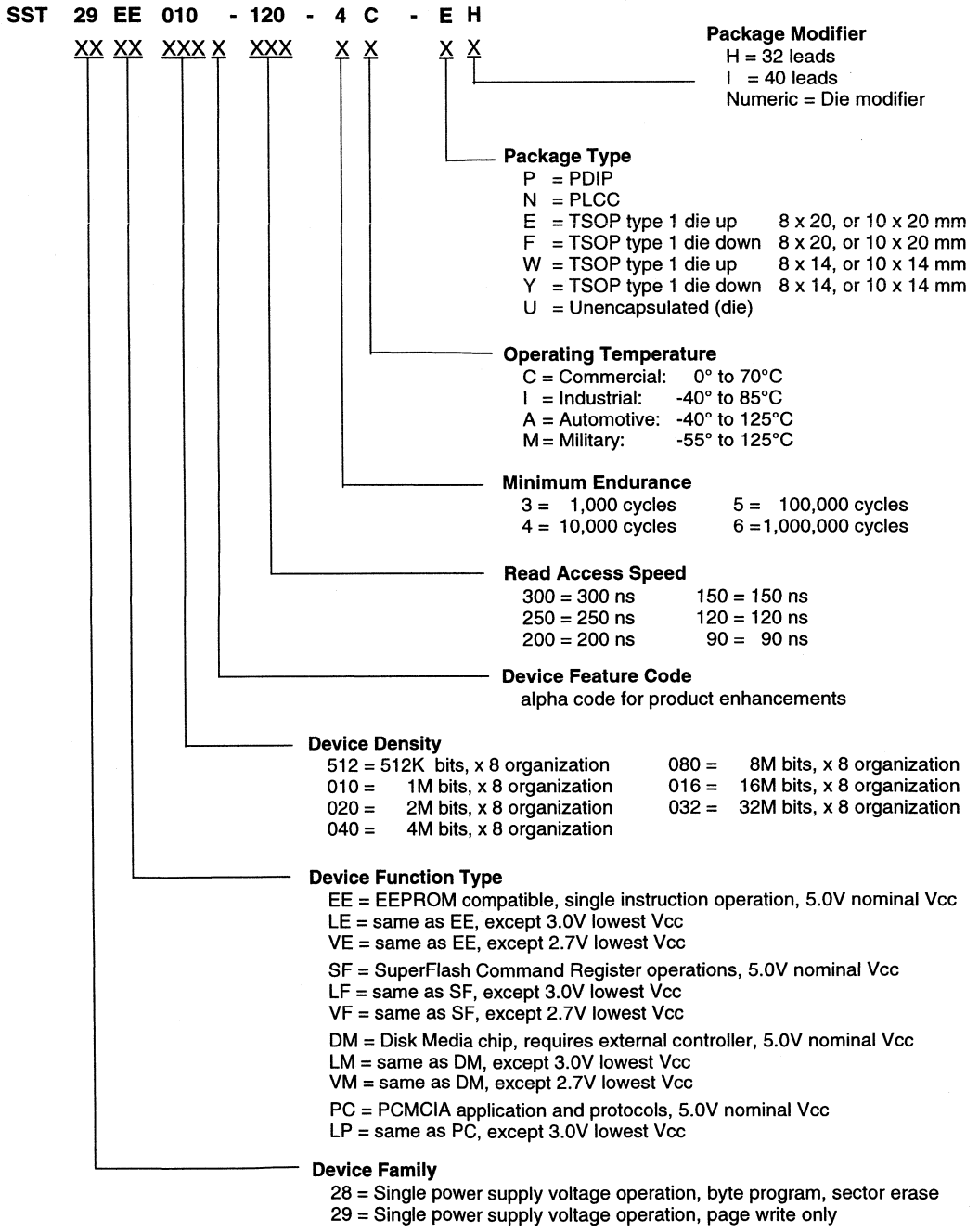


Data Sheet

SST 29EE512
5.0V-only 512 Kilobit
Page Mode EEPROM

July 1996

SST 29EE512
5.0V-only 512 Kilobit
Page Mode EEPROM

Features:

Single 5.0-Volt Read and Write Operations
CMOS SuperFlash EEPROM Technology
- Endurance: 100,000 Cycles (typical)
- Greater than 100 years Data Retention

Low Power Consumption:
- Active Current: 20 mA (typical)
- Standby Current: 10 µA (typical)

Fast Page-Write Operation
- 128 Bytes per Page, 512 Pages
- Page-Write Cycle: 5 ms (typical)
- Complete Memory Rewrite: 2.5 sec (typical)
- Effective Byte-write Cycle Time: 39 µs (typical)

Fast Access Time: 90 and 120 ns
Latched Address and Data
Automatic Write Timing with Internal V_{pp} Generation
End of Write Detection
- Toggle Bit
- Data# Polling

Hardware and Software Data Protection
TTL I/O Compatibility
JEDEC Standard Byte-wide EEPROM Pinouts
Packages Available
- 32-Pin TSOP
- 32-Lead PLCC
- 32 Pin Plastic DIP

Product Description

The 29EE512 is a 64K x 8 CMOS page mode EEPROM manufactured with SST's proprietary, high performance CMOS SuperFlash technology. The split gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The 29EE512 writes with a 5.0-volt-only power supply. Internal erase/program is transparent to the user. The 29EE512 conforms to JEDEC standard pinouts for byte-wide memories.

Featuring high performance page write, the 29EE512 provides a typical byte-write time of 39 µsec. The entire memory, i.e., 64K bytes, can be written page by page in as little as 2.5 seconds, when using interface features such as Toggle Bit or Data# Polling to indicate the completion of a write cycle. To protect against inadvertent write, the 29EE512 has on-chip hardware and software data protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, the 29EE512 is offered with a guaranteed page-write endurance of 10^4 or 10^3 cycles. Data retention is rated at greater than 100 years.

The 29EE512 is suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, the 29EE512 significantly improves performance and reliability, while lowering power consumption, when compared with floppy disk or EPROM approaches. The 29EE512 improves flexibility while lowering the cost for program, data, and configuration storage applications.

To meet high density, surface mount requirements, the 29EE512 is offered in 32-pin TSOP and 32-lead PLCC packages. A 600-mil, 32-pin PDIP package is also available. See Figures 2A and 2B for pinouts.

Device Operation

The SST page mode EEPROM offers in-circuit electrical write capability. The 29EE512 does not require separate erase and program operations. The internally timed write cycle executes both erase and program transparently to the user. The 29EE512 has industry standard optional Software Data Protection, which SST recommends always to be enabled. The 29EE512 is compatible with industry standard EEPROM pinouts and functionality.

Read

The read operation of the 29EE512 is controlled by CE# and OE#, both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the read cycle timing diagram for further details (Figure 3).

Write

The write operation consists of three steps. The first step is the optional three byte load sequence for Software Data Protection. This is an optional first step in the write operation, but highly recommended to ensure proper data integrity. Step 2 is the byte-load cycle to a page buffer of the 29EE512. Step 3 is an internally controlled write cycle for writing the data loaded in the page buffer into the memory array for nonvolatile storage. During the byte-load cycle, the addresses are latched by the falling edge of either CE# or WE#, whichever occurs last. The data is latched by the rising edge of either CE# or WE#, whichever occurs first. The internal write cycle is initiated by a timer after the rising edge of WE# or CE#, whichever occurs first. The write cycle, once initiated, will continue to completion, typically within 5 ms. See Figures 4 and 5 for WE# and CE# controlled page write cycle timing diagrams and Figures 15 and 17 for flowcharts.

The write operation has three functional cycles: the optional Software Data Protection load sequence, the page load cycle and the internal write cycle. The Software Data Protection consists of a specific three byte load sequence that will leave the 29EE512 protected at the end of the page write. The page load cycle consists of loading 1 to 128 bytes of data into the page buffer. The internal write cycle consists of the T_{BLCO} time-out and the write timer operation. During the write operation, the only valid reads are Data# Polling and Toggle Bit.

The page-write operation allows the loading of up to 128 bytes of data into the page buffer of the 29EE512 before the initiation of the internal write cycle. During the internal write cycle, all the data in the page buffer is written simultaneously into the memory array. Hence, the page-write feature of 29EE512 allows the entire memory to be written in as little as 2.5 seconds. During the internal write cycle, the host is free to perform additional tasks, such as to fetch data from other locations in the system to set up the write to the next page. In each page-write operation, all the bytes that are loaded into the page buffer must have the same page address, i.e., A_7 through A_{15}. Any byte not loaded with user data will be written to FF.

See Figures 4, 5, and 8 for the page-write cycle timing diagrams. If after the initial byte-load cycle, the host loads a second byte into the page buffer within a byte-load cycle time (T_{BLC}) of 100 µs, the 29EE512 will stay in the page load cycle. Additional bytes are then loaded consecutively. The page load cycle will be terminated if no additional byte is loaded into the page buffer within 200 µs (T_{BLCO}) from the last byte-load cycle, i.e., no subsequent WE# or CE# high-to-low transition after the last rising edge of WE# or CE#. Data in the page buffer can be changed by a subsequent byte-load cycle. The page load period can continue indefinitely, as long as the host continues to load the device within the byte-load cycle time of 100 µs. The page to be loaded is determined by the page address of the last byte loaded.

Software Chip-Erase

The 29EE512 provides a chip-erase operation, which allows the user to simultaneously clear the entire memory array to the "1" state. This is useful when the entire device must be quickly erased.

The Software Chip-Erase operation is initiated by using a specific six byte-load sequence. After the load sequence, the device enters into an internally timed cycle similar to the write cycle. During the erase operation, the only valid read is Toggle Bit. See Table 4 for the load sequence, Figure 10 for timing diagram, and Figure 19 for the flowchart.

Write Operation Status Detection

The 29EE512 provides two software means to detect the completion of a write cycle, in order to optimize the system write cycle time. The software detection includes two status bits: Data# Polling (DQ_7) and Toggle Bit (DQ_6). The end of write detection mode is enabled after the rising WE# or CE# whichever occurs first, which initiates the internal write cycle.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If

both reads are valid, then the device has completed the write cycle, otherwise the rejection is valid.

Data# Polling (DQ_7)

When the 29EE512 is in the internal write cycle, any attempt to read DQ_7 of the last byte loaded during the byte-load cycle will receive the complement of the true data. Once the write cycle is completed, DQ_7 will show true data. The device is then ready for the next operation. See Figure 6 for Data# Polling timing diagram and Figure 16 for a flowchart.

Toggle Bit (DQ_6)

During the internal write cycle, any consecutive attempts to read DQ_6 will produce alternating 0's and 1's, i.e., toggling between 0 and 1. When the write cycle is completed, the toggling will stop. The device is then ready for the next operation. See Figure 7 for Toggle Bit timing diagram and Figure 16 for a flowchart. The initial read of the Toggle Bit will be a "1".

Data Protection

The 29EE512 provides both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a write cycle.

V_{CC} Power Up/Down Detection: The write operation is inhibited when V_{CC} is less than 2.5V.

Write Inhibit Mode: Forcing OE# low, CE# high, or WE# high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down.

Software Data Protection (SDP)

The 29EE512 provides the JEDEC approved optional software data protection scheme for all data alteration operations, i.e., write and chip erase. With this scheme, any write operation requires the inclusion of a series of three byte-load operations to precede the data loading operation. The three byte-load sequence is used to initiate the write cycle, providing optimal protection from inadvertent write operations, e.g., during the system power-up or power-down. The 29EE512 is shipped with the software data protection disabled.

The software protection scheme can be enabled by applying a three-byte sequence to the device, during a page-load cycle (Figure 8). The device will then be automatically set into the data protect mode. Any subsequent write operation will require the preceding three-byte sequence. See Table 4 for the specific software command codes and Figure 8 for the timing diagram. To set the device into the unprotected mode, a six-byte sequence is required. See Table 4 for the specific codes and Figure 9 for the timing diagram. If a write is attempted while SDP is enabled the device will be in a non-accessible state for ~ 300 µs. SST recommends Software Data Protection always be enabled. See Figure 17 for flowcharts.

The 29EE512 Software Data Protection is a global command, protecting (or unprotecting) all pages in the entire memory array once enabled (or disabled). Therefore using SDP for a single page write will enable SDP for the entire array. Single pages by themselves cannot be SDP enabled or disabled.

Single power supply reprogrammable nonvolatile memories may be unintentionally altered. SST strongly recommends that Software Data Protection (SDP) always be enabled. The 29EE512 should be programmed using the SDP command sequence. SST recommends the SDP Disable Command Sequence not be issued to the device prior to writing.

Product Identification

The product identification mode identifies the device as the 29EE512 and manufacturer as SST. This mode may be accessed by hardware or software operations. The hardware operation is typically used by a programmer to identify the correct algorithm for the SST 29EE512. Users may wish to use the software product identification operation to identify the part (i.e., using the device code) when using multiple manufacturers in the same socket. For details, see Table 3 for hardware operation or Table 4 for software operation, Figure 11 for the software ID entry and read timing diagram and Figure 18 for the ID entry command sequence flowchart. The manufacturer and device codes are the same for both operations.

Table 1: Product Identification Table

	Byte	Data
Manufacturers Code	0000 H	BF H
Device Code	0001 H	5D H

Product Identification Mode Exit

In order to return to the standard read mode, the Software Product Identification mode must be exited. Exiting is accomplished by issuing the Software ID Exit (reset) operation, which returns the device to the read operation. The reset operation may also be used to reset the device to the read mode after an inadvertent transient condition that apparently causes the device to behave abnormally, e.g., not read correctly. See Table 4 for software command codes, Figure 12 for timing waveform and Figure 18 for a flowchart.

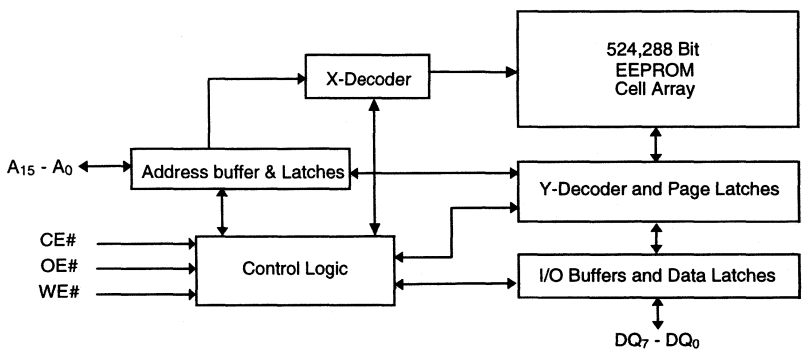


Figure 1: Functional Block Diagram of SST 29EE512

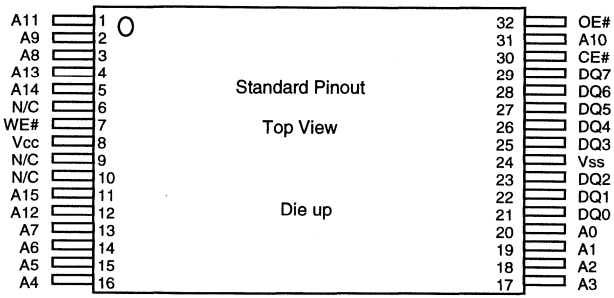


Figure 2A: Pin Assignments for 32-pin TSOP Packages

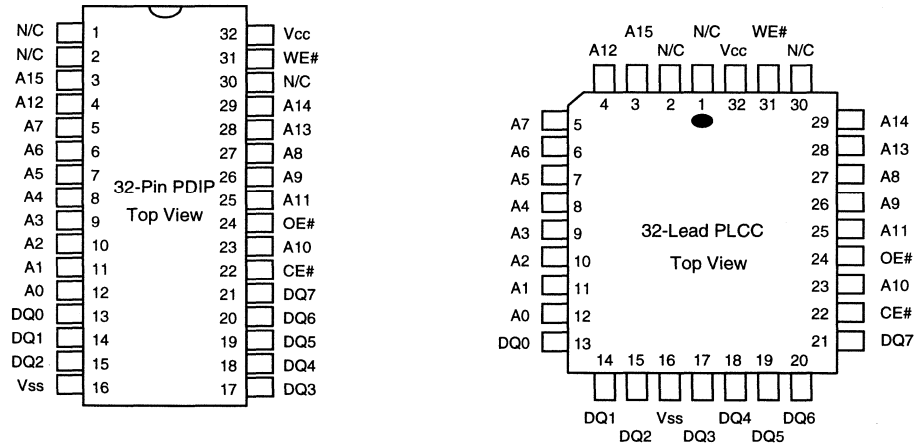


Figure 2B: Pin Assignments for 32-pin Plastic DIPs and 32-lead PLCCs

Table 2: Pin Description

Symbol	Pin Name	Functions
A_{15}-A_7	Row Address Inputs	To provide memory addresses. Row addresses define a page for a write cycle.
A_6-A_0	Column Address Inputs	Column Addresses are toggled to load page data.
DQ_7-DQ_0	Data Input/output	To output data during read cycles and receive input data during write cycles. Data is internally latched during a write cycle. The outputs are in tri-state when OE# or CE# is high.
CE#	Chip Enable	To activate the device when CE# is low.
OE#	Output Enable	To gate the data output buffers.
WE#	Write Enable	To control the write operations
Vcc	Power Supply	To provide 5-volt supply (± 10%)
Vss	Ground	
NC	No Connection	Unconnected pins.

Table 3: Operation Modes Selection

Mode	CE#	OE#	WE#	DQ	Address
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	A_{IN}
Page Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}
Standby	V_{IH}	X	X	High Z	X
Write Inhibit	X	V_{IL}	X	High Z/ D_{OUT}	X
Write Inhibit	X	X	V_{IH}	High Z/ D_{OUT}	X
Software Chip Erase	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}, See Table 4
Product Identification					
Hardware Mode	V_{IL}	V_{IL}	V_{IH}	Manufacturer Code (BF)	A_{15} - A_1 = V_{IL}, A_9 = V_H, A_0 = V_{IL}
				Device Code (5D)	A_{15} - A_1 = V_{IL}, A_9 = V_H, A_0= V_{IH}
Software Mode	V_{IL}	V_{IH}	V_{IL}		See Table 4
SDP Enable Mode	V_{IL}	V_{IH}	V_{IL}		See Table 4
SDP Disable Mode	V_{IL}	V_{IH}	V_{IL}		See Table 4

Table 4: Software Command Codes

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data
Software Data Protect Enable & Page Write	5555H	AAH	2AAAH	55H	5555H	A0H	Addr[2]	Data				
Software Data Protect Disable	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	20H
Software Chip Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry	5555H	AAH	2AAAH	55H	5555H	90H						
Software ID Exit	5555H	AAH	2AAAH	55H	5555H	F0H						
Alternate Software ID Entry[3]	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	60H

Notes: (1) Address format A_{14}-A_0 (Hex), Address A_{15} is a "Don't Care".

(2) Page Write consists of loading up to 128 bytes (A_6 - A_0).

(3) Alternate 6 byte Software Product ID Command Code

Notes for Software Product ID Command Code:

1. With A_{14} -A_1 =0; SST Manufacturer Code = BFH, is read with A_0 = 0,
   29EE512 Device Code = 5DH, is read with A_0 = 1.
2. The device does not remain in Software Product ID Mode if powered down.
3. This product supports both the JEDEC standard 3 byte command code sequence and SST's original 6 byte command code sequence. For new designs, SST recommends that the 3 byte command code sequence be used.

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential ..... -0.5V to V_{CC}+ 0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential ..... -1.0V to V_{CC}+ 1.0V
Voltage on A_9 Pin to Ground Potential ..... -0.5V to 14.0V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Through Hole Lead Soldering Temperature (10 Seconds) ..... 300°C
Surface Mount Lead Soldering Temperature (3 Seconds) ..... 240°C
Output Short Circuit Current[1] ..... 100 mA

Note: [1] Outputs shorted for no more than one second. No more than one output shorted at a time.

Operating Range

Range	Ambient Temp	V_{CC}
Commercial	0 °C to +70 °C	5V±10%
Industrial	-40 °C to +85 °C	5V±10%

AC Conditions of Test

Input Rise/Fall Time.....10 ns
Output Load.....1 TTL Gate and C_L = 100 pF
See Figures 13 and 14

Table 5: DC Operating Characteristics

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{CC}	Power Supply Current				CE#=OE#=V_{IL},WE#=V_{IH}, all I/Os open,
	Read		30	mA	Address input = V_{IL}/V_{IH}, at f=1/T_{RC} Min., V_{CC}=V_{CC} Max
	Write		50	mA	CE#=WE#=V_{IL}, OE#=V_{IH}, V_{CC}=V_{CC} Max.
I_{SB1}	Standby V_{CC} Current (TTL input)		3	mA	CE#=OE#=WE#=V_{IH}, V_{CC}=V_{CC} Max.
I_{SB2}	Standby V_{CC} Current (CMOS input)		50	µA	CE#=OE#=WE#=V_{CC} -0.3V. V_{CC} = V_{CC} Max.
I_{LI}	Input Leakage Current		1	µA	V_{IN} =GND to V_{CC}, V_{CC} = V_{CC} Max.
I_{LO}	Output Leakage Current		10	µA	V_{OUT} =GND to V_{CC}, V_{CC} = V_{CC} Max.
V_{IL}	Input Low Voltage		0.8	V	V_{CC} = V_{CC} Max.
V_{IH}	Input High Voltage	2.0		V	V_{CC} = V_{CC} Max.
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.1 mA, V_{CC} = V_{CC} Min.
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400µA, V_{CC} = V_{CC} Min.
V_H	Supervoltage for A_9	11.6	12.4	V	CE# = OE# =V_{IL}, WE# = V_{IH}
I_H	Supervoltage Current for A_9		200	µA	CE# = OE# = V_{IL}, WE# = V_{IH}, A_9 = V_H Max.

Table 6: Power-up Timings

Symbol	Parameter	Maximum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$[1]	Power-up to Write Operation	5	ms

Table 7: Capacitance (Ta = 25 °C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0v	6 pF

Note: [1]This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 8: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}	Endurance	1,000 & 10,000[2]	Cycles	MIL-STD-883, Method 1033
T_{DR}[1]	Data Retention	100	Years	MIL-STD-883, Method 1008
V_{ZAP_HBM}[1]	ESD Susceptibility Human Body Model	1000	Volts	JEDEC Standard A114
V_{ZAP_MM}[1]	ESD Susceptibility Machine Model	200	Volts	JEDEC
I_{LTH}[1]	Latch Up	100	mA	JEDEC Standard 17

Note: [1]This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

[2]See Ordering Information for desired type.

AC Characteristics

Table 9: Read Cycle Timing Parameters

Symbol	Parameter	29EE512-90		29EE512-120		Units
		Min	Max	Min	Max	
T_{RC}	Read Cycle Time	90		120		ns
T_{CE}	Chip Enable Access Time		90		120	ns
T_{AA}	Address Access Time		90		120	ns
T_{OE}	Output Enable Access Time		40		50	ns
T_{CLZ}[1]	CE# Low to Active Output	0		0		ns
T_{OLZ}[1]	OE# Low to Active Output	0		0		ns
T_{CHZ}[1]	CE# High to High-Z Output		30		30	ns
T_{OHZ}[1]	OE# High to High-Z Output		30		30	ns
T_{OH}[1]	Output Hold from Address Change	0		0		ns

Table 10: Page-Write Cycle Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{WC}	Write Cycle (erase and program)		10	ms
T_{AS}	Address Setup Time	0		ns
T_{AH}	Address Hold Time	50		ns
T_{CS}	WE# and CE# Setup Time	0		ns
T_{CH}	WE# and CE# Hold Time	0		ns
T_{OES}	OE# High Setup Time	0		ns
T_{OEH}	OE# High Hold Time	0		ns
T_{CP}	CE# Pulse Width	70		ns
T_{WP}	WE# Pulse Width	70		ns
T_{DS}	Data Setup Time	35		ns
T_{DH}	Data Hold Time	0		ns
T_{BLC}[1]	Byte Load Cycle Time	0.05	100	µs
T_{BLCO}[1]	Byte Load Cycle Time	200		µs
T_{IDA}	Software ID Access and Exit Time		10	µs
T_{SCE}	Software Chip Erase		20	ms

Note: [1]This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.

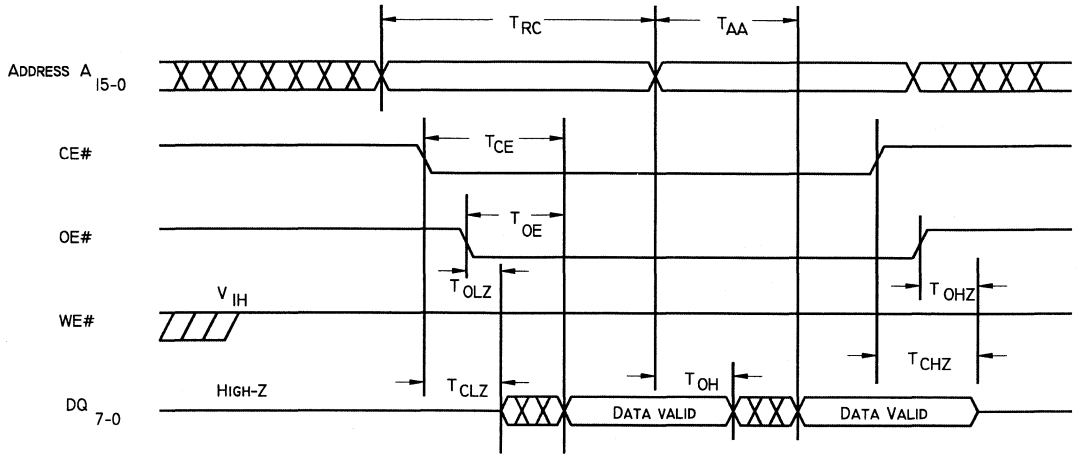


Figure 3: Read Cycle Timing Diagram

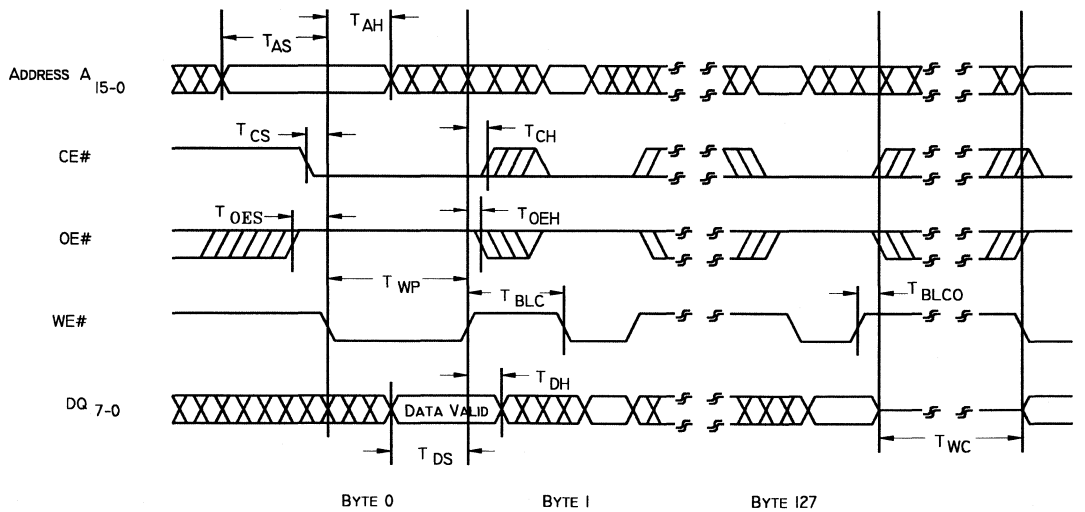


Figure 4: WE# Controlled Page Write Cycle Timing Diagram

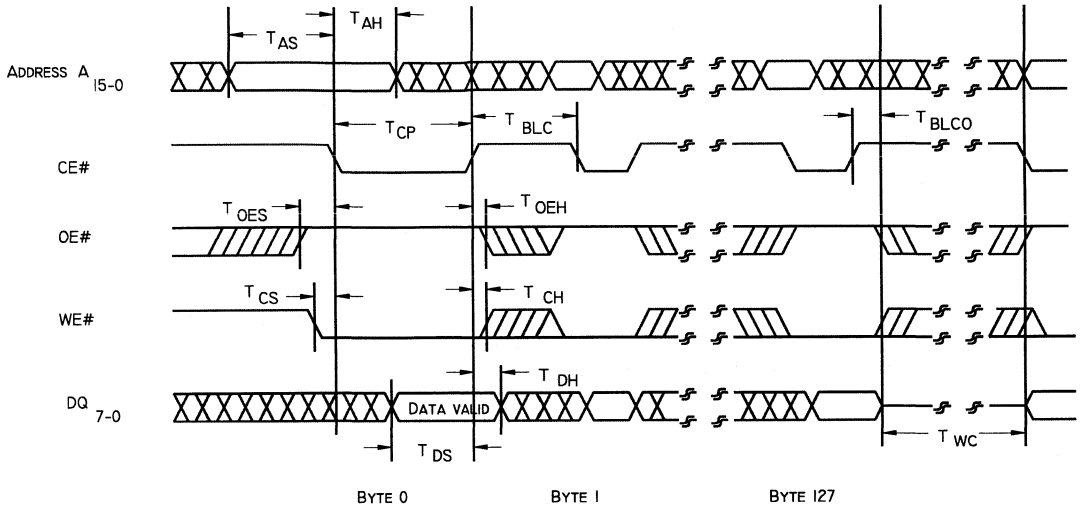


Figure 5: CE# Controlled Page Write Cycle Timing Diagram

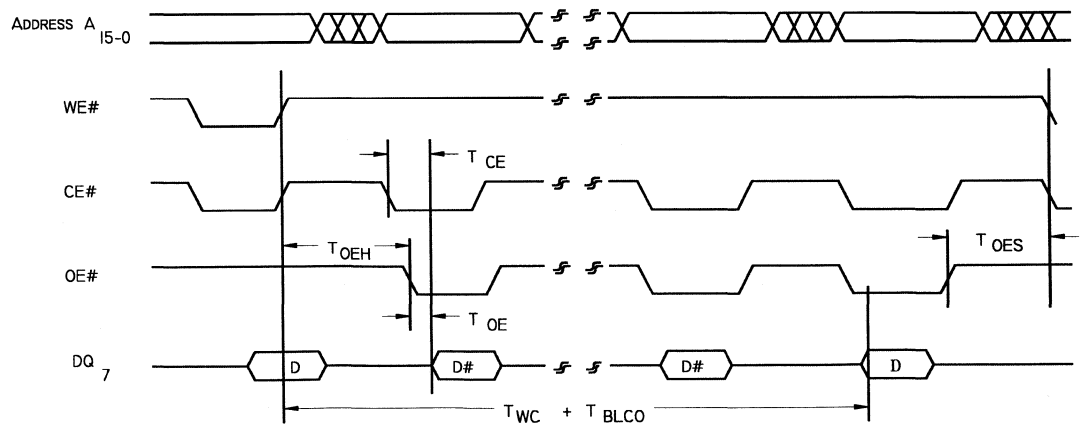


Figure 6: Data# Polling Timing Diagram

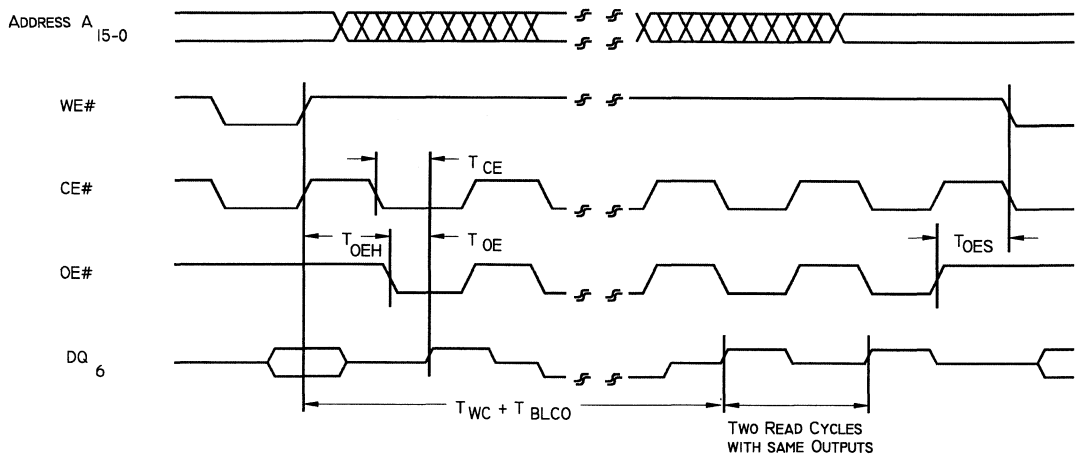
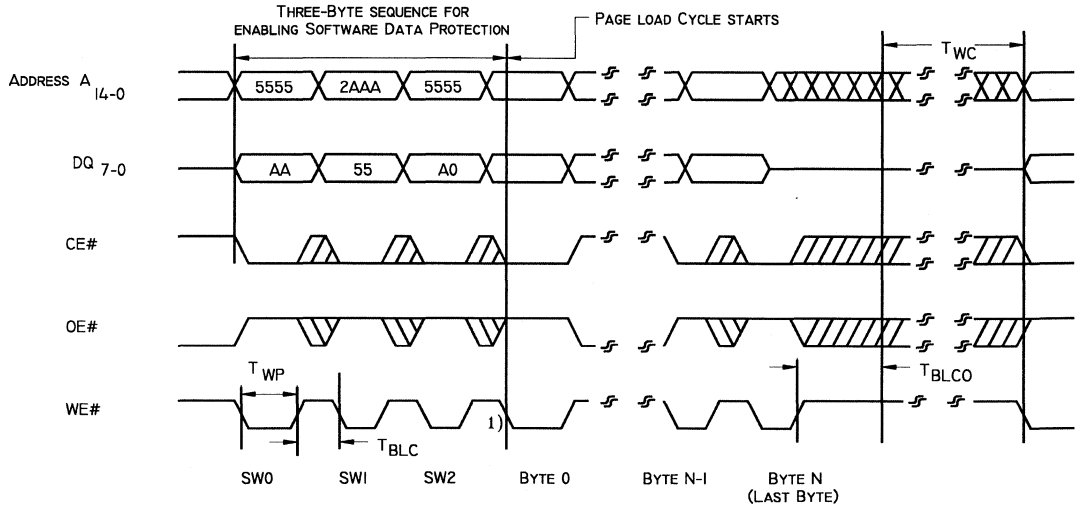


Figure 7: Toggle Bit Timing Diagram



NOTE 1): THE TIME BETWEEN ENABLING SOFTWARE DATA PROTECT AND THE PAGE LOAD MUST BE LESS THAN T_{BLCO}

Figure 8: Software Data Protection Page Write Timing Diagram

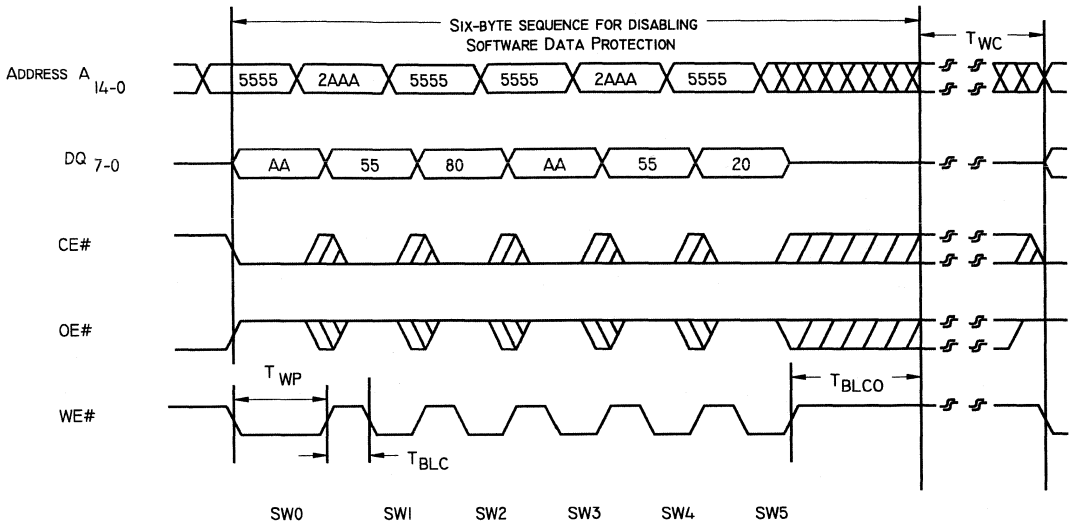


Figure 9: Software Data Protect Disable Timing Diagram

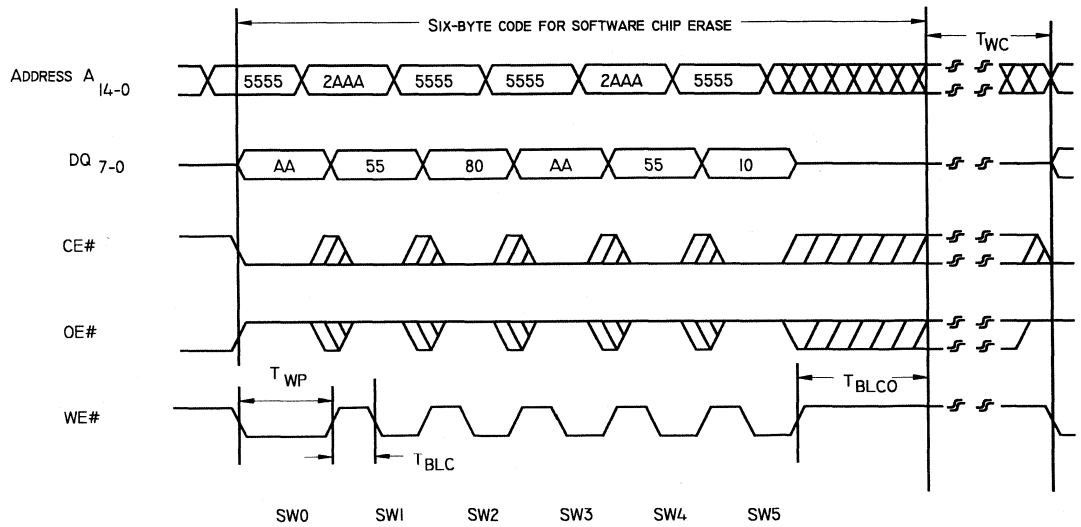


Figure 10: Software Chip Erase Timing Diagram

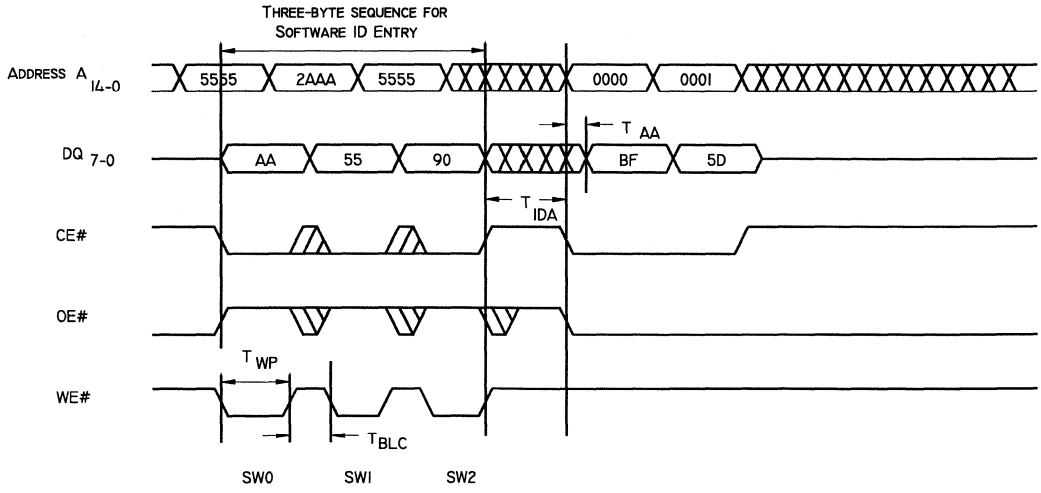


Figure 11: Software ID Entry and Read

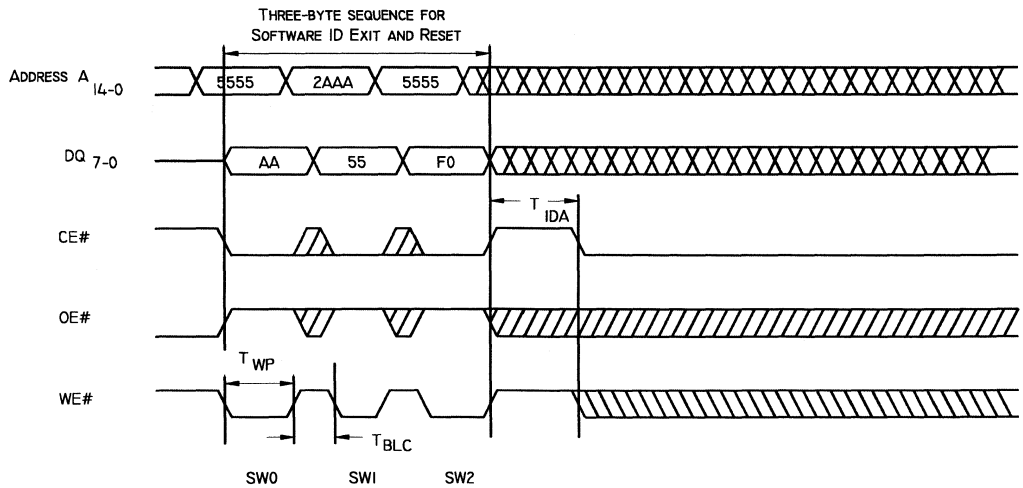
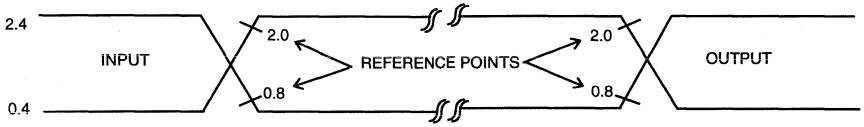


Figure 12: Software ID Exit and Reset



AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a logic "1" and V_{OL} (0.4 V_{TTL}) for a logic "0". Measurement reference points for inputs and outputs are V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Inputs rise and fall times (10% ↔ 90%) are <10 ns.

Figure 13: AC Input/Output Reference Waveforms

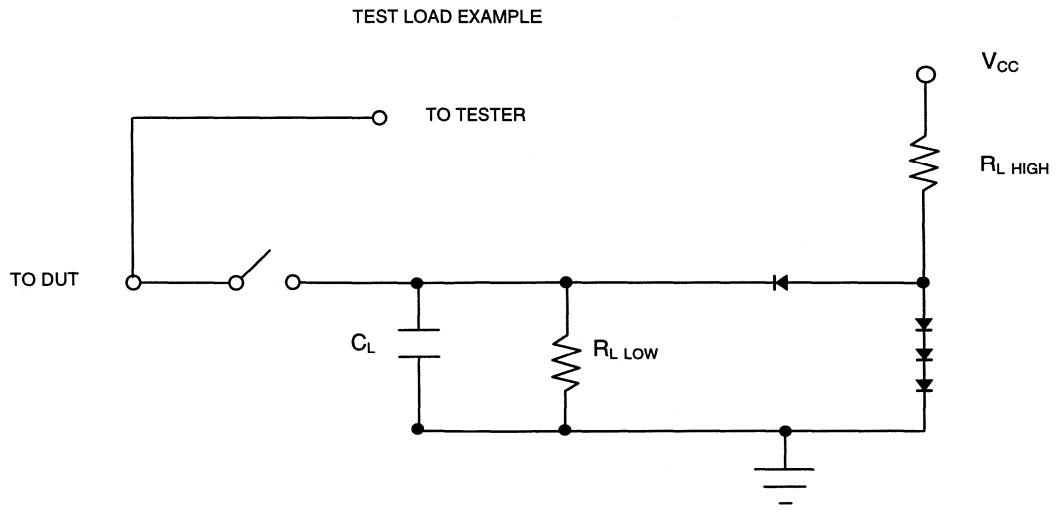


Figure 14: Test Load Example

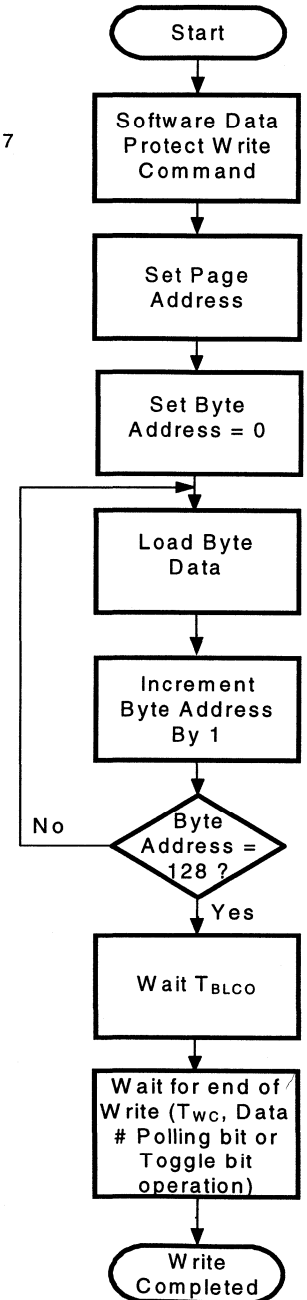


Figure 15: Write Algorithm

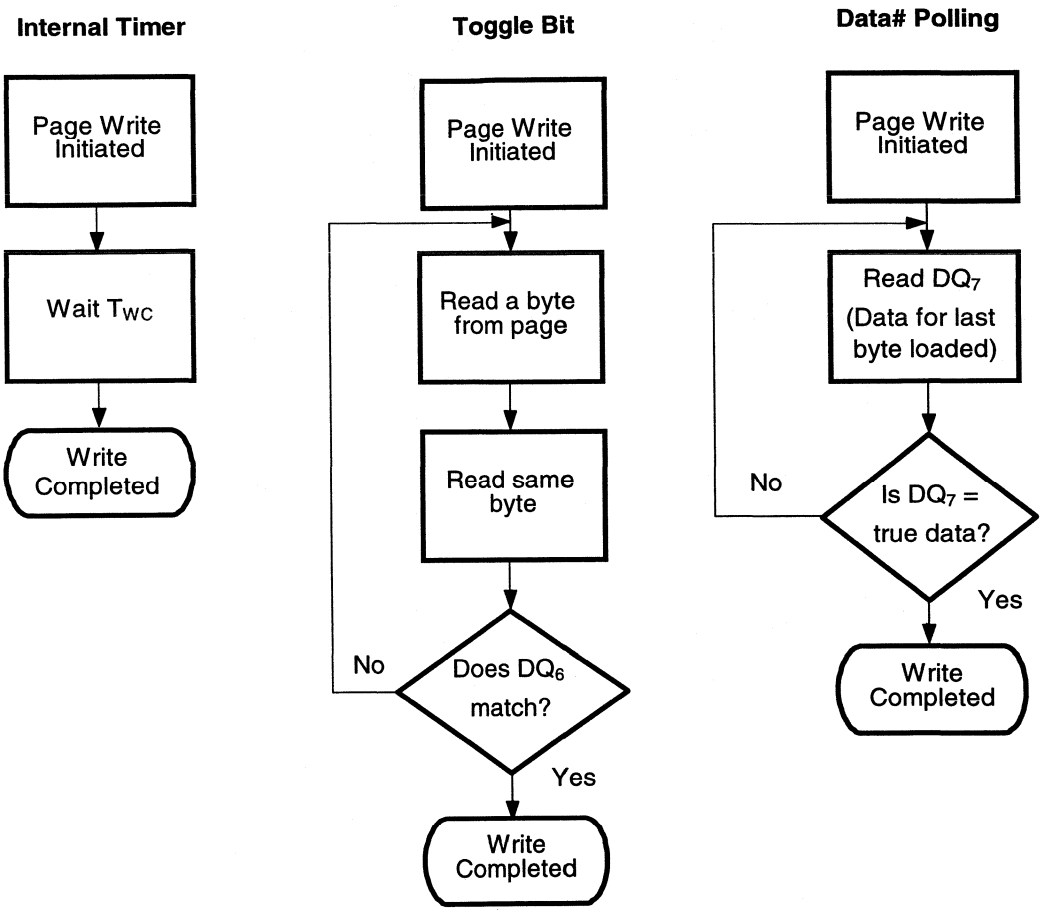


Figure 16: Wait Options

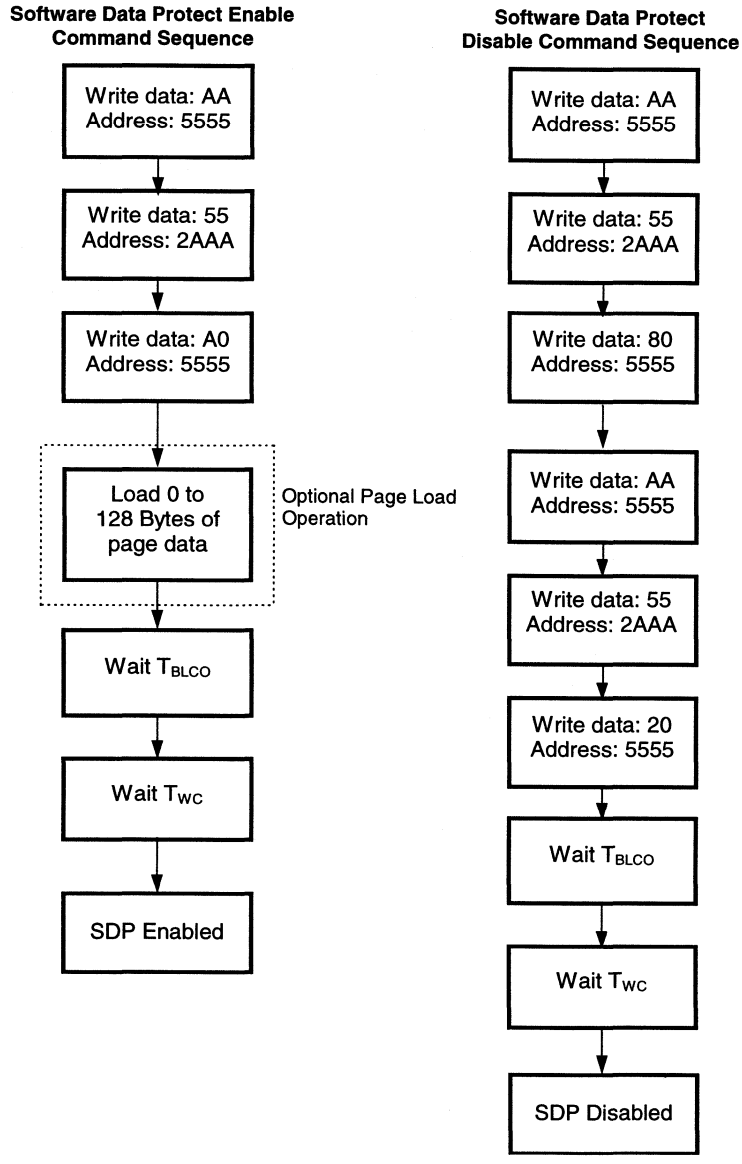


Figure 17: Software Data Protection Flowcharts

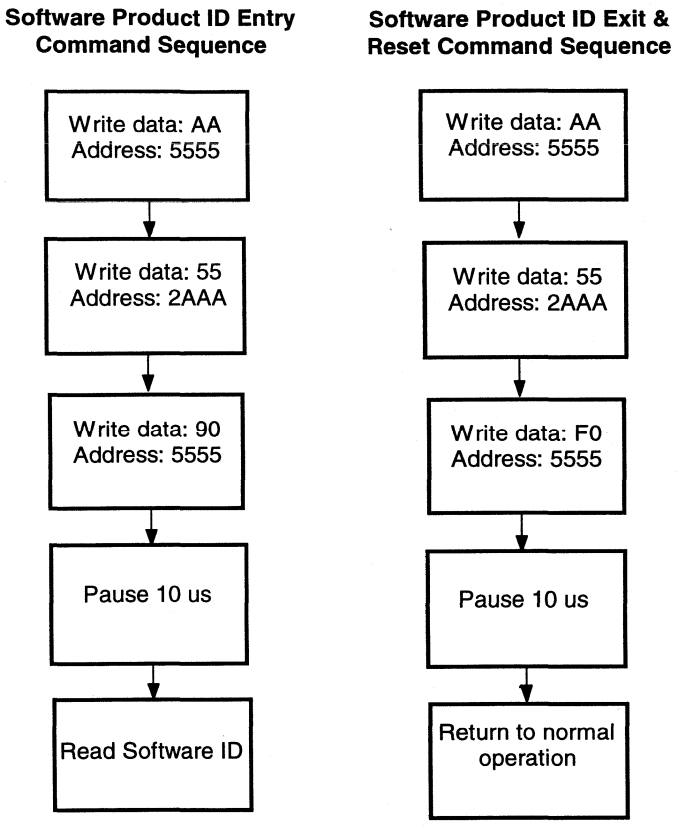


Figure 18: Software Product Command Flowcharts

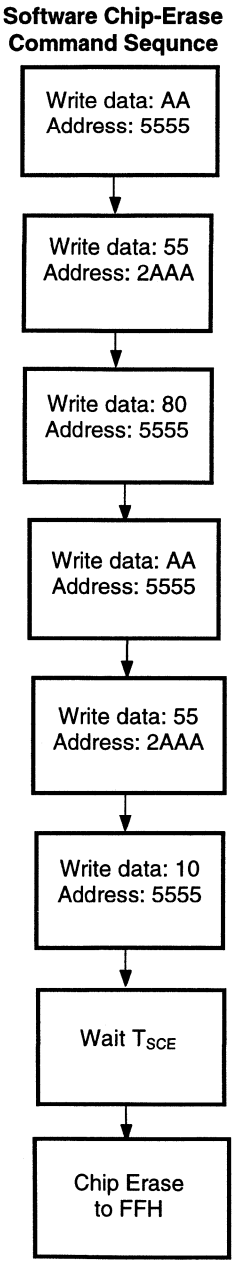


Figure 19: Software Chip Erase Command Codes

Product Ordering Information

Device		Speed		Suffix1		Suffix2
SST29EE512	-	XXX	-	XX	-	XX

Package Modifier
H = 32 leads
Numeric = Die modifier

Package Type
P = PDIP
N = PLCC
E = TSOP (die up)
U = Unencapsulated die

Operating Temperature
C = Commercial = 0° to 70°C
I = Industrial = -40° to 85°C

Minimum Endurance
3 = 1000 cycles
4 = 10,000 cycles

Read Access Speed
120 = 120 ns
90 = 90 ns

Valid combinations

SST29EE512- 90-4C- EH	SST29EE512- 90-4C- NH	SST29EE512- 90-4C- PH
SST29EE512-120-4C- EH	SST29EE512-120-4C- NH	SST29EE512-120-4C- PH
SST29EE512- 90-3C- EH	SST29EE512- 90-3C- NH	SST29EE512- 90-3C- PH
SST29EE512-120-3C- EH	SST29EE512-120-3C- NH	SST29EE512-120-3C- PH
SST29EE512- 90-4I-EH	SST29EE512- 90-4I-NH	
SST29EE512-120-4I-EH	SST29EE512-120-4I-NH	SST29EE512-120-4C-U1
SST29EE512- 90-3I-EH	SST29EE512- 90-3I-NH	
SST29EE512-120-3I-EH	SST29EE512-120-3I-NH	SST29EE512-120-3C-U1

Example: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Data Sheet

SST 29LE512
3.0V-only 512 Kilobit
Page Mode EEPROM

July 1996

SST 29LE512
3.0V-only 512 Kilobit
Page Mode EEPROM

Features:

Single 3.0-Volt Read and Write Operations
CMOS SuperFlash EEPROM Technology
- Endurance: 100,000 Cycles (typical)
- Greater than 100 years Data Retention

Low Power Consumption:
- Active Current: 15 mA (typical)
- Standby Current: 10 µA (typical)

Fast Page-Write Operation
- 128 Bytes per Page, 512 Pages
- Page-Write Cycle: 5 ms (typical)
- Complete Memory Rewrite: 2.5 sec (typical)
- Effective Byte-write Cycle Time: 39 µs (typical)

Fast Access Time: 150 and 200 ns
Latched Address and Data
Automatic Write Timing with Internal V_{PP} Generation
End of Write Detection
- Toggle Bit
- Data# Polling

Hardware and Software Data Protection
TTL I/O Compatibility
JEDEC Standard Byte-wide EEPROM Pinouts
Packages Available
- 32-Pin TSOP
- 32-Lead PLCC
- 32 Pin Plastic DIP

Product Description

The 29LE512 is a 64K x 8 CMOS page mode EEPROM manufactured with SST's proprietary, high performance CMOS SuperFlash technology. The split gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The 29LE512 writes with a 3.0-volt-only power supply. (V_{CC}: 3.0V to 3.6V) Internal erase/program is transparent to the user. The 29LE512 conforms to JEDEC standard pinouts for byte-wide memories.

Featuring high performance page write, the 29LE512 provides a typical byte-write time of 39 µsec. The entire memory, i.e., 64K bytes, can be written page by page in as little as 2.5 seconds, when using interface features such as Toggle Bit or Data# Polling to indicate the completion of a write cycle. To protect against inadvertent write, the 29LE512 has on-chip hardware and software data protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, the 29LE512 is offered with a guaranteed page-write endurance of 10^4 or 10^3 cycles. Data retention is rated at greater than 100 years.

The 29LE512 is suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, the 29LE512 significantly improves performance and reliability, while lowering power consumption, when compared with floppy disk or EPROM approaches. The 29LE512 improves flexibility while lowering the cost for program, data, and configuration storage applications.

To meet high density, surface mount requirements, the 29LE512 is offered in 32-pin TSOP and 32-lead PLCC packages. A 600-mil, 32-pin PDIP package is also available. See Figures 2A and 2B for pinouts.

Device Operation

The SST page mode EEPROM offers in-circuit electrical write capability. The 29LE512 does not require separate erase and program operations. The internally timed write cycle executes both erase and program transparently to the user. The 29LE512 has industry standard optional Software Data Protection, which SST recommends always to be enabled. The 29LE512 is compatible with industry standard EEPROM pinouts and functionality.

Read

The read operation of the 29LE512 is controlled by CE# and OE#, both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the read cycle timing diagram for further details (Figure 3).

Write

The write operation consists of three steps. The first step is the optional three byte load sequence for Software Data Protection. This is an optional first step in the write operation, but highly recommended to ensure proper data integrity. Step 2 is the byte-load cycle to a page buffer of the 29LE512. Step 3 is an internally controlled write cycle for writing the data loaded in the page buffer into the memory array for nonvolatile storage. During the byte-load cycle, the addresses are latched by the falling edge of either CE# or WE#, whichever occurs last. The data is latched by the rising edge of either CE# or WE#, whichever occurs first. The internal write cycle is initiated by a timer after the rising edge of WE# or CE#, whichever occurs first. The write cycle, once initiated, will continue to completion, typically within 5 ms. See Figures 4 and 5 for WE# and CE# controlled page write cycle timing diagrams and Figures 15 and 17 for flowcharts.

The write operation has three functional cycles: the optional Software Data Protection load sequence, the page load cycle and the internal write cycle. The Software Data Protection consists of a specific three byte load sequence that will leave the 29LE512 protected at the end of the page write. The page load cycle consists of loading 1 to 128 bytes of data into the page buffer. The internal write cycle consists of the T_{BLCO} time-out and the write timer operation. During the write operation, the only valid reads are Data# Polling and Toggle Bit.

The page-write operation allows the loading of up to 128 bytes of data into the page buffer of the 29LE512 before the initiation of the internal write cycle. During the internal write cycle, all the data in the page buffer is written simultaneously into the memory array. Hence, the page-write feature of 29LE512 allows the entire memory to be written in as little as 2.5 seconds. During the internal write cycle, the host is free to perform additional tasks, such as to fetch data from other locations in the system to set up the write to the next page. In each page-write operation, all the bytes that are loaded into the page buffer must have the same page address, i.e., A_7 through A_{15}. Any byte not loaded with user data will be written to FF.

See Figures 4, 5, and 8 for the page-write cycle timing diagrams. If after the initial byte-load cycle, the host loads a second byte into the page buffer within a byte-load cycle time (T_{BLC}) of 100 µs, the 29LE512 will stay in the page load cycle. Additional bytes are then loaded consecutively. The page load cycle will be terminated if no additional byte is loaded into the page buffer within 200 µs (T_{BLCO}) from the last byte-load cycle, i.e., no subsequent WE# or CE# high-to-low transition after the last rising edge of WE# or CE#. Data in the page buffer can be changed by a subsequent byte-load cycle. The page load period can continue indefinitely, as long as the host continues to load the device within the byte-load cycle time of 100 µs. The page to be loaded is determined by the page address of the last byte loaded.

Software Chip-Erase

The 29LE512 provides a chip-erase operation, which allows the user to simultaneously clear the entire memory array to the "1" state. This is useful when the entire device must be quickly erased.

The Software Chip-Erase operation is initiated by using a specific six byte-load sequence. After the load sequence, the device enters into an internally timed cycle similar to the write cycle. During the erase operation, the only valid read is Toggle Bit. See Table 4 for the load sequence, Figure 10 for timing diagram, and Figure 19 for the flowchart.

Write Operation Status Detection

The 29LE512 provides two software means to detect the completion of a write cycle, in order to optimize the system write cycle time. The software detection includes two status bits: Data# Polling (DQ_7) and Toggle Bit (DQ_6). The end of write detection mode is enabled after the rising WE# or CE# whichever occurs first, which initiates the internal write cycle.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If

both reads are valid, then the device has completed the write cycle, otherwise the rejection is valid.

Data# Polling (DQ_7)

When the 29LE512 is in the internal write cycle, any attempt to read DQ_7 of the last byte loaded during the byte-load cycle will receive the complement of the true data. Once the write cycle is completed, DQ_7 will show true data. The device is then ready for the next operation. See Figure 6 for Data# Polling timing diagram and Figure 16 for a flowchart.

Toggle Bit (DQ_6)

During the internal write cycle, any consecutive attempts to read DQ_6 will produce alternating 0's and 1's, i.e., toggling between 0 and 1. When the write cycle is completed, the toggling will stop. The device is then ready for the next operation. See Figure 7 for Toggle Bit timing diagram and Figure 16 for a flowchart. The initial read of the Toggle Bit will be a "1".

Data Protection

The 29LE512 provides both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a write cycle.

V_{CC} Power Up/Down Detection: The write operation is inhibited when V_{CC} is less than 2.5V.

Write Inhibit Mode: Forcing OE# low, CE# high, or WE# high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down.

Software Data Protection (SDP)

The 29LE512 provides the JEDEC approved optional software data protection scheme for all data alteration operations, i.e., write and chip erase. With this scheme, any write operation requires the inclusion of a series of three byte-load operations to precede the data loading operation. The three byte-load sequence is used to initiate the write cycle, providing optimal protection from inadvertent write operations, e.g., during the system power-up or power-down. The 29LE512 is shipped with the software data protection disabled.

The software protection scheme can be enabled by applying a three-byte sequence to the device, during a page-load cycle (Figure 8). The device will then be automatically set into the data protect mode. Any subsequent write operation will require the preceding three-byte sequence. See Table 4 for the specific software command codes and Figure 8 for the timing diagram. To set the device into the unprotected mode, a six-byte sequence is required. See Table 4 for the specific codes and Figure 9 for the timing diagram. If a write is attempted while SDP is enabled the device will be in a non-accessible state for ~ 300 µs. SST recommends Software Data Protection always be enabled. See Figure 17 for flowcharts.

The 29LE512 Software Data Protection is a global command, protecting (or unprotecting) all pages in the entire memory array once enabled (or disabled). Therefore using SDP for a single page write will enable SDP for the entire array. Single pages by themselves cannot be SDP enabled or disabled.

Single power supply reprogrammable nonvolatile memories may be unintentionally altered. SST strongly recommends that Software Data Protection (SDP) always be enabled. The 29LE512 should be programmed using the SDP command sequence. SST recommends the SDP Disable Command Sequence not be issued to the device prior to writing.

Product Identification

The product identification mode identifies the device as the 29LE512 and manufacturer as SST. This mode may be accessed by hardware or software operations. The hardware operation is typically used by a programmer to identify the correct algorithm for the 29LE512. Users may wish to use the software product identification operation to identify the part (i.e., using the device code) when using multiple manufacturers in the same socket. For details, see Table 3 for hardware operation or Table 4 for software operation, Figure 11 for the software ID entry and read timing diagram and Figure 18 for the ID entry command sequence flowchart. The manufacturer and device codes are the same for both operations.

Table 1: Product Identification Table

	Byte	Data
Manufacturers Code	0000 H	BF H
Device Code	0001 H	3D H

Product Identification Mode Exit

In order to return to the standard read mode, the Software Product Identification mode must be exited. Exiting is accomplished by issuing the Software ID Exit (reset) operation, which returns the device to the read operation. The reset operation may also be used to reset the device to the read mode after an inadvertent transient condition that apparently causes the device to behave abnormally, e.g., not read correctly. See Table 4 for software command codes, Figure 12 for timing wavefrom and Figure 18 for a flowchart.

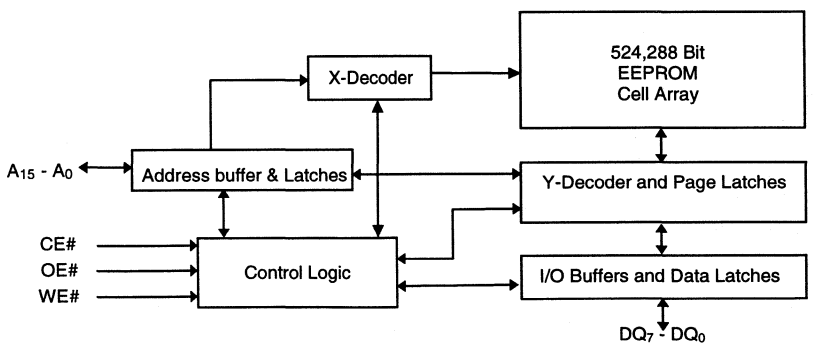


Figure 1: Functional Block Diagram of SST 29LE512

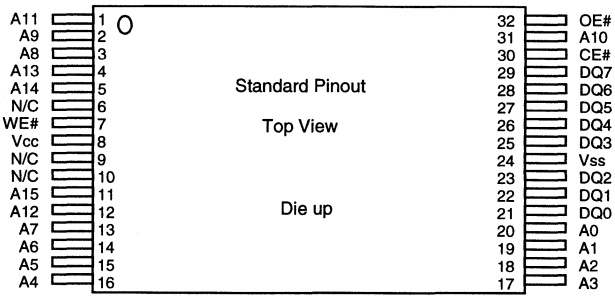


Figure 2A: Pin Assignments for 32-pin TSOP Packages

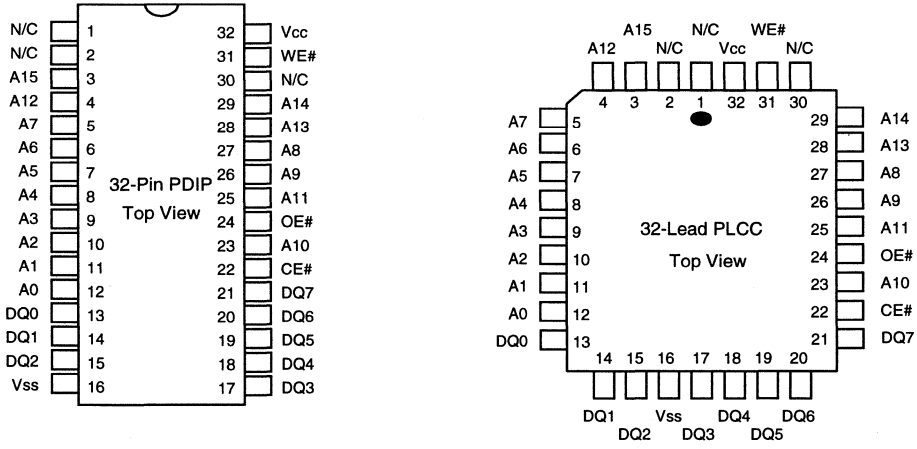


Figure 2B: Pin Assignments for 32-pin Plastic DIPs and 32-lead PLCCs

Table 2: Pin Description

Symbol	Pin Name	Functions
A_{15}-A_7	Row Address Inputs	To provide memory addresses. Row addresses define a page for a write cycle.
A_6-A_0	Column Address Inputs	Column Addresses are toggled to load page data.
DQ_7-DQ_0	Data Input/output	To output data during read cycles and receive input data during write cycles. Data is internally latched during a write cycle. The outputs are in tri-state when OE# or CE# is high.
CE#	Chip Enable	To activate the device when CE# is low.
OE#	Output Enable	To gate the data output buffers.
WE#	Write Enable	To control the write operations
Vcc	Power Supply	To provide 3.3-volt supply (± 0.3V)
Vss	Ground	
NC	No Connection	Unconnected pins.

Table 3: Operation Modes Selection

Mode	CE#	OE#	WE#	DQ	Address
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	A_{IN}
Page Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}
Standby	V_{IH}	X	X	High Z	X
Write Inhibit	X	V_{IL}	X	High Z/ D_{OUT}	X
Write Inhibit	X	X	V_{IH}	High Z/ D_{OUT}	X
Software Chip Erase	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}, See Table 4
Product Identification					
Hardware Mode	V_{IL}	V_{IL}	V_{IH}	Manufacturer Code (BF)	A_{15} - A_1 = V_{IL}, A_9 = V_H, A_0 = V_{IL}
				Device Code (3D)	A_{15} - A_1 = V_{IL}, A_9 = V_H, A_0= V_{IH}
Software Mode	V_{IL}	V_{IH}	V_{IL}		See Table 4
SDP Enable Mode	V_{IL}	V_{IH}	V_{IL}		See Table 4
SDP Disable Mode	V_{IL}	V_{IH}	V_{IL}		See Table 4

Table 4: Software Command Codes

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data
Software Data Protect Enable & Page Write	5555H	AAH	2AAAH	55H	5555H	A0H	Addr[2]	Data				
Software Data Protect Disable	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	20H
Software Chip Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry	5555H	AAH	2AAAH	55H	5555H	90H						
Software ID Exit	5555H	AAH	2AAAH	55H	5555H	F0H						
Alternate Software ID Entry[3]	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	60H

Notes: (1) Address format A_{14}-A_0 (Hex), Address A_{15} is a "Don't Care".

(2) Page Write consists of loading up to 128 bytes (A_6 - A_0).

(3) Alternate 6 byte Software Product ID Command Code

Notes for Software Product ID Command Code:

1. With A_{14}-A_1 =0; SST Manufacturer Code = BFH, is read with A_0 = 0,
   29LE512 Device Code = 3DH, is read with A_0 = 1.
2. The device does not remain in Software Product ID Mode if powered down.
3. This product supports both the JEDEC standard 3 byte command code sequence and SST's original 6 byte command code sequence. For new designs, SST recommends that the 3 byte command code sequence be used.

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential ..... -0.5V to V_{CC}+ 0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential ..... -1.0V to V_{CC}+ 1.0V
Voltage on A_9 Pin to Ground Potential ..... -0.5V to 14.0V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Through Hole Lead Soldering Temperature (10 Seconds) ..... 300°C
Surface Mount Lead Soldering Temperature (3 Seconds) ..... 240°C
Output Short Circuit Current[1] ..... 100 mA

Note: [1] Outputs shorted for no more than one second. No more than one output shorted at a time.

Operating Range

Range	Ambient Temp	V_{CC}
Commercial	0 °C to +70 °C	3.0V to 3.6V
Industrial	-40 °C to +85 °C	3.0V to 3.6V

AC Conditions of Test

Input Rise/Fall Time.....10 ns
Output Load.....1 TTL Gate and C_L = 100 pF
See Figures 13 and 14

Table 5: DC Operating Characteristics

Symbol	Parameter	Limits Min	Limits Max	Limits Units	Test Conditions
I_{CC}	Power Supply Current				CE#=OE#=V_{IL},WE#=V_{IH}, all I/Os open,
	Read		12	mA	Address input = V_{IL}/V_{IH}, at f=1/T_{RC} Min., V_{CC}=V_{CC} Max
	Write		15	mA	CE#=WE#=V_{IL}, OE#=V_{IH}, V_{CC} =V_{CC} Max.
I_{SB1}	Standby V_{CC} Current (TTL input)		1	mA	CE#=OE#=WE#=V_{IH}, V_{CC} =V_{CC} Max.
I_{SB2}	Standby V_{CC} Current (CMOS input)		15	µA	CE#=OE#=WE#=V_{CC} -0.3V. V_{CC} = V_{CC} Max.
I_{LI}	Input Leakage Current		1	µA	V_{IN} =GND to V_{CC}, V_{CC} = V_{CC} Max.
I_{LO}	Output Leakage Current		10	µA	V_{OUT} =GND to V_{CC}, V_{CC} = V_{CC} Max.
V_{IL}	Input Low Voltage		0.8	V	V_{CC} = V_{CC} Max.
V_{IH}	Input High Voltage	2.0		V	V_{CC} = V_{CC} Max.
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 100 µA, V_{CC} = V_{CC} Min.
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -100 µA, V_{CC} = V_{CC} Min.
V_H	Supervoltage for A_9	11.6	12.4	V	CE# = OE# =V_{IL}, WE# = V_{IH}
I_H	Supervoltage Current for A_9		200	µA	CE# = OE# = V_{IL}, WE# = V_{IH}, A_9 = V_H Max.

Table 6: Power-up Timings

Symbol	Parameter	Maximum	Units
$T_{PU-READ}$ [1]	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$ [1]	Power-up to Write Operation	5	ms

Table 7: Capacitance (Ta = 25 °C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$ [1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN} [1]	Input Capacitance	V_{IN} = 0v	6 pF

Note: [1]This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 8: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}	Endurance	1,000 & 10,000[2]	Cycles	MIL-STD-883, Method 1033
T_{DR} [1]	Data Retention	100	Years	MIL-STD-883, Method 1008
V_{ZAP_HBM} [1]	ESD Susceptibility Human Body Model	1000	Volts	JEDEC Standard A114
V_{ZAP_MM} [1]	ESD Susceptibility Machine Model	200	Volts	JEDEC
I_{LTH} [1]	Latch Up	100	mA	JEDEC Standard 17

Note: [1]This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

[2]See Ordering Information for desired type.

AC Characteristics

Table 9: Read Cycle Timing Parameters

Symbol	Parameter	29LE512-150		29LE512-200		Units
		Min	Max	Min	Max	
T_{RC}	Read Cycle Time	150		200		ns
T_{CE}	Chip Enable Access Time		150		200	ns
T_{AA}	Address Access Time		150		200	ns
T_{OE}	Output Enable Access Time		60		100	ns
T_{CLZ}[1]	CE# Low to Active Output	0		0		ns
T_{OLZ}[1]	OE# Low to Active Output	0		0		ns
T_{CHZ}[1]	CE# High to High-Z Output		30		50	ns
T_{OHZ}[1]	OE# High to High-Z Output		30		50	ns
T_{OH}[1]	Output Hold from Address Change	0		0		ns

Table 10: Page-Write Cycle Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{WC}	Write Cycle (erase and program)		10	ms
T_{AS}	Address Setup Time	0		ns
T_{AH}	Address Hold Time	50		ns
T_{CS}	WE# and CE# Setup Time	0		ns
T_{CH}	WE# and CE# Hold Time	0		ns
T_{OES}	OE# High Setup Time	0		ns
T_{OEH}	OE# High Hold Time	0		ns
T_{CP}	CE# Pulse Width	70		ns
T_{WP}	WE# Pulse Width	70		ns
T_{DS}	Data Setup Time	35		ns
T_{DH}	Data Hold Time	0		ns
T_{BLC}[1]	Byte Load Cycle Time	0.05	100	µs
T_{BLCO}[1]	Byte Load Cycle Time	200		µs
T_{IDA}	Software ID Access and Exit Time		10	µs
T_{SCE}	Software Chip Erase		20	ms

Note: [1]This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.

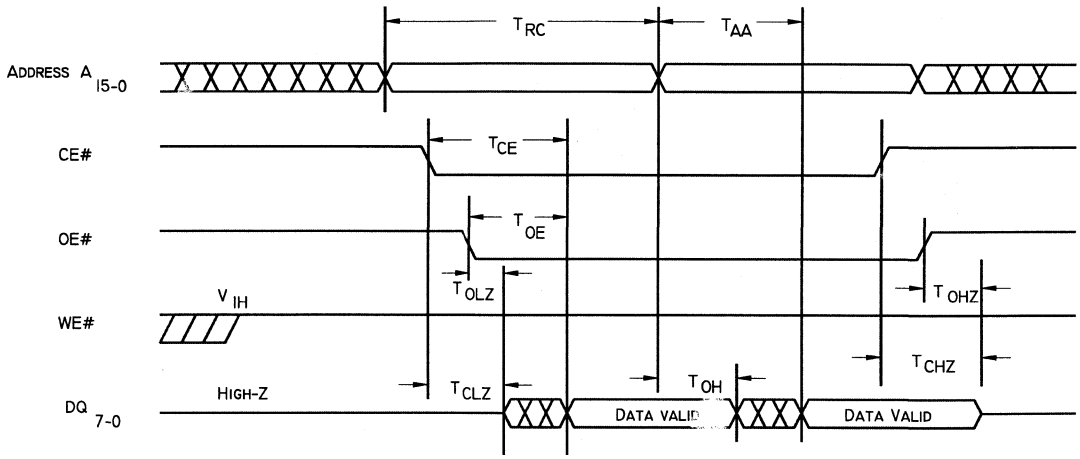


Figure 3: Read Cycle Timing Diagram

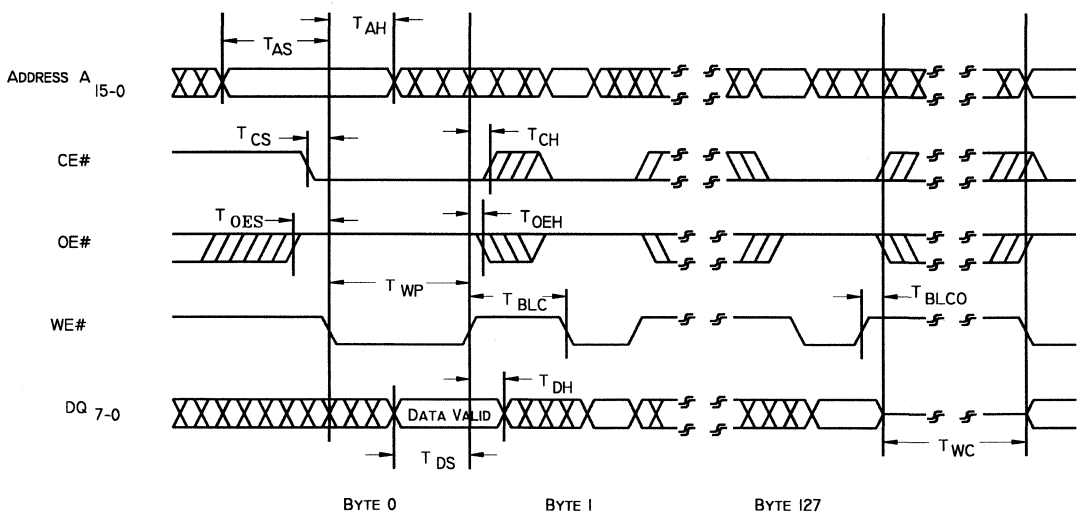


Figure 4: WE# Controlled Page Write Cycle Timing Diagram

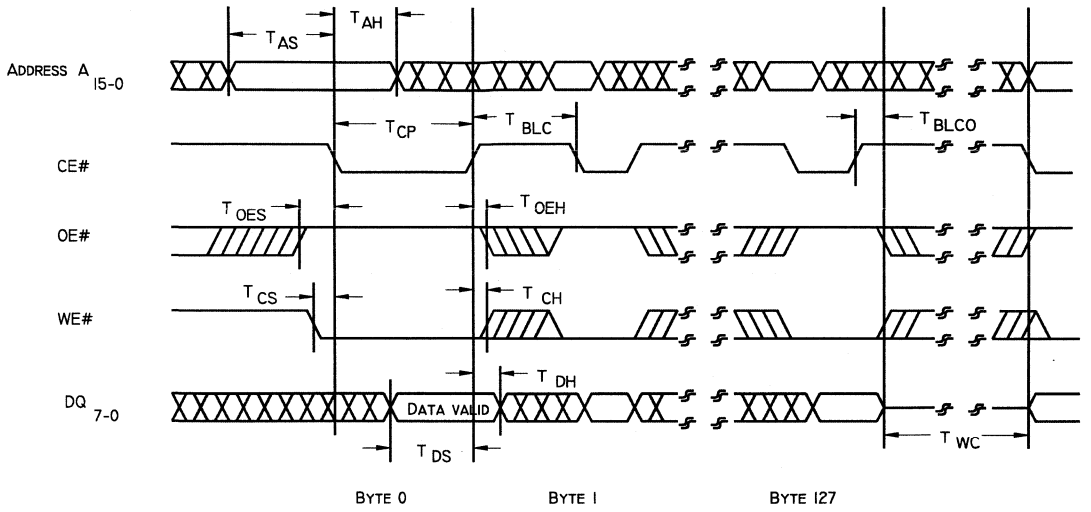


Figure 5: CE# Controlled Page Write Cycle Timing Diagram

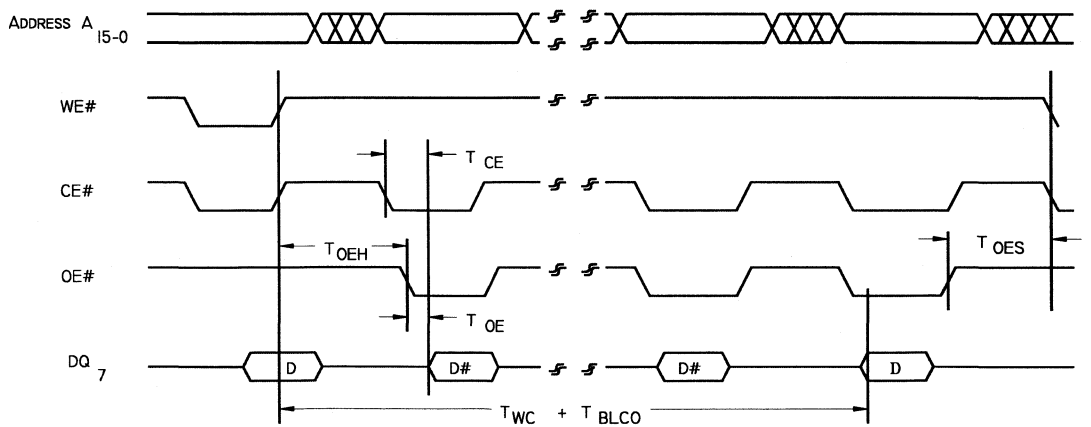


Figure 6: Data# Polling Timing Diagram

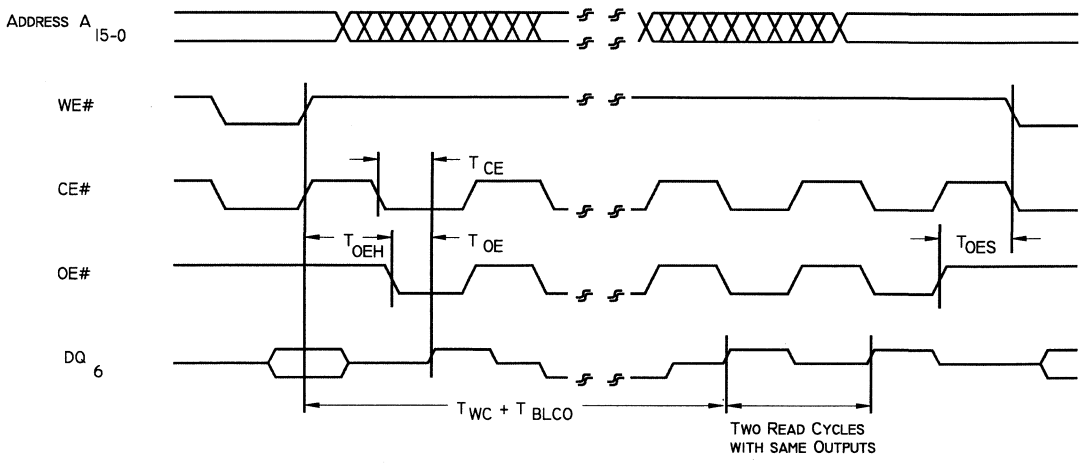
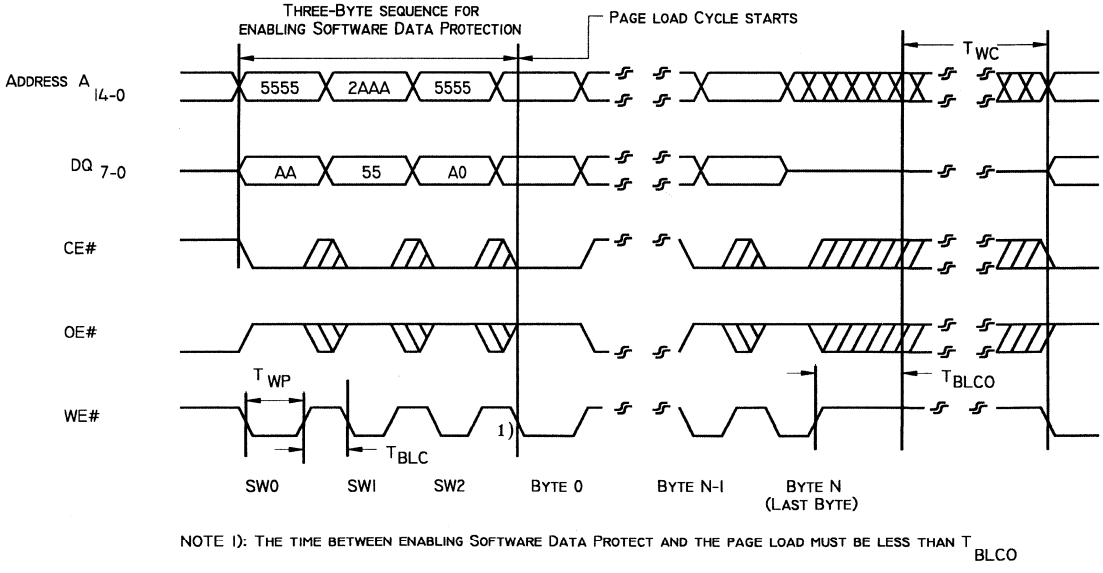


Figure 7: Toggle Bit Timing Diagram



NOTE 1): THE TIME BETWEEN ENABLING SOFTWARE DATA PROTECT AND THE PAGE LOAD MUST BE LESS THAN T_{BLCO}

Figure 8: Software Data Protection Page Write Timing Diagram

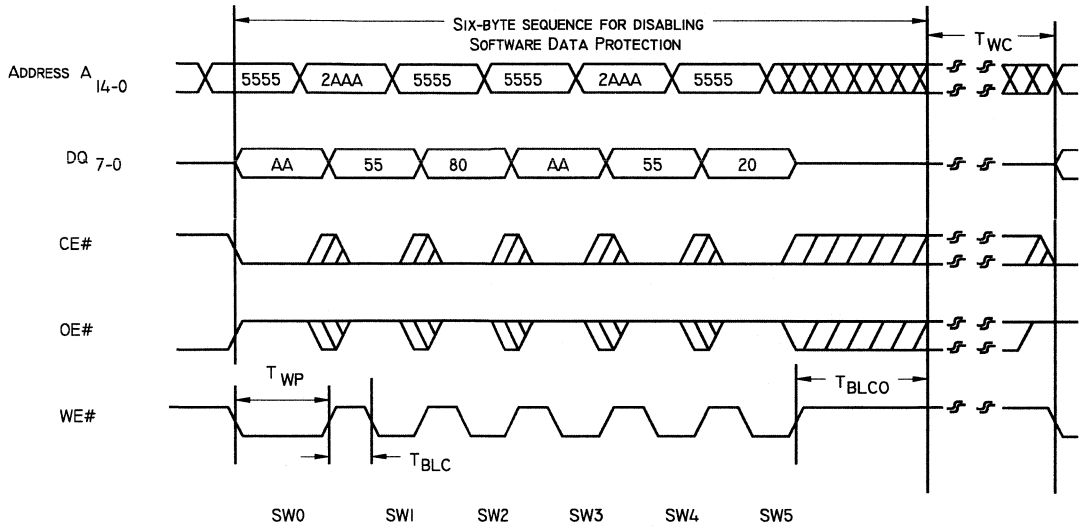


Figure 9: Software Data Protect Disable Timing Diagram

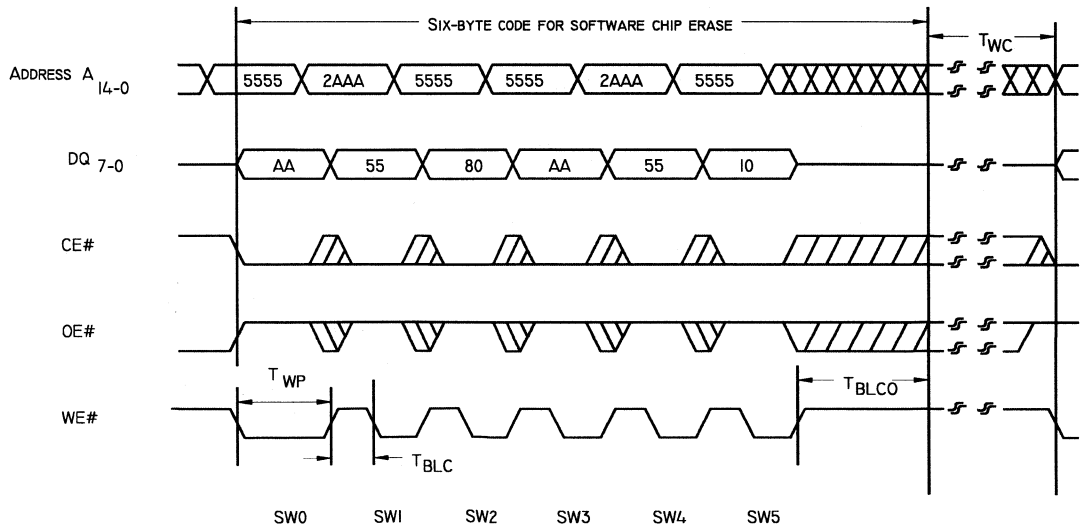


Figure 10: Software Chip Erase Timing Diagram

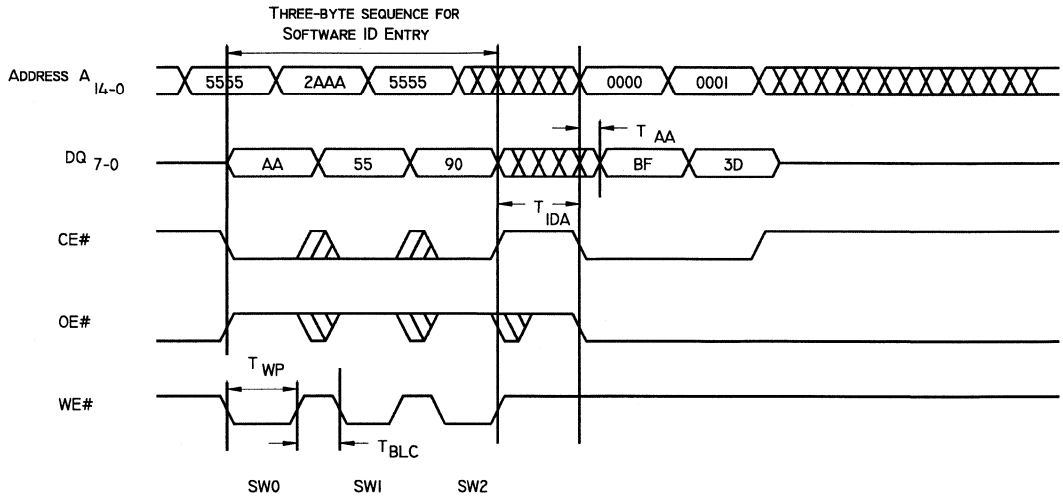


Figure 11: Software ID Entry and Read

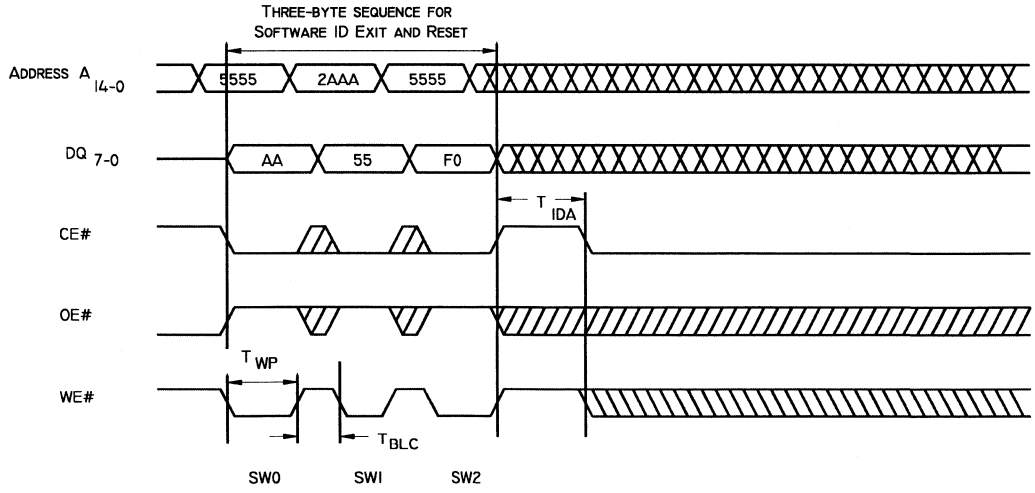
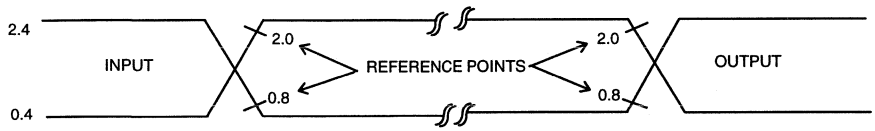


Figure 12: Software ID Exit and Reset



AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a logic "1" and V_{OL} (0.4 V_{TTL}) for a logic "0". Measurement reference points for inputs and outputs are V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Inputs rise and fall times (10% ↔ 90%) are <10 ns.

Figure 13: AC Input/Output Reference Waveforms

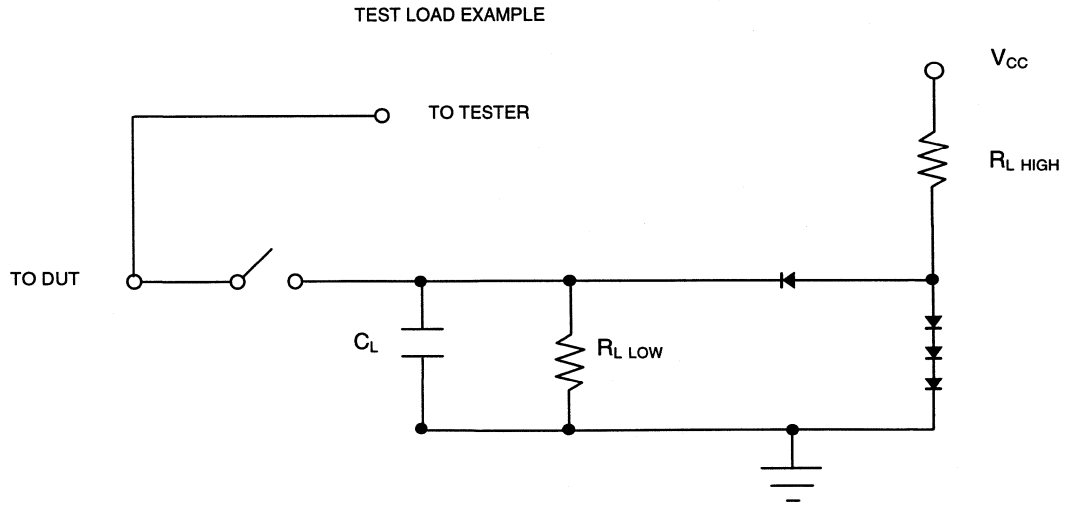


Figure 14: Test Load Example

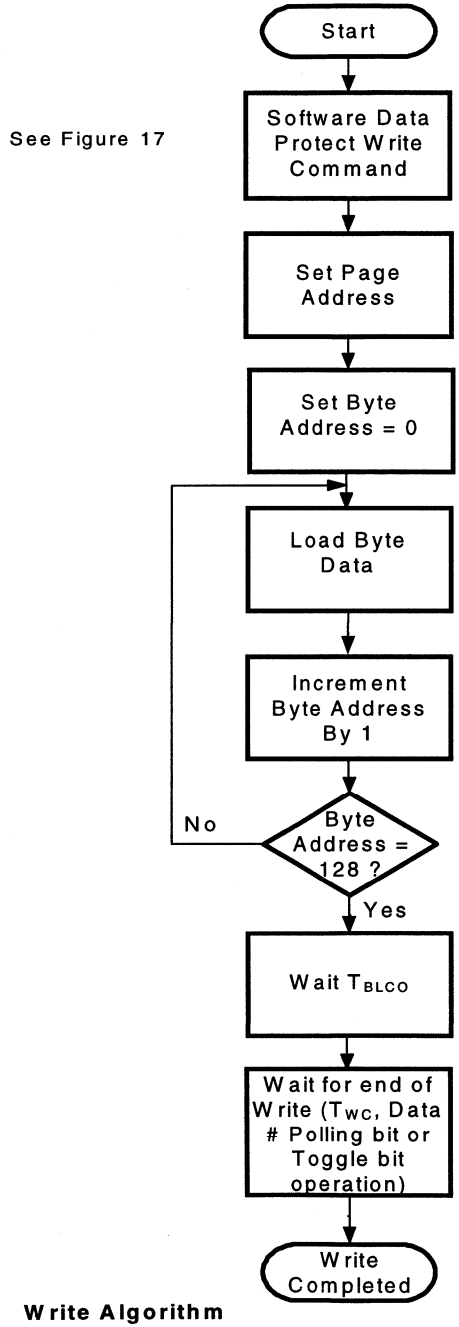


Figure 15: Write Algorithm

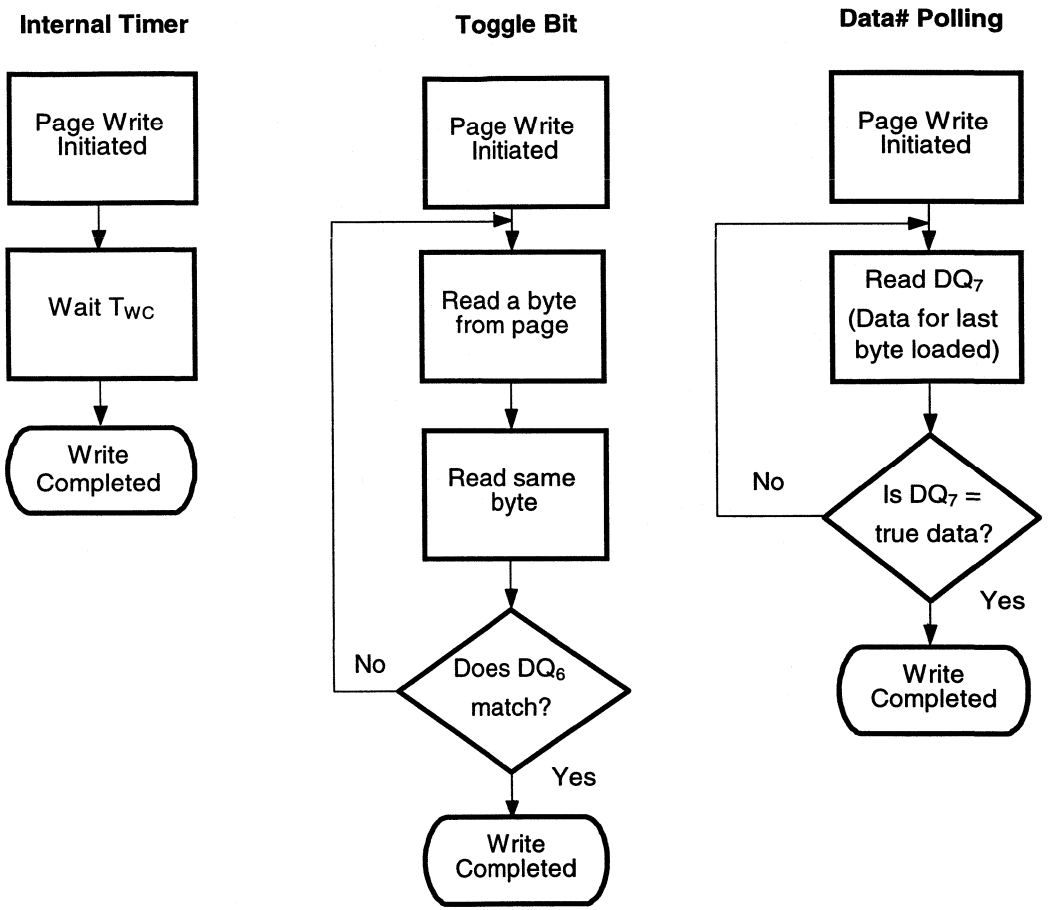


Figure 16: Wait Options

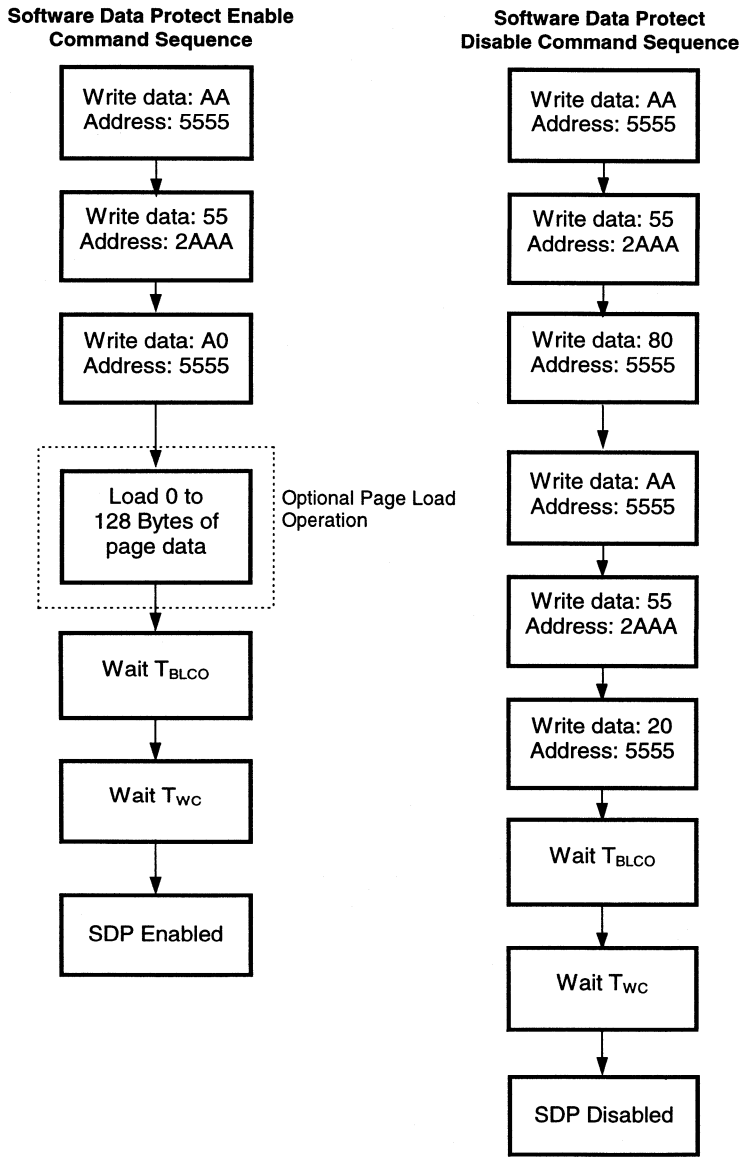


Figure 17: Software Data Protection Flowcharts

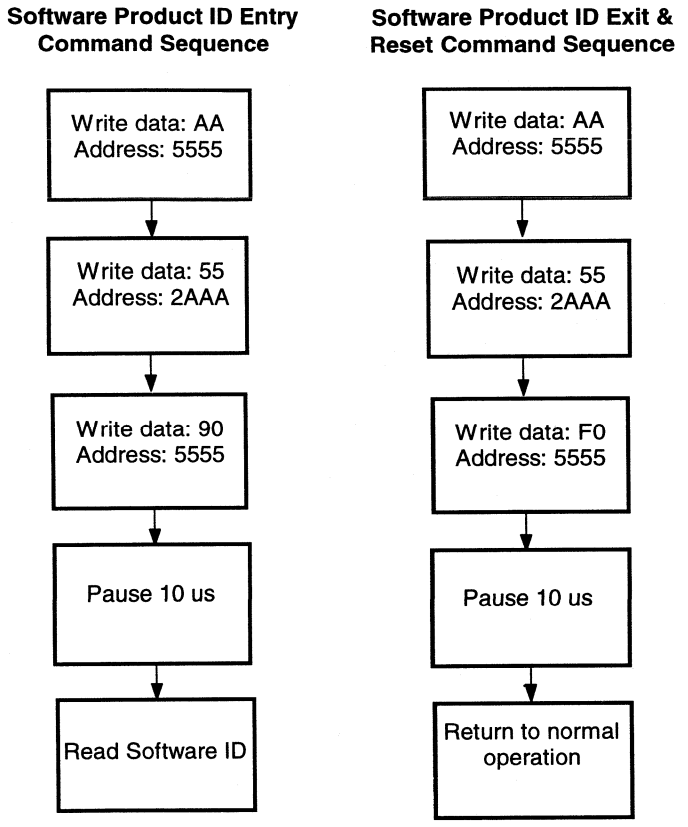


Figure 18: Software Product Command Flowcharts

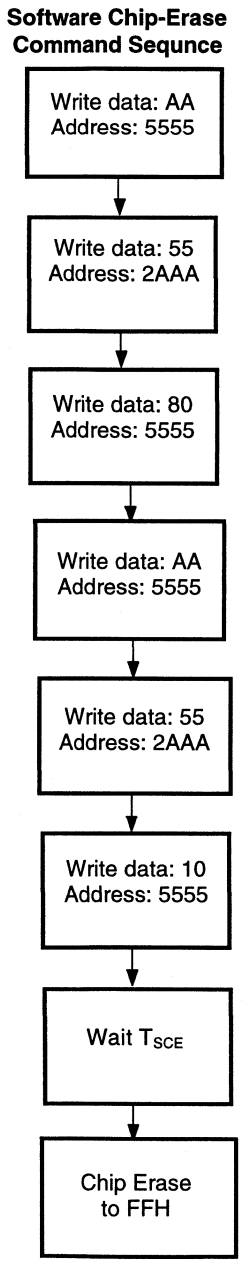
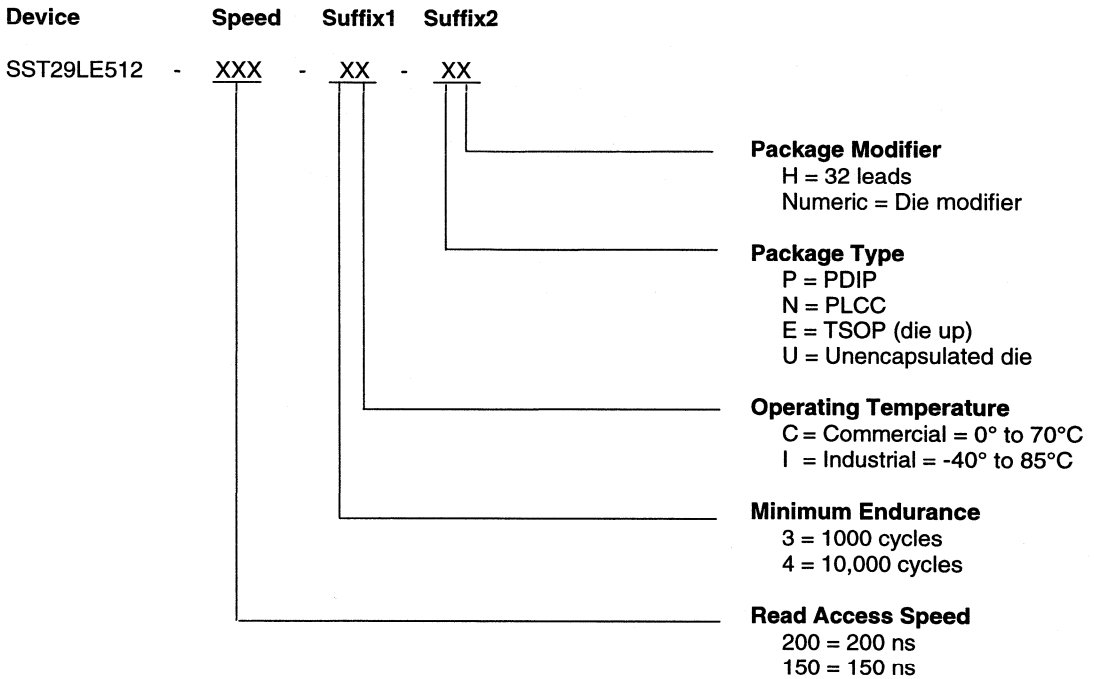


Figure 19: Software Chip Erase Command Codes

Product Ordering Information



Valid combinations

SST29LE512-150-4C- EH	SST29LE512-150-4C- NH	SST29LE512-150-4C- PH
SST29LE512-200-4C- EH	SST29LE512-200-4C- NH	SST29LE512-200-4C- PH
SST29LE512-150-3C- EH	SST29LE512-150-3C- NH	SST29LE512-150-3C- PH
SST29LE512-200-3C- EH	SST29LE512-200-3C- NH	SST29LE512-200-3C- PH
SST29LE512-150-4I-EH	SST29LE512-150-4I-NH	
SST29LE512-200-4I-EH	SST29LE512-200-4I-NH	SST29LE512-200-4C-U1
SST29LE512-150-3I-EH	SST29LE512-150-3I-NH	
SST29LE512-200-3I-EH	SST29LE512-200-3I-NH	SST29LE512-200-3C-U1

Example: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Data Sheet

SST 29VE512
2.7V-only 512 Kilobit
Page Mode EEPROM

July 1996

SST 29VE512
2.7V-only 512 Kilobit
Page Mode EEPROM

Features:

Single 2.7-Volt Read and Write Operations
CMOS SuperFlash EEPROM Technology
- Endurance: 100,000 Cycles (typical)
- Greater than 100 years Data Retention

Low Power Consumption:
- Active Current: 15 mA (typical)
- Standby Current: 10 µA (typical)

Fast Page-Write Operation
- 128 Bytes per Page, 512 Pages
- Page-Write Cycle: 5 ms (typical)
- Complete Memory Rewrite: 2.5 sec.(typical)
- Effective Byte-write Cycle Time: 39 µs (typical)

Fast Access Time: 200 and 250 ns

Latched Address and Data
Automatic Write Timing with Internal V_{PP} Generation
End of Write Detection
- Toggle Bit
- Data# Polling

Hardware and Software Data Protection
TTL I/O Compatibility
JEDEC Standard Byte-wide EEPROM Pinouts
Packages Available
- 32-Pin TSOP
- 32-Lead PLCC
- 32 Pin Plastic DIP

Product Description

The 29VE512 is a 64K x 8 CMOS page mode EEPROM manufactured with SST's proprietary, high performance CMOS SuperFlash technology. The split gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The 29VE512 writes with a 2.7-volt-only power supply. (V_{CC}: 2.7V to 3.6V) Internal erase/program is transparent to the user. The 29VE512 conforms to JEDEC standard pinouts for byte-wide memories.

Featuring high performance page write, the 29VE512 provides a typical byte-write time of 39 µsec. The entire memory, i.e., 64K bytes, can be written page by page in as little as 2.5 seconds, when using interface features such as Toggle Bit or Data# Polling to indicate the completion of a write cycle. To protect against inadvertent write, the 29VE512 has on-chip hardware and software data protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, the 29VE512 is offered with a guaranteed page-write endurance of 10^4 or 10^3 cycles. Data retention is rated at greater than 100 years.

The 29VE512 is suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, the 29VE512 significantly improves performance and reliability, while lowering power consumption, when compared with floppy disk or EPROM approaches. The 29VE512 improves flexibility while lowering the cost for program, data, and configuration storage applications.

To meet high density, surface mount requirements, the 29VE512 is offered in 32-pin TSOP and 32-lead PLCC packages. A 600-mil, 32-pin PDIP package is also available. See Figures 2A and 2B for pinouts.

Device Operation

The SST page mode EEPROM offers in-circuit electrical write capability. The 29VE512 does not require separate erase and program operations. The internally timed write cycle executes both erase and program transparently to the user. The 29VE512 has industry standard optional Software Data Protection, which SST recommends always to be enabled. The 29VE512 is compatible with industry standard EEPROM pinouts and functionality.

Read

The read operation of the 29VE512 is controlled by CE# and OE#, both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the read cycle timing diagram for further details (Figure 3).

Write

The write operation consists of three steps. The first step is the optional three byte load sequence for Software Data Protection. This is an optional first step in the write operation, but highly recommended to ensure proper data integrity. Step 2 is the byte-load cycle to a page buffer of the 29VE512. Step 3 is an internally controlled write cycle for writing the data loaded in the page buffer into the memory array for nonvolatile storage. During the byte-load cycle, the addresses are latched by the falling edge of either CE# or WE#, whichever occurs last. The data is latched by the rising edge of either CE# or WE#, whichever occurs first. The internal write cycle is initiated by a timer after the rising edge of WE# or CE#, whichever occurs first. The write cycle, once initiated, will continue to completion, typically within 5 ms. See Figures 4 and 5 for WE# and CE# controlled page write cycle timing diagrams and Figures 15 and 17 for flowcharts.

The write operation has three functional cycles: the optional Software Data Protection load sequence, the page load cycle and the internal write cycle. The Software Data Protection consists of a specific three byte load sequence that will leave the 29VE512 protected at the end of the page write. The page load cycle consists of loading 1 to 128 bytes of data into the page buffer. The internal write cycle consists of the T_{BLCO} time-out and the write timer operation. During the write operation, the only valid reads are Data# Polling and Toggle Bit.

The page-write operation allows the loading of up to 128 bytes of data into the page buffer of the 29VE512 before the initiation of the internal write cycle. During the internal write cycle, all the data in the page buffer is written simultaneously into the memory array. Hence, the page-write feature of 29VE512 allows the entire memory to be written in as little as 2.5 seconds. During the internal write cycle, the host is free to perform additional tasks, such as to fetch data from other locations in the system to set up the write to the next page. In each page-write operation, all the bytes that are loaded into the page buffer must have the same page address, i.e., A_7 through A_{15}. Any byte not loaded with user data will be written to FF.

See Figures 4, 5, and 8 for the page-write cycle timing diagrams. If after the initial byte-load cycle, the host loads a second byte into the page buffer within a byte-load cycle time (T_{BLC}) of 100 µs, the 29VE512 will stay in the page load cycle. Additional bytes are then loaded consecutively. The page load cycle will be terminated if no additional byte is loaded into the page buffer within 200 µs (T_{BLCO}) from the last byte-load cycle, i.e., no subsequent WE# or CE# high-to-low transition after the last rising edge of WE# or CE#. Data in the page buffer can be changed by a subsequent byte-load cycle. The page load period can continue indefinitely, as long as the host continues to load the device within the byte-load cycle time of 100 µs. The page to be loaded is determined by the page address of the last byte loaded.

Software Chip-Erase

The 29VE512 provides a chip-erase operation, which allows the user to simultaneously clear the entire memory array to the "1" state. This is useful when the entire device must be quickly erased.

The Software Chip-Erase operation is initiated by using a specific six byte-load sequence. After the load sequence, the device enters into an internally timed cycle similar to the write cycle. During the erase operation, the only valid read is Toggle Bit. See Table 4 for the load sequence, Figure 10 for timing diagram, and Figure 19 for the flowchart.

Write Operation Status Detection

The 29VE512 provides two software means to detect the completion of a write cycle, in order to optimize the system write cycle time. The software detection includes two status bits: Data# Polling (DQ_7) and Toggle Bit (DQ_6). The end of write detection mode is enabled after the rising WE# or CE# whichever occurs first, which initiates the internal write cycle.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If

both reads are valid, then the device has completed the write cycle, otherwise the rejection is valid.

Data# Polling (DQ_7)

When the 29VE512 is in the internal write cycle, any attempt to read DQ_7 of the last byte loaded during the byte-load cycle will receive the complement of the true data. Once the write cycle is completed, DQ_7 will show true data. The device is then ready for the next operation. See Figure 6 for Data# Polling timing diagram and Figure 16 for a flowchart.

Toggle Bit (DQ_6)

During the internal write cycle, any consecutive attempts to read DQ_6 will produce alternating 0's and 1's, i.e., toggling between 0 and 1. When the write cycle is completed, the toggling will stop. The device is then ready for the next operation. See Figure 7 for Toggle Bit timing diagram and Figure 16 for a flowchart. The initial read of the Toggle Bit will be a "1".

Data Protection

The 29VE512 provides both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a write cycle.

V_{CC} Power Up/Down Detection: The write operation is inhibited when V_{CC} is less than 2.5V.

Write Inhibit Mode: Forcing OE# low, CE# high, or WE# high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down.

Software Data Protection (SDP)

The 29VE512 provides the JEDEC approved optional software data protection scheme for all data alteration operations, i.e., write and chip erase. With this scheme, any write operation requires the inclusion of a series of three byte-load operations to precede the data loading operation. The three byte-load sequence is used to initiate the write cycle, providing optimal protection from inadvertent write operations, e.g., during the system power-up or power-down. The 29VE512 is shipped with the software data protection disabled.

The software protection scheme can be enabled by applying a three-byte sequence to the device, during a page-load cycle (Figure 8). The device will then be automatically set into the data protect mode. Any subsequent write operation will require the preceding three-byte sequence. See Table 4 for the specific software command codes and Figure 8 for the timing diagram. To set the device into the unprotected mode, a six-byte sequence is required. See Table 4 for the specific codes and Figure 9 for the timing diagram. If a write is attempted while SDP is enabled the device will be in a non-accessible state for ~ 300 µs. SST recommends Software Data Protection always be enabled. See Figure 17 for flowcharts.

The 29VE512 Software Data Protection is a global command, protecting (or unprotecting) all pages in the entire memory array once enabled (or disabled). Therefore using SDP for a single page write will enable SDP for the entire array. Single pages by themselves cannot be SDP enabled or disabled.

Single power supply reprogrammable nonvolatile memories may be unintentionally altered. SST strongly recommends that Software Data Protection (SDP) always be enabled. The 29VE512 should be programmed using the SDP command sequence. SST recommends the SDP Disable Command Sequence not be issued to the device prior to writing.

Product Identification

The product identification mode identifies the device as the 29VE512 and manufacturer as SST. This mode may be accessed by hardware or software operations. The hardware operation is typically used by a programmer to identify the correct algorithm for the 29VE512. Users may wish to use the software product identification operation to identify the part (i.e., using the device code) when using multiple manufacturers in the same socket. For details, see Table 3 for hardware operation or Table 4 for software operation, Figure 11 for the software ID entry and read timing diagram and Figure 18 for the ID entry command sequence flowchart. The manufacturer and device codes are the same for both operations.

Table 1: Product Identification Table

	Byte	Data
Manufacturers Code	0000 H	BF H
Device Code	0001 H	3D H

Product Identification Mode Exit

In order to return to the standard read mode, the Software Product Identification mode must be exited. Exiting is accomplished by issuing the Software ID Exit (reset) operation, which returns the device to the read operation. The reset operation may also be used to reset the device to the read mode after an inadvertent transient condition that apparently causes the device to behave abnormally, e.g., not read correctly. See Table 4 for software command codes, Figure 12 for timing wavefrom and Figure 18 for a flowchart.

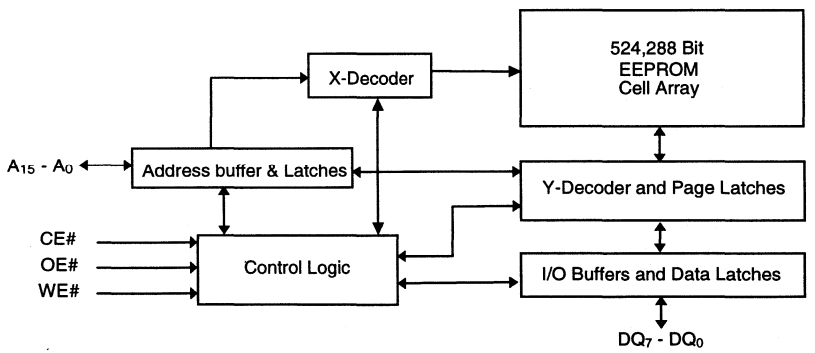


Figure 1: Functional Block Diagram of SST 29VE512

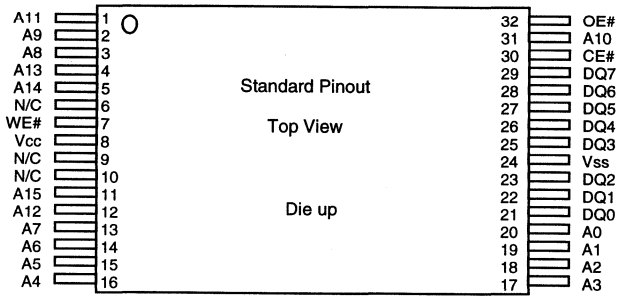


Figure 2A: Pin Assignments for 32-pin TSOP Packages

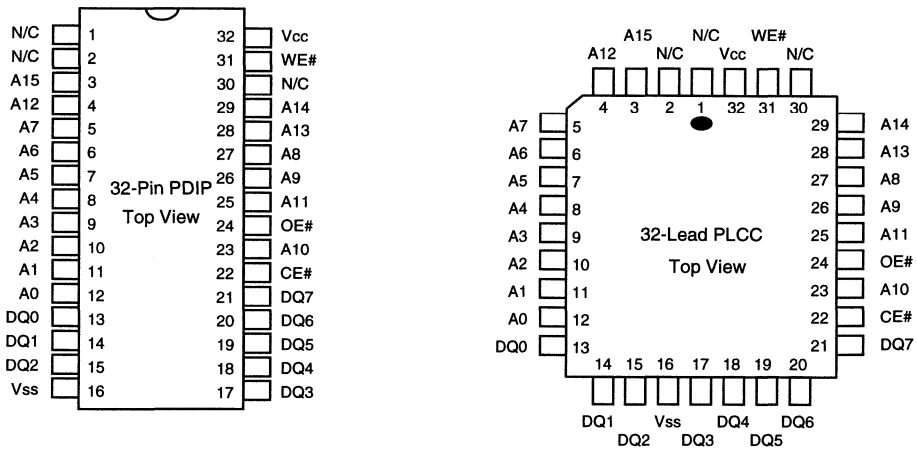


Figure 2B: Pin Assignments for 32-pin Plastic DIPs and 32-lead PLCCs

Table 2: Pin Description

Symbol	Pin Name	Functions
A_{15}-A_7	Row Address Inputs	To provide memory addresses. Row addresses define a page for a write cycle.
A_6-A_0	Column Address Inputs	Column Addresses are toggled to load page data.
DQ_7-DQ_0	Data Input/output	To output data during read cycles and receive input data during write cycles. Data is internally latched during a write cycle. The outputs are in tri-state when OE# or CE# is high.
CE#	Chip Enable	To activate the device when CE# is low.
OE#	Output Enable	To gate the data output buffers.
WE#	Write Enable	To control the write operations
Vcc	Power Supply	To provide 3-volt supply (2.7V-3.6V)
Vss	Ground	
NC	No Connection	Unconnected pins.

Table 3: Operation Modes Selection

Mode	CE#	OE#	WE#	DQ	Address
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	A_{IN}
Page Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}
Standby	V_{IH}	X	X	High Z	X
Write Inhibit	X	V_{IL}	X	High Z/ D_{OUT}	X
Write Inhibit	X	X	V_{IH}	High Z/ D_{OUT}	X
Software Chip Erase	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}, See Table 4
Product Identification					
Hardware Mode	V_{IL}	V_{IL}	V_{IH}	Manufacturer Code (BF)	A_{15} - A_1 = V_{IL}, A_9 = V_H, A_0 = V_{IL}
				Device Code (3D)	A_{15} - A_1 = V_{IL}, A_9 = V_H, A_0= V_{IH}
Software Mode	V_{IL}	V_{IH}	V_{IL}		See Table 4
SDP Enable Mode	V_{IL}	V_{IH}	V_{IL}		See Table 4
SDP Disable Mode	V_{IL}	V_{IH}	V_{IL}		See Table 4

Table 4: Software Command Codes

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data
Software Data Protect Enable & Page Write	5555H	AAH	2AAAH	55H	5555H	A0H	Addr[2]	Data				
Software Data Protect Disable	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	20H
Software Chip Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry	5555H	AAH	2AAAH	55H	5555H	90H						
Software ID Exit	5555H	AAH	2AAAH	55H	5555H	F0H						
Alternate Software ID Entry[3]	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	60H

Notes: (1) Address format A_{14}-A_0 (Hex), Address A_{15} is a "Don't Care".

(2) Page Write consists of loading up to 128 bytes (A_6 - A_0).

(3) Alternate 6 byte Software Product ID Command Code

Notes for Software Product ID Command Code:

1. With A_{14}-A_1 =0; SST Manufacturer Code = BFH, is read with A_0 = 0,
   29VE512 Device Code = 3DH, is read with A_0 = 1.
2. The device does not remain in Software Product ID Mode if powered down.
3. This product supports both the JEDEC standard 3 byte command code sequence and SST's original 6 byte command code sequence. For new designs, SST recommends that the 3 byte command code sequence be used.

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential ..... -0.5V to V_{CC}+ 0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential ..... -1.0V to V_{CC}+ 1.0V
Voltage on A_9 Pin to Ground Potential ..... -0.5V to 14.0V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Through Hole Lead Soldering Temperature (10 Seconds) ..... 300°C
Surface Mount Lead Soldering Temperature (3 Seconds) ..... 240°C
Output Short Circuit Current[1] ..... 100 mA

Note: [1] Outputs shorted for no more than one second. No more than one output shorted at a time.

Operating Range

Range	Ambient Temp	V_{CC}
Commercial	0 °C to +70 °C	2.7V to 3.6V
Industrial	-40 °C to +85 °C	2.7V to 3.6V

AC Conditions of Test

Input Rise/Fall Time.....10 ns
Output Load.....1 TTL Gate and C_L = 100 pF
See Figures 13 and 14

Table 5: DC Operating Characteristics

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{CC}	Power Supply Current				CE#=OE#=V_{IL},WE#=V_{IH}, all I/Os open,
	Read		12	mA	Address input = V_{IL}/V_{IH}, at f=1/T_{RC} Min., V_{CC}=V_{CC} Max
	Write		15	mA	CE#=WE#=V_{IL}, OE#=V_{IH}, V_{CC}=V_{CC} Max.
I_{SB1}	Standby V_{CC} Current (TTL input)		1	mA	CE#=OE#=WE#=V_{IH}, V_{CC}=V_{CC} Max.
I_{SB2}	Standby V_{CC} Current (CMOS input)		15	µA	CE#=OE#=WE#=V_{CC} -0.3V. V_{CC} = V_{CC} Max.
I_{LI}	Input Leakage Current		1	µA	V_{IN} =GND to V_{CC}, V_{CC} = V_{CC} Max.
I_{LO}	Output Leakage Current		10	µA	V_{OUT} =GND to V_{CC}, V_{CC} = V_{CC} Max.
V_{IL}	Input Low Voltage		0.8	V	V_{CC} = V_{CC} Max.
V_{IH}	Input High Voltage	2.0		V	V_{CC} = V_{CC} Max.
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 100 µA, V_{CC} = V_{CC} Min.
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -100 µA, V_{CC} = V_{CC} Min.
V_H	Supervoltage for A_9	11.6	12.4	V	CE# = OE# =V_{IL}, WE# = V_{IH}
I_H	Supervoltage Current for A_9		200	µA	CE# = OE# = V_{IL}, WE# = V_{IH}, A_9 = V_H Max.

Table 6: Power-up Timings

Symbol	Parameter	Maximum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$[1]	Power-up to Write Operation	5	ms

Table 7: Capacitance (Ta = 25 °C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pf
C_{IN}[1]	Input Capacitance	V_{IN} = 0v	6 pf

Note: [1]This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 8: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}	Endurance	1,000 & 10,000[2]	Cycles	MIL-STD-883, Method 1033
T_{DR}[1]	Data Retention	100	Years	MIL-STD-883, Method 1008
V_{ZAP_HBM}[1]	ESD Susceptibility Human Body Model	1000	Volts	JEDEC Standard A114
V_{ZAP_MM}[1]	ESD Susceptibility Machine Model	200	Volts	JEDEC
I_{LTH}[1]	Latch Up	100	mA	JEDEC Standard 17

Note: [1]This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

[2]See Ordering Information for desired type.

AC Characteristics

Table 9: Read Cycle Timing Parameters

Symbol	Parameter	29VE512-200		29VE512-250		Units
		Min	Max	Min	Max	
T_{RC}	Read Cycle Time	200		250		ns
T_{CE}	Chip Enable Access Time		200		250	ns
T_{AA}	Address Access Time		200		250	ns
T_{OE}	Output Enable Access Time		100		120	ns
T_{CLZ}[1]	CE# Low to Active Output	0		0		ns
T_{OLZ}[1]	OE# Low to Active Output	0		0		ns
T_{CHZ}[1]	CE# High to High-Z Output		50		50	ns
T_{OHZ}[1]	OE# High to High-Z Output		50		50	ns
T_{OH}[1]	Output Hold from Address Change	0		0		ns

Table 10: Page-Write Cycle Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{WC}	Write Cycle (erase and program)		10	ms
T_{AS}	Address Setup Time	0		ns
T_{AH}	Address Hold Time	50		ns
T_{CS}	WE# and CE# Setup Time	0		ns
T_{CH}	WE# and CE# Hold Time	0		ns
T_{OES}	OE# High Setup Time	0		ns
T_{OEH}	OE# High Hold Time	0		ns
T_{CP}	CE# Pulse Width	70		ns
T_{WP}	WE# Pulse Width	70		ns
T_{DS}	Data Setup Time	35		ns
T_{DH}	Data Hold Time	0		ns
T_{BLC}[1]	Byte Load Cycle Time	0.05	100	µs
T_{BLCO}[1]	Byte Load Cycle Time	200		µs
T_{IDA}	Software ID Access and Exit Time		10	µs
T_{SCE}	Software Chip Erase		20	ms

Note: [1]This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.

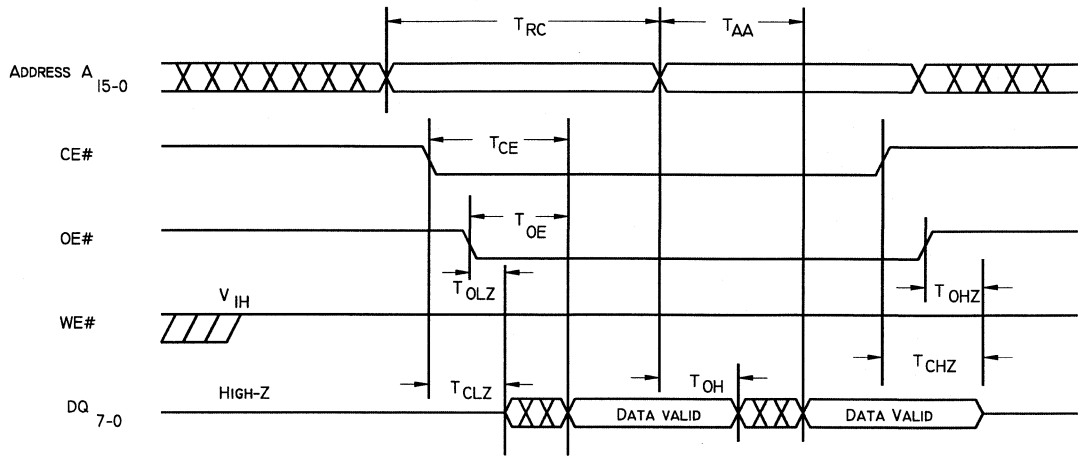


Figure 3: Read Cycle Timing Diagram

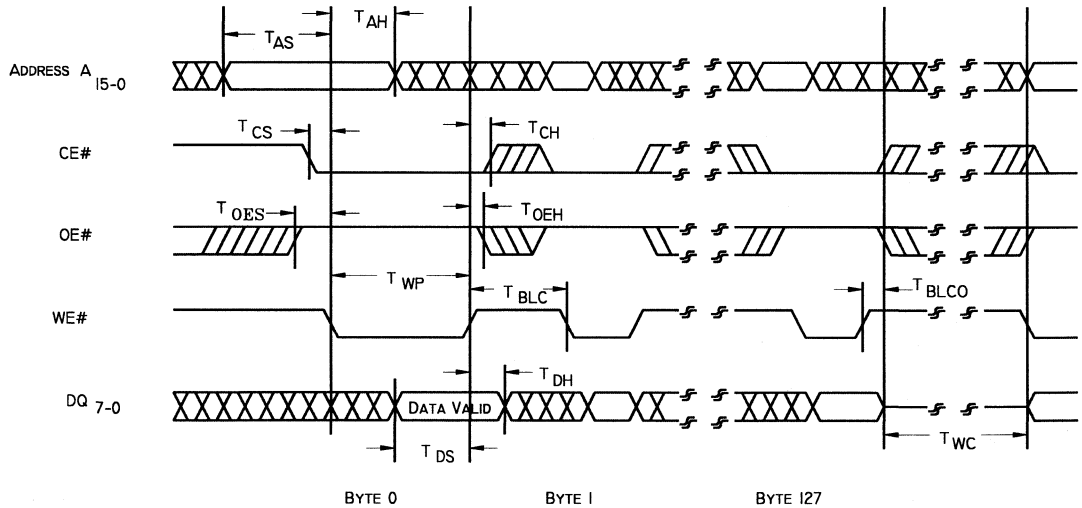


Figure 4: WE# Controlled Page Write Cycle Timing Diagram

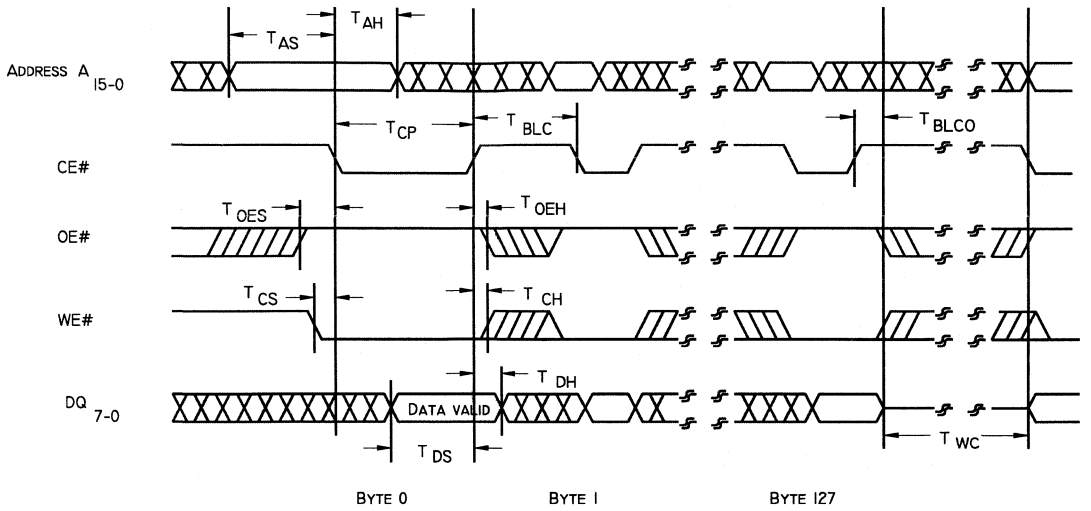


Figure 5: CE# Controlled Page Write Cycle Timing Diagram

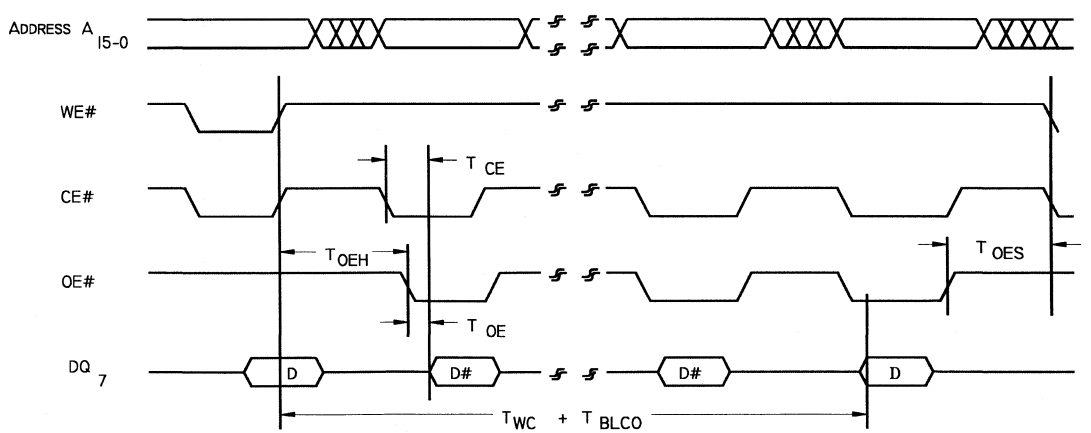


Figure 6: Data# Polling Timing Diagram

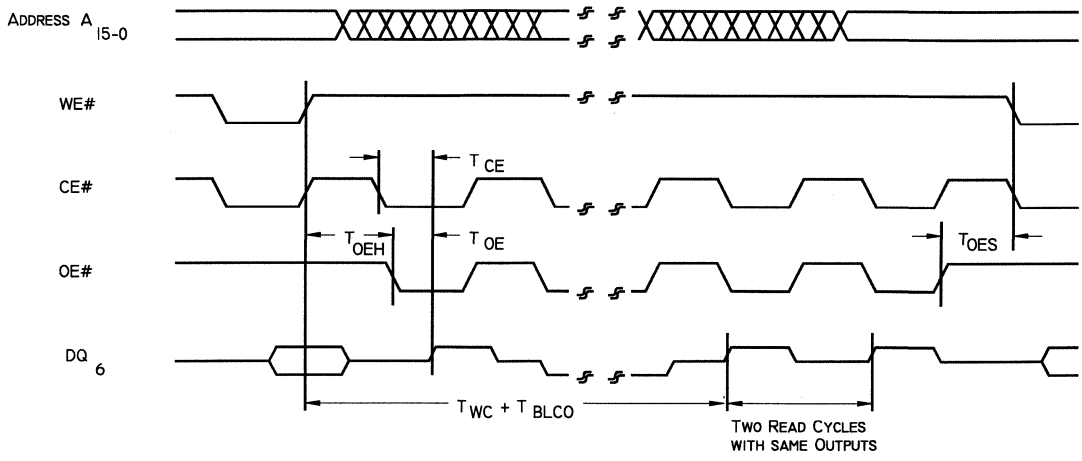
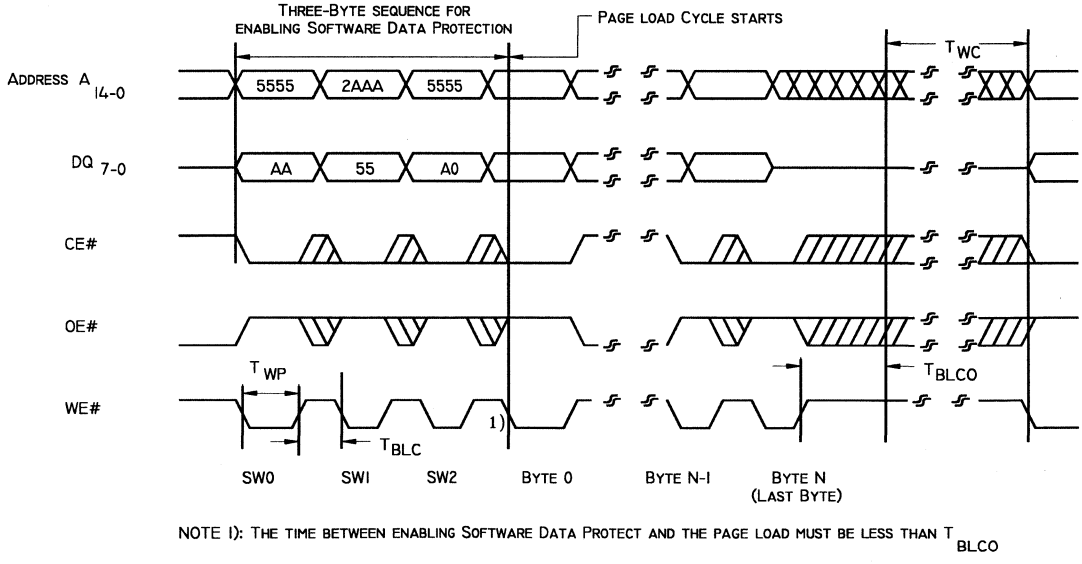


Figure 7: Toggle Bit Timing Diagram



NOTE 1): THE TIME BETWEEN ENABLING SOFTWARE DATA PROTECT AND THE PAGE LOAD MUST BE LESS THAN T_{BLCO}

Figure 8: Software Data Protection Page Write Timing Diagram

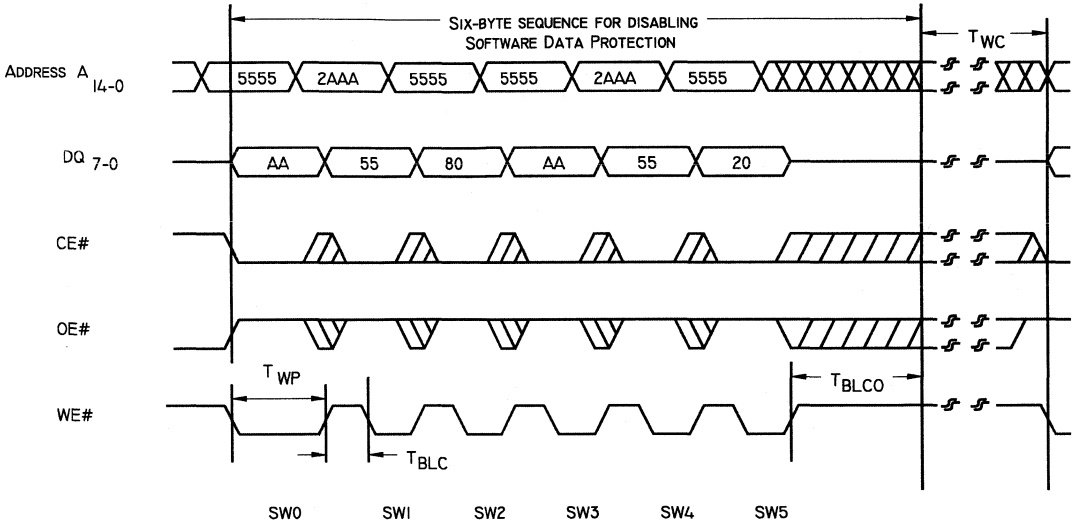


Figure 9: Software Data Protect Disable Timing Diagram

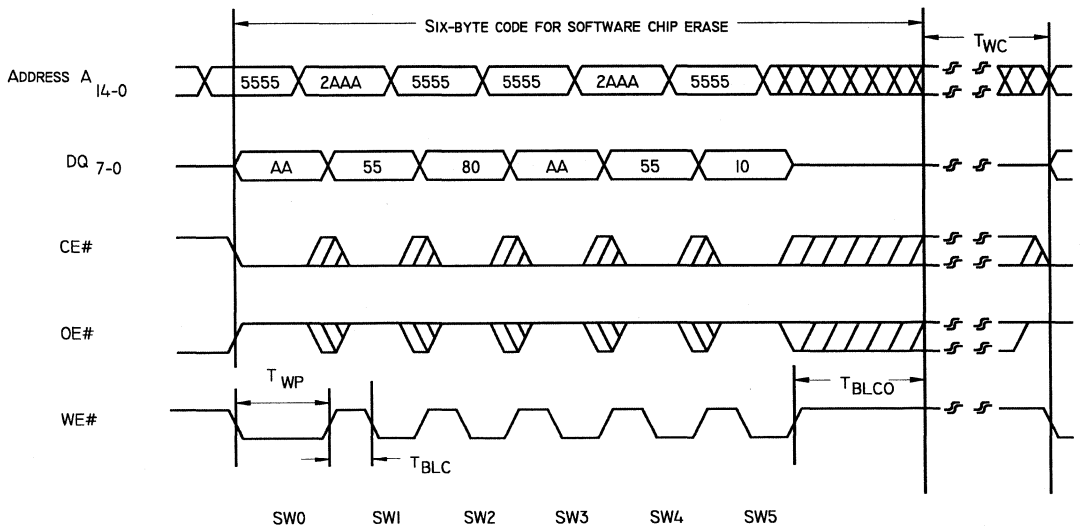


Figure 10: Software Chip Erase Timing Diagram

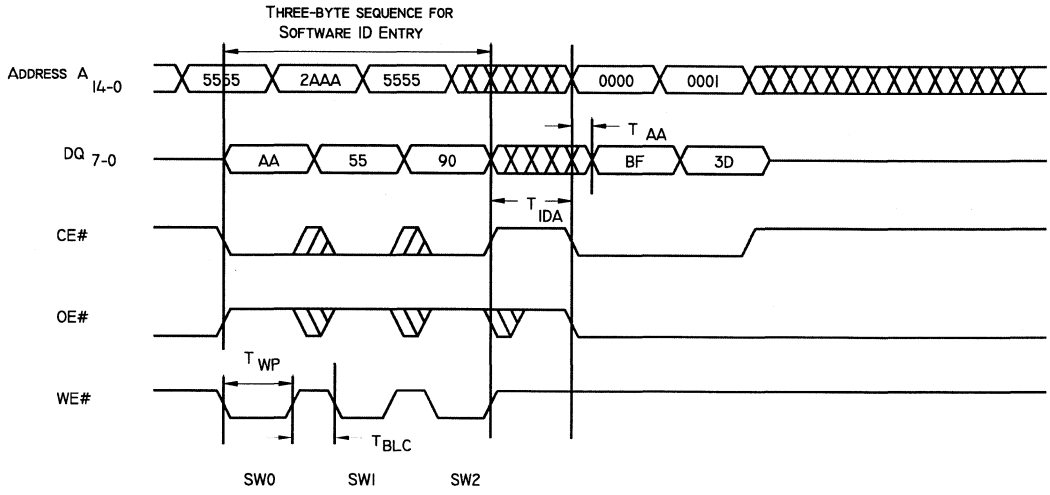


Figure 11: Software ID Entry and Read

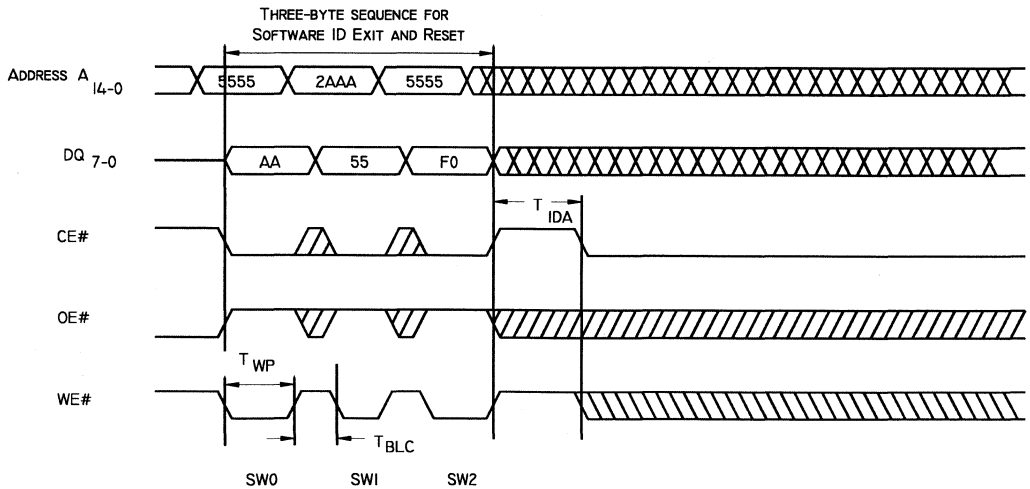
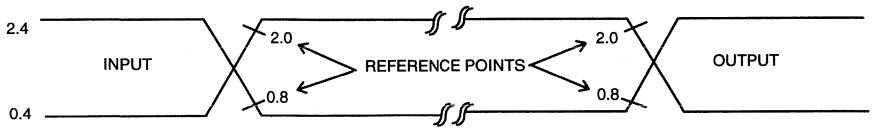


Figure 12: Software ID Exit and Reset



AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a logic "1" and V_{OL} (0.4 V_{TTL}) for a logic "0". Measurement reference points for inputs and outputs are V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Inputs rise and fall times (10% ↔ 90%) are <10 ns.

Figure 13: AC Input/Output Reference Waveforms

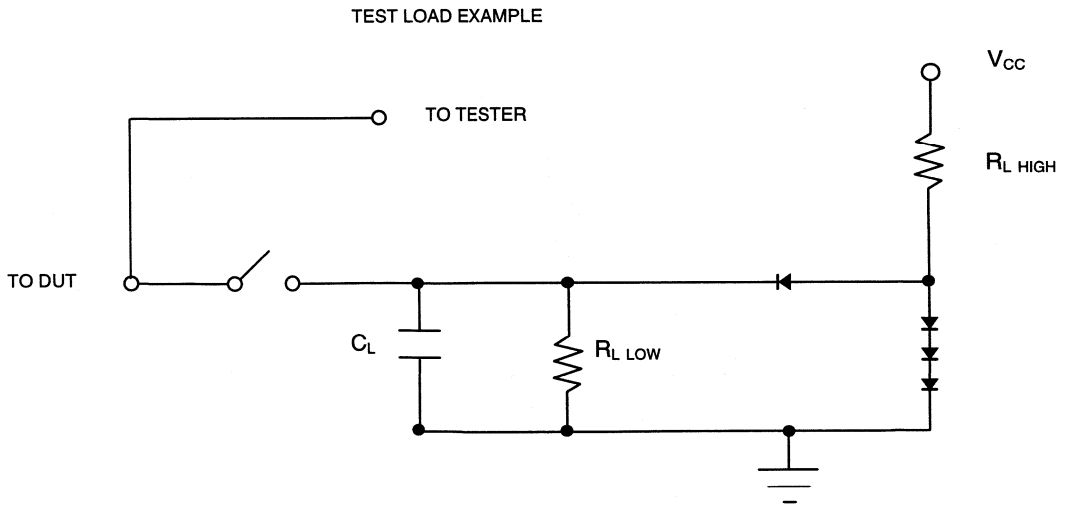


Figure 14: Test Load Example

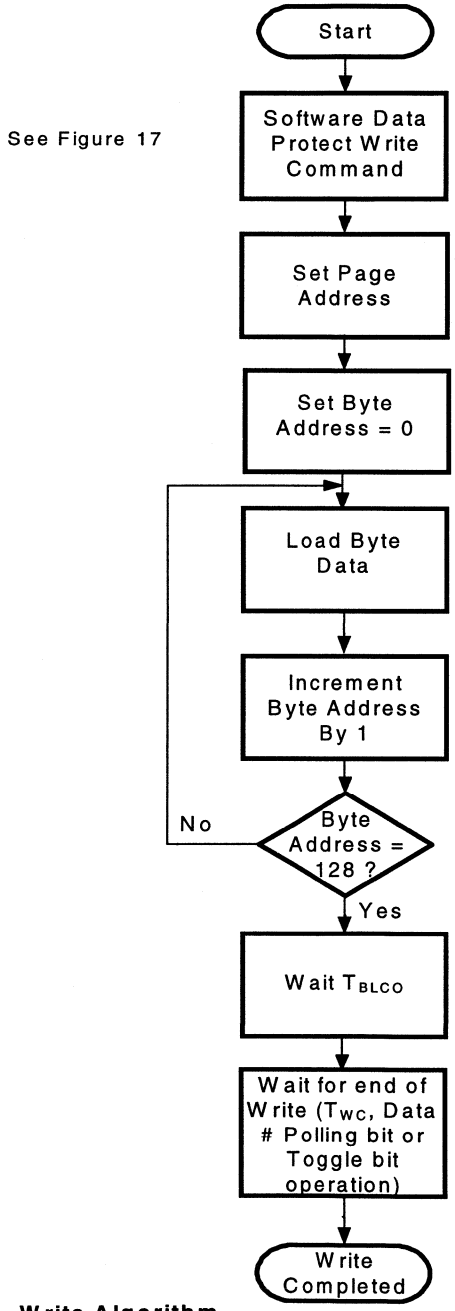


Figure 15: Write Algorithm

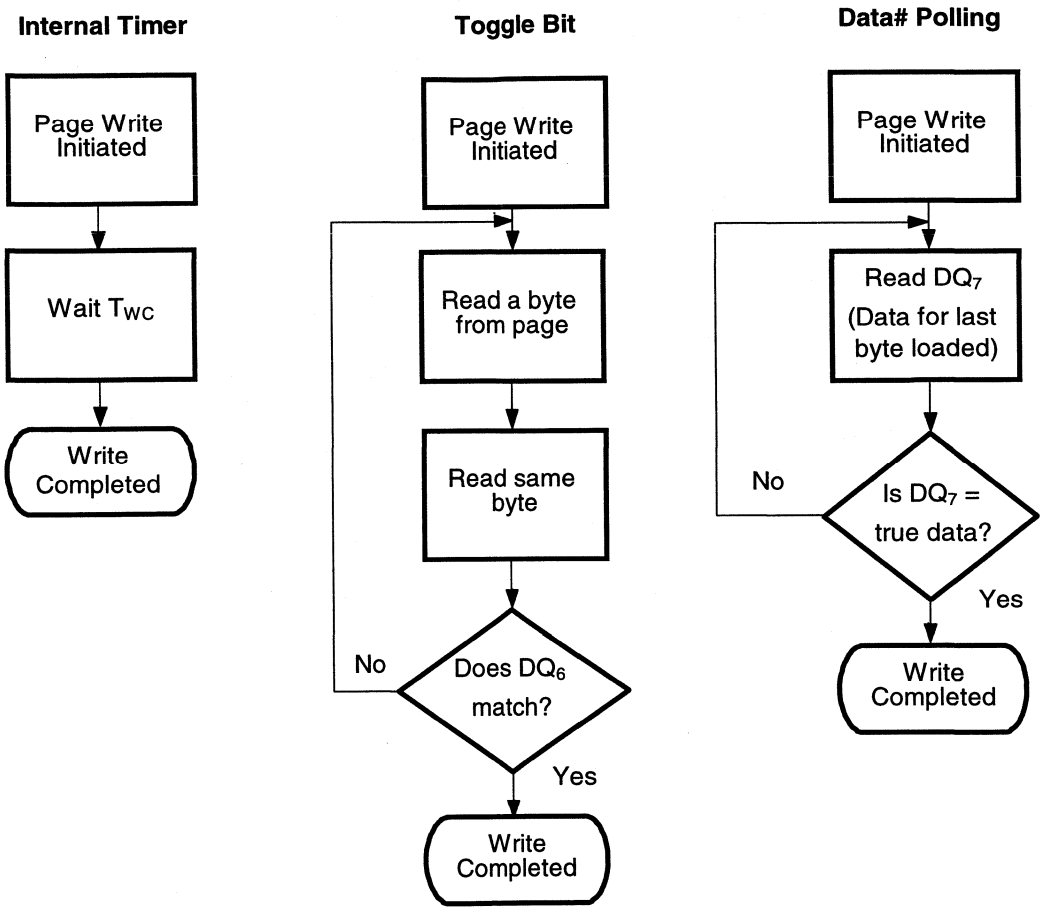


Figure 16: Wait Options

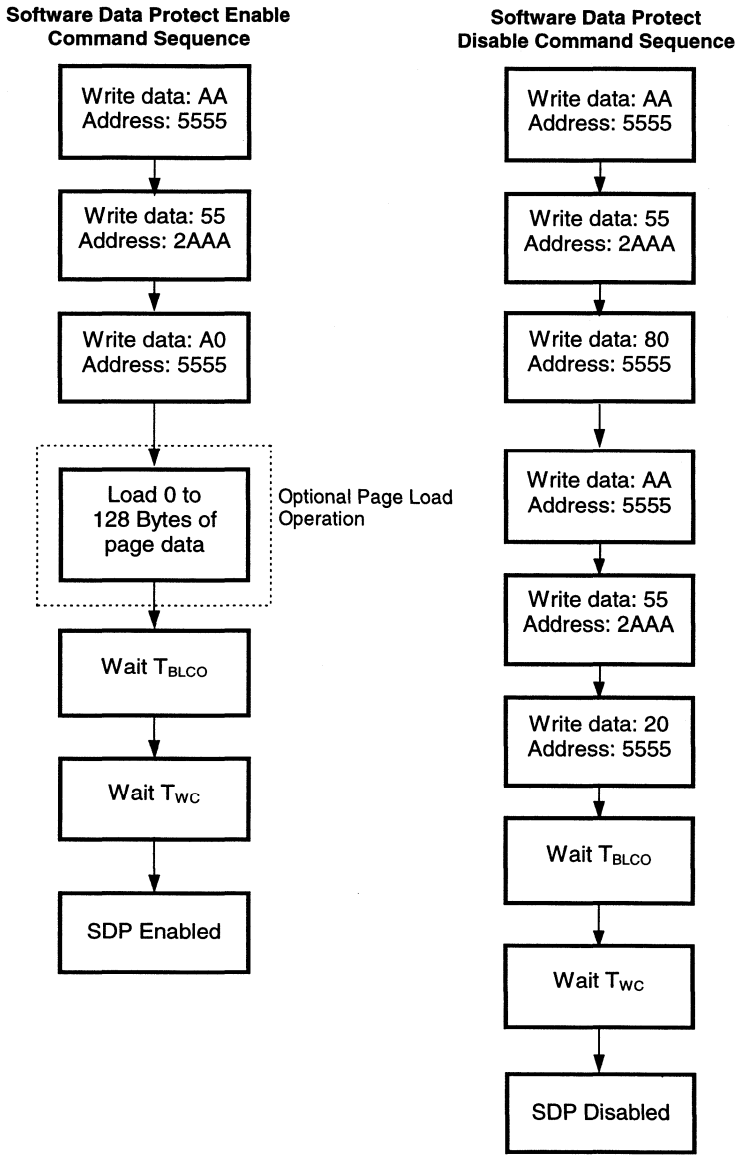


Figure 17: Software Data Protection Flowcharts

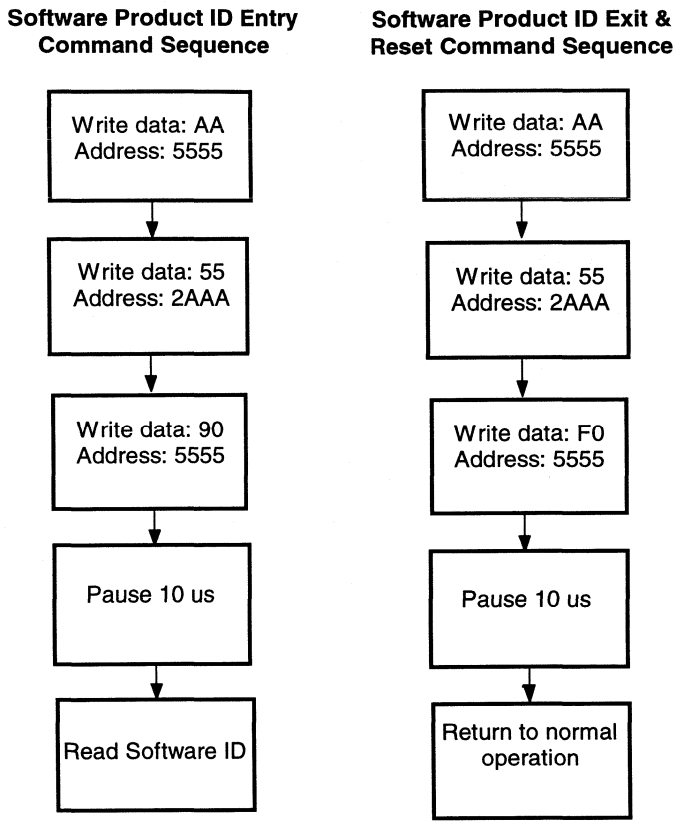


Figure 18: Software Product Command Flowcharts

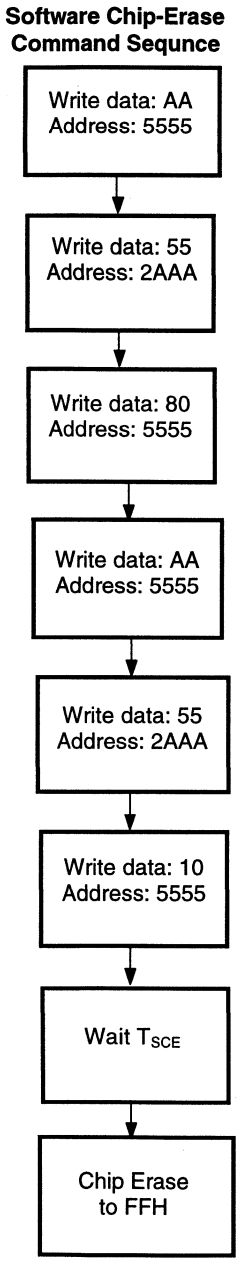
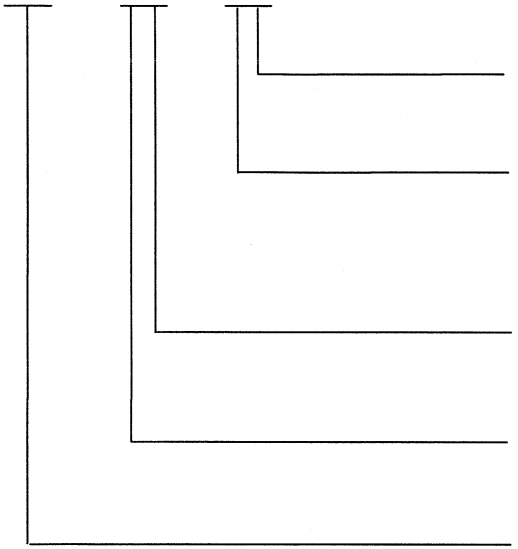


Figure 19: Software Chip Erase Command Codes

Product Ordering Information

Device		Speed		Suffix1		Suffix2
SST29VE512	-	XXX	-	XX	-	XX



Package Modifier
H = 32 leads
Numeric = Die modifier

Package Type
P = PDIP
N = PLCC
E = TSOP (die up)
U = Unencapsulated die

Operating Temperature
C = Commercial = 0° to 70°C
I = Industrial = -40° to 85°C

Minimum Endurance
3 = 1000 cycles
4 = 10,000 cycles

Read Access Speed
250 = 250 ns
200 = 200 ns

Valid combinations

SST29VE512-200-4C- EH	SST29VE512-200-4C- NH	SST29VE512-200-4C- PH
SST29VE512-250-4C- EH	SST29VE512-250-4C- NH	SST29VE512-250-4C- PH
SST29VE512-200-3C- EH	SST29VE512-200-3C- NH	SST29VE512-200-3C- PH
SST29VE512-250-3C- EH	SST29VE512-250-3C- NH	SST29VE512-250-3C- PH
SST29VE512-200-4I-EH	SST29VE512-200-4I-NH	
SST29VE512-250-4I-EH	SST29VE512-250-4I-NH	SST29VE512-250-4I-U1
SST29VE512-200-3I-EH	SST29VE512-200-3I-NH	
SST29VE512-250-3I-EH	SST29VE512-250-3I-NH	SST29VE512-250-3I-U1

Example: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Data Sheet

SST 29EE010
5.0V-only 1 Megabit
Page Mode EEPROM

July 1996

SST 29EE010
5.0V-only 1 Megabit
Page Mode EEPROM

Features:

Single 5.0-Volt Read and Write Operations
CMOS SuperFlash EEPROM Technology
- Endurance: 100,000 Cycles (typical)
- Greater than 100 years Data Retention

Low Power Consumption:
- Active Current: 20 mA (typical)
- Standby Current: 10 µA (typical)

Fast Page-Write Operation
- 128 Bytes per Page, 1024 Pages
- Page-Write Cycle: 5 ms (typical)
- Complete Memory Rewrite: 5 sec (typical)
- Effective Byte-write Cycle Time: 39 µs (typical)

Fast Access Time: 90, 120, and 150 ns
Latched Address and Data
Automatic Write Timing with Internal V_{pp} Generation
End of Write Detection
- Toggle Bit
- Data# Polling

Hardware and Software Data Protection
TTL I/O Compatibility
JEDEC Standard Byte-wide EEPROM Pinouts
Packages Available
- 32-Pin TSOP
- 32-Lead PLCC
- 32 Pin Plastic DIP

Product Description

The 29EE010 is a 128K x 8 CMOS page mode EEPROM manufactured with SST's proprietary, high performance CMOS SuperFlash technology. The split gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The 29EE010 writes with a 5.0-volt-only power supply. Internal erase/program is transparent to the user. The 29EE010 conforms to JEDEC standard pinouts for byte-wide memories.

Featuring high performance page write, the 29EE010 provides a typical byte-write time of 39 µsec. The entire memory, i.e., 128K bytes, can be written page by page in as little as 5 seconds, when using interface features such as Toggle Bit or Data# Polling to indicate the completion of a write cycle. To protect against inadvertent write, the 29EE010 has on-chip hardware and software data protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, the 29EE010 is offered with a guaranteed page-write endurance of 10^4 or 10^3 cycles. Data retention is rated at greater than 100 years.

The 29EE010 is suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, the 29EE010 significantly improves performance and reliability, while lowering power consumption, when compared with floppy disk or EPROM approaches. The 29EE010 improves flexibility while lowering the cost for program, data, and configuration storage applications.

To meet high density, surface mount requirements, the 29EE010 is offered in 32-pin TSOP and 32-lead PLCC packages. A 600-mil, 32-pin PDIP package is also available. See Figures 2A and 2B for pinouts.

Device Operation

The SST page mode EEPROM offers in-circuit electrical write capability. The 29EE010 does not require separate erase and program operations. The internally timed write cycle executes both erase and program transparently to the user. The 29EE010 has industry standard optional Software Data Protection, which SST recommends always to be enabled. The 29EE010 is compatible with industry standard EEPROM pinouts and functionality.

Read

The read operation of the 29EE010 is controlled by CE# and OE#, both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the read cycle timing diagram for further details (Figure 3).

Write

The write operation consists of three steps. The first step is the optional three byte load sequence for Software Data Protection. This is an optional first step in the write operation, but highly recommended to ensure proper data integrity. Step 2 is the byte-load cycle to a page buffer of the 29EE010. Step 3 is an internally controlled write cycle for writing the data loaded in the page buffer into the memory array for nonvolatile storage. During the byte-load cycle, the addresses are latched by the falling edge of either CE# or WE#, whichever occurs last. The data is latched by the rising edge of either CE# or WE#, whichever occurs first. The internal write cycle is initiated by a timer after the rising edge of WE# or CE#, whichever occurs first. The write cycle, once initiated, will continue to completion, typically within 5 ms. See Figures 4 and 5 for WE# and CE# controlled page write cycle timing diagrams and Figures 15 and 17 for flowcharts.

The write operation has three functional cycles: the optional Software Data Protection load sequence, the page load cycle, and the internal write cycle. The Software Data Protection consists of a specific three byte load sequence that will leave the 29EE010 protected at the end of the page write. The page load cycle consists of loading 1 to 128 bytes of data into the page buffer. The internal write cycle consists of the T_{BLCO} time-out and the write timer operation. During the write operation, the only valid reads are Data# Polling and Toggle Bit.

The page-write operation allows the loading of up to 128 bytes of data into the page buffer of the 29EE010 before the initiation of the internal write cycle. During the internal write cycle, all the data in the page buffer is written simultaneously into the memory array. Hence, the page-write feature of 29EE010 allows the entire memory to be written in as little as 5 seconds. During the internal write cycle, the host is free to perform additional tasks, such as to fetch data from other locations in the system to set up the write to the next page. In each page-write operation, all the bytes that are loaded into the page buffer must have the same page address, i.e. A_7 through A_{16}. Any byte not loaded with user data will be written to FF.

See Figures 4, 5, and 8 for the page-write cycle timing diagrams. If after the initial byte-load cycle, the host loads a second byte into the page buffer within a byte-load cycle time (T_{BLC}) of 100 µs, the 29EE010 will stay in the page load cycle. Additional bytes are then loaded consecutively. The page load cycle will be terminated if no additional byte is loaded into the page buffer within 200 µs (T_{BLCO}) from the last byte-load cycle, i.e., no subsequent WE# or CE# high-to-low transition after the last rising edge of WE# or CE#. Data in the page buffer can be changed by a subsequent byte-load cycle. The page load period can continue indefinitely, as long as the host continues to load the device within the byte-load cycle time of 100 µs. The page to be loaded is determined by the page address of the last byte loaded.

Software Chip-Erase

The 29EE010 provides a chip-erase operation, which allows the user to simultaneously clear the entire memory array to the "1" state. This is useful when the entire device must be quickly erased.

The Software Chip-Erase operation is initiated by using a specific six byte-load sequence. After the load sequence, the device enters into an internally timed cycle similar to the write cycle. During the erase operation, the only valid read is Toggle Bit. See Table 4 for the load sequence, Figure 10 for timing diagram, and Figure 19 for the flowchart.

Write Operation Status Detection

The 29EE010 provides two software means to detect the completion of a write cycle, in order to optimize the system write cycle time. The software detection includes two status bits: Data# Polling (DQ_7) and Toggle Bit (DQ_6). The end of write detection mode is enabled after the rising WE# or CE# whichever occurs first, which initiates the internal write cycle.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the

accessed location an additional two (2) times. If both reads are valid, then the device has completed the write cycle, otherwise the rejection is valid.

Data# Polling (DQ_7)

When the 29EE010 is in the internal write cycle, any attempt to read DQ_7 of the last byte loaded during the byte-load cycle will receive the complement of the true data. Once the write cycle is completed, DQ_7 will show true data. The device is then ready for the next operation. See Figure 6 for Data# Polling timing diagram and Figure 16 for a flowchart.

Toggle Bit (DQ_6)

During the internal write cycle, any consecutive attempts to read DQ_6 will produce alternating 0's and 1's, i.e. toggling between 0 and 1. When the write cycle is completed, the toggling will stop. The device is then ready for the next operation. See Figure 7 for Toggle Bit timing diagram and Figure 16 for a flowchart. The initial read of the Toggle Bit will be a "1".

Data Protection

The 29EE010 provides both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a write cycle.

V_{CC} Power Up/Down Detection: The write operation is inhibited when V_{CC} is less than 2.5V.

Write Inhibit Mode: Forcing OE# low, CE# high, or WE# high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down.

Software Data Protection (SDP)

The 29EE010 provides the JEDEC approved optional software data protection scheme for all data alteration operations, i.e., write and chip erase. With this scheme, any write operation requires the inclusion of a series of three byte-load operations to precede the data loading operation. The three byte-load sequence is used to initiate the write cycle, providing optimal protection from inadvertent write operations, e.g., during the system power-up or power-down. The 29EE010 is shipped with the software data protection disabled.

The software protection scheme can be enabled by applying a three-byte sequence to the device, during a page-load cycle (Figure 8). The device will then be automatically set into the data protect mode. Any subsequent write operation will require the preceding three-byte sequence. See Table 4 for the specific software command codes and Figure 8 for the timing diagram. To set the device into the unprotected mode, a six-byte sequence is required. See Table 4 for the specific codes and Figure 9 for the timing diagram. If a write is attempted while SDP is enabled the device will be in a non-accessible state for ~ 300 µs. SST recommends Software Data Protection always be enabled. See Figure 17 for flowcharts.

The 29EE010 Software Data Protection is a global command, protecting (or unprotecting) all pages in the entire memory array once enabled (or disabled). Therefore using SDP for a single page write will enable SDP for the entire array. Single pages by themselves cannot be SDP enabled or disabled.

Single power supply reprogrammable nonvolatile memories may be unintentionally altered. SST strongly recommends that Software Data Protection (SDP) always be enabled. The 29EE010 should be programmed using the SDP command sequence. SST recommends the SDP Disable Command Sequence not be issued to the device prior to writing.

Product Identification

The product identification mode identifies the device as the 29EE010 and manufacturer as SST. This mode may be accessed by hardware or software operations. The hardware operation is typically used by a programmer to identify the correct algorithm for the 29EE010. Users may wish to use the software product identification operation to identify the part (i.e. using the device code) when using multiple manufacturers in the same socket. For details, see Table 3 for hardware operation or Table 4 for software operation, Figure 11 for the software ID entry and read timing diagram and Figure 18 for the ID entry command sequence flowchart. The manufacturer and device codes are the same for both operations.

Table 1: Product Identification Table

	Byte	Data
Manufacturers Code	0000 H	BF H
Device Code	0001 H	07 H

Product Identification Mode Exit

In order to return to the standard read mode, the Software Product Identification mode must be exited. Exiting is accomplished by issuing the Software ID Exit (reset) operation, which returns the device to the read operation. The reset operation may also be used to reset the device to the read mode after an inadvertent transient condition that apparently causes the device to behave abnormally, e.g. not read correctly. See Table 4 for software command codes, Figure 12 for timing wavefrom and Figure 18 for a flowchart.

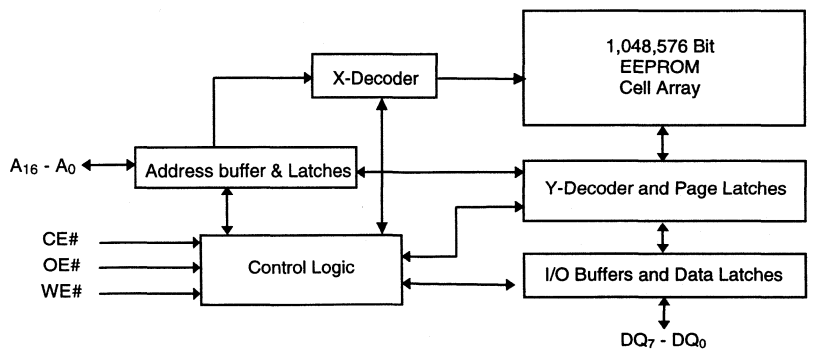


Figure 1: Functional Block Diagram of SST 29EE010

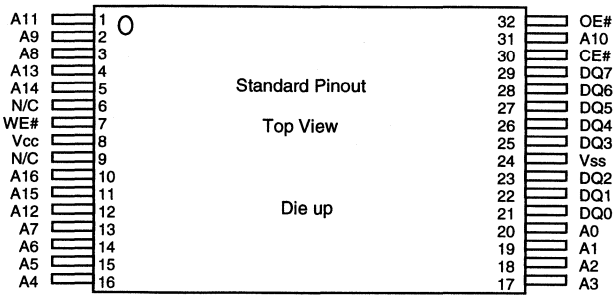
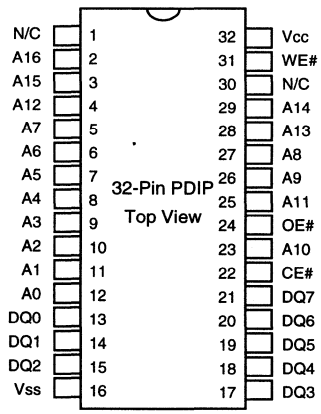


Figure 2A: Pin Assignments for 32-pin TSOP Packages



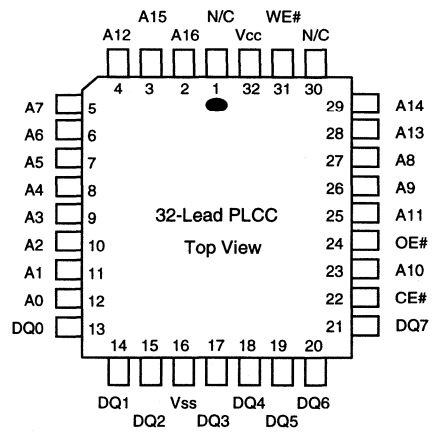


Figure 2B: Pin Assignments for 32-pin Plastic DIPs and 32-lead PLCCs

Table 2: Pin Description

Symbol	Pin Name	Functions
A_{16}-A_7	Row Address Inputs	To provide memory addresses. Row addresses define a page for a write cycle.
A_6-A_0	Column Address Inputs	Column Addresses are toggled to load page data.
DQ_7-DQ_0	Data Input/output	To output data during read cycles and receive input data during write cycles. Data is internally latched during a write cycle. The outputs are in tri-state when OE# or CE# is high.
CE#	Chip Enable	To activate the device when CE# is low.
OE#	Output Enable	To gate the data output buffers.
WE#	Write Enable	To control the write operations
Vcc	Power Supply	To provide 5-volt supply (± 10%)
Vss	Ground	
NC	No Connection	Unconnected pins.

Table 3: Operation Modes Selection

Mode	CE#	OE#	WE#	DQ	Address
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	A_{IN}
Page Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}
Standby	V_{IH}	X	X	High Z	X
Write Inhibit	X	V_{IL}	X	High Z/ D_{OUT}	X
Write Inhibit	X	X	V_{IH}	High Z/ D_{OUT}	X
Software Chip Erase	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}, See Table 4
Product Identification					
Hardware Mode	V_{IL}	V_{IL}	V_{IH}	Manufacturer Code (BF) Device Code (07)	A_{16} - A_1 = V_{IL}, A_9 = V_H, A_0 = V_{IL} A_{16} - A_1 = V_{IL}, A_9 = V_H, A_0= V_{IH}
Software Mode	V_{IL}	V_{IH}	V_{IL}		See Table 4
SDP Enable Mode	V_{IL}	V_{IH}	V_{IL}		See Table 4
SDP Disable Mode	V_{IL}	V_{IH}	V_{IL}		See Table 4

Table 4: Software Command Codes

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data
Software Data Protect Enable & Page Write	5555H	AAH	2AAAH	55H	5555H	A0H	Addr[2]	Data				
Software Data Protect Disable	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	20H
Software Chip Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	60H
Software ID Exit	5555H	AAH	2AAAH	55H	5555H	F0H						

Notes: (1) Address format A_{14}-A_0 (Hex), Addresses A_{15} and A_{16} are a "Don't Care".

(2) Page Write consists of loading up to 128 bytes (A_6 - A_0).

Notes for Software Product ID Command Code:

1. With A_{14} -A_1 =0; SST Manufacturer Code = BFH, is read with A_0 = 0,
   29EE010 Device Code = 07H, is read with A_0 = 1.
2. The device does not remain in Software Product ID Mode if powered down.

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential ..... -0.5V to V_{CC}+ 0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential ..... -1.0V to V_{CC}+ 1.0V
Voltage on A_9 Pin to Ground Potential ..... -0.5V to 14.0V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Through Hole Lead Soldering Temperature (10 Seconds) ..... 300°C
Surface Mount Lead Soldering Temperature (3 Seconds) ..... 240°C
Output Short Circuit Current[1] ..... 100 mA

Note: [1] Outputs shorted for no more than one second. No more than one output shorted at a time.

Operating Range

Range	Ambient Temp	V_{CC}
Commercial	0 °C to +70 °C	5V±10%
Industrial	-40 °C to +85 °C	5V±10%

AC Conditions of Test

Input Rise/Fall Time.....10 ns
Output Load.....1 TTL Gate and C_L = 100 pF
See Figures 13 and 14

Table 5: DC Operating Characteristics

Symbol	Parameter	Limits Min	Limits Max	Units	Test Conditions
I_{CC}	Power Supply Current				CE#=OE#=V_{IL},WE#=V_{IH}, all I/Os open,
	Read		30	mA	Address input = V_{IL}/V_{IH}, at f=1/T_{RC} Min., V_{CC}=V_{CC} Max
	Write		50	mA	CE#=WE#=V_{IL}, OE#=V_{IH}, V_{CC}=V_{CC} Max.
I_{SB1}	Standby V_{CC} Current (TTL input)		3	mA	CE#=OE#=WE#=V_{IH}, V_{CC}=V_{CC} Max.
I_{SB2}	Standby V_{CC} Current (CMOS input)		50	µA	CE#=OE#=WE#=V_{CC} -0.3V. V_{CC} = V_{CC} Max.
I_{LI}	Input Leakage Current		1	µA	V_{IN} =GND to V_{CC}, V_{CC} = V_{CC} Max.
I_{LO}	Output Leakage Current		10	µA	V_{OUT} =GND to V_{CC}, V_{CC} = V_{CC} Max.
V_{IL}	Input Low Voltage		0.8	V	V_{CC} = V_{CC} Max.
V_{IH}	Input High Voltage	2.0		V	V_{CC} = V_{CC} Max.
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.1 mA, V_{CC} = V_{CC} Min.
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400µA, V_{CC} = V_{CC} Min.
V_H	Supervoltage for A_9	11.6	12.4	V	CE# = OE# =V_{IL}, WE# = V_{IH}
I_H	Supervoltage Current for A_9		100	µA	CE# = OE# = V_{IL}, WE# = V_{IH}, A_9 = V_H Max.

Table 6: Power-up Timings

Symbol	Parameter	Maximum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$[1]	Power-up to Write Operation	5	ms

Table 7: Capacitance (Ta = 25 °C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0v	6 pF

Note: [1]This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 8: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}	Endurance	1,000 & 10,000[2]	Cycles	MIL-STD-883, Method 1033
T_{DR}[1]	Data Retention	100	Years	MIL-STD-883, Method 1008
V_{ZAP_HBM}[1]	ESD Susceptibility Human Body Model	1000	Volts	JEDEC Standard A114
V_{ZAP_MM}[1]	ESD Susceptibility Machine Model	200	Volts	JEDEC
I_{LTH}[1]	Latch Up	100	mA	JEDEC Standard 17

Note: [1]This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

[2]See Ordering Information for desired type.

AC Characteristics

Table 9: Read Cycle Timing Parameters

Symbol	Parameter	29EE010-90		29EE010-120		29EE010-150		Units
		Min	Max	Min	Max	Min	Max	
T_{RC}	Read Cycle time	90		120		150		ns
T_{CE}	Chip Enable Access Time		90		120		150	ns
T_{AA}	Address Access Time		90		120		150	ns
T_{OE}	Output Enable Access Time		40		50		60	ns
T_{CLZ}(1)	CE# Low to Active Output	0		0		0		ns
T_{OLZ}(1)	OE# Low to Active Output	0		0		0		ns
T_{CHZ}(1)	CE# High to High-Z Output		30		30		30	ns
T_{OHZ}(1)	OE# High to High-Z Output		30		30		30	ns
T_{OH}(1)	Output Hold from Address Change	0		0		0		ns

Table 10: Page-Write Cycle Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{WC}	Write Cycle (erase and program)		10	ms
T_{AS}	Address Setup Time	0		ns
T_{AH}	Address Hold Time	50		ns
T_{CS}	WE# and CE# Setup Time	0		ns
T_{CH}	WE# and CE# Hold Time	0		ns
T_{OES}	OE# High Setup Time	0		ns
T_{OEH}	OE# High Hold Time	0		ns
T_{CP}	CE# Pulse Width	70		ns
T_{WP}	WE# Pulse Width	70		ns
T_{DS}	Data Setup Time	35		ns
T_{DH}	Data Hold Time	0		ns
T_{BLC}(1)	Byte Load Cycle Time	0.05	100	µs
T_{BLCO}(1)	Byte Load Cycle Time	200		µs
T_{IDA}	Software ID Access and Exit Time		10	µs
T_{SCE}	Software Chip Erase		20	ms

Note: (1)This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.

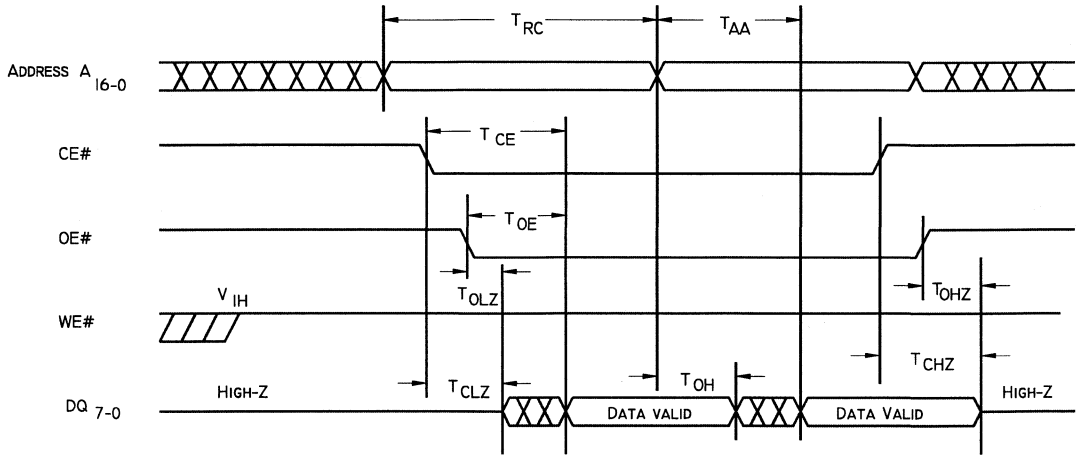


Figure 3: Read Cycle Timing Diagram

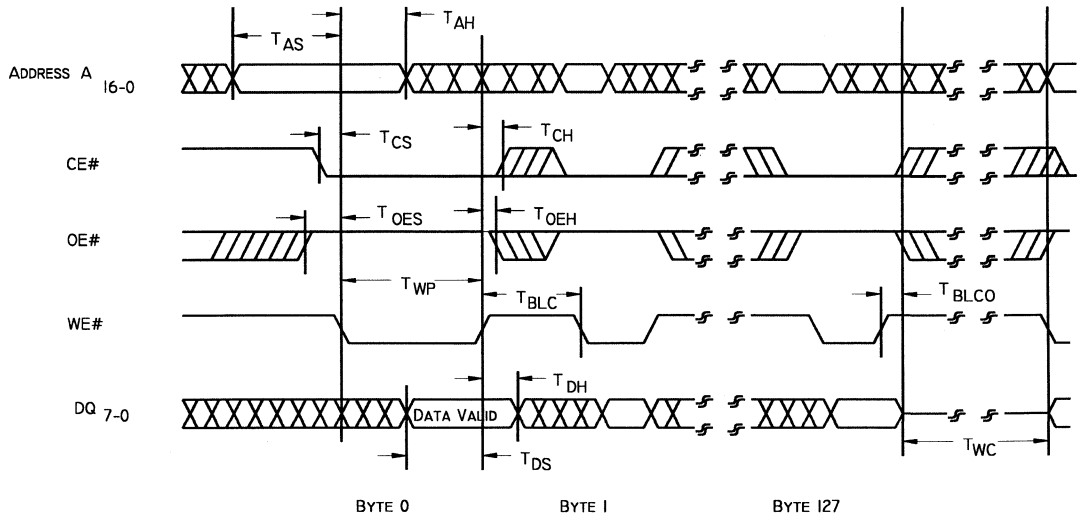


Figure 4: WE# Controlled Page Write Cycle Timing Diagram

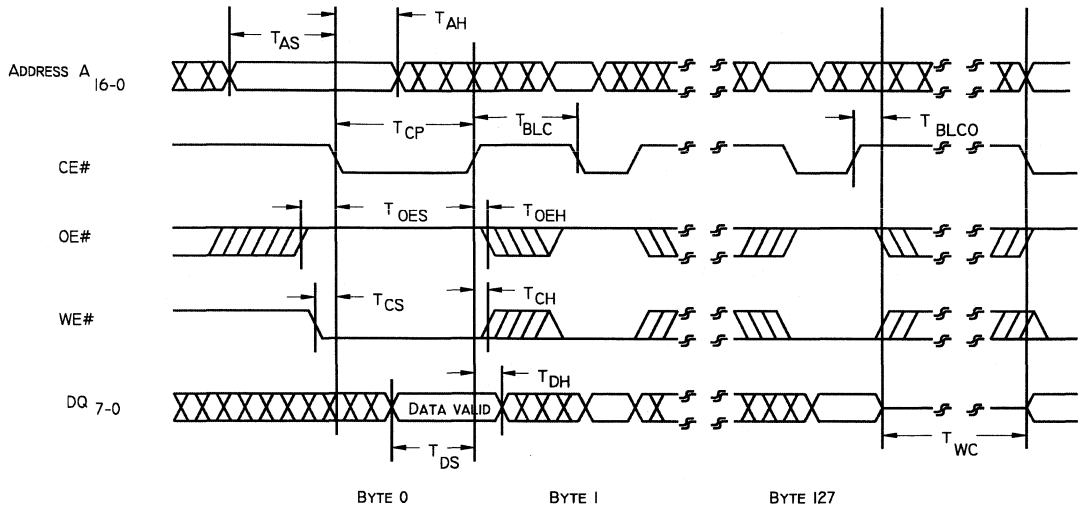


Figure 5: CE# Controlled Page Write Cycle Timing Diagram

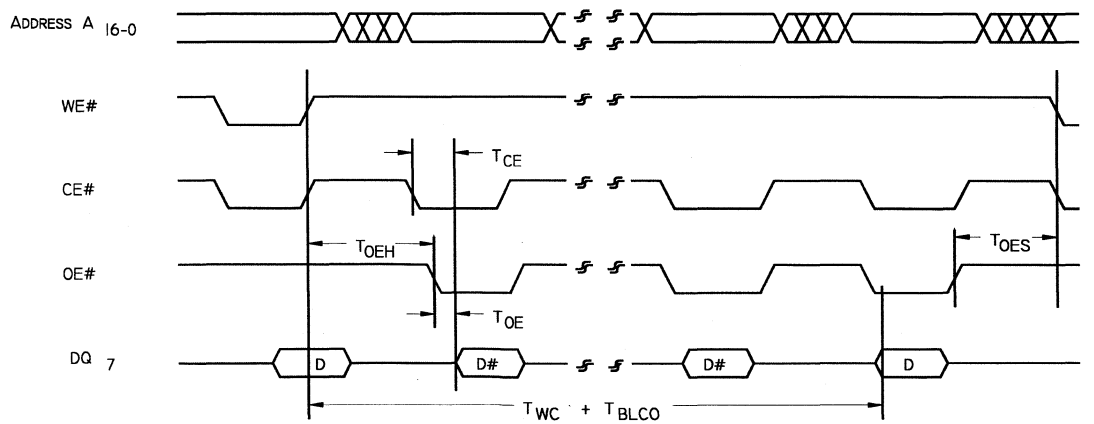


Figure 6: Data# Polling Timing Diagram

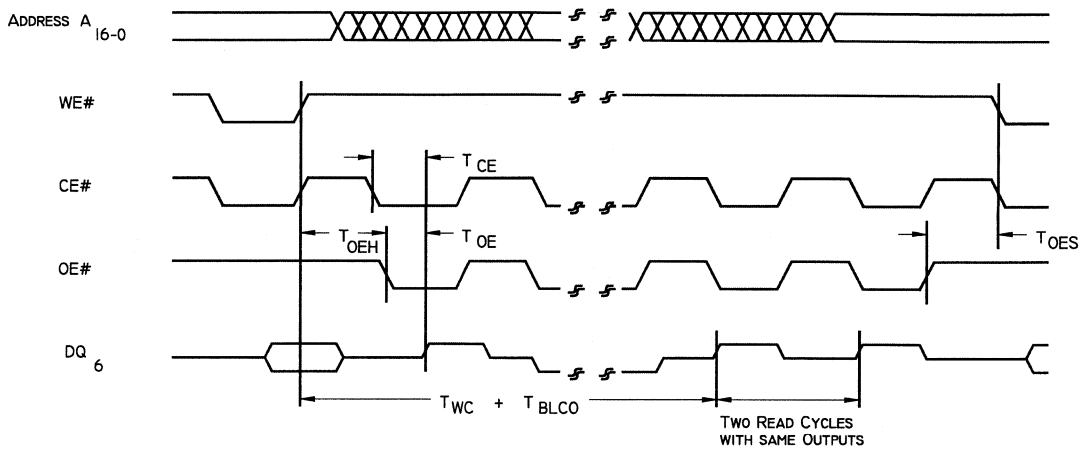
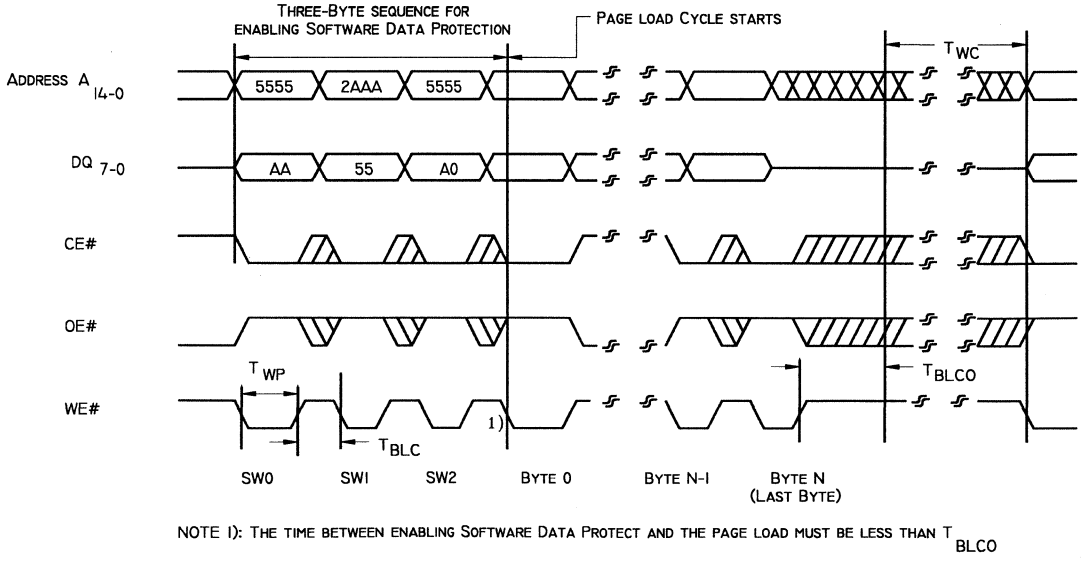


Figure 7: Toggle Bit Timing Diagram



NOTE 1): THE TIME BETWEEN ENABLING SOFTWARE DATA PROTECT AND THE PAGE LOAD MUST BE LESS THAN T_{BLCO}

Figure 8: Software Data Protection Page Write Timing Diagram

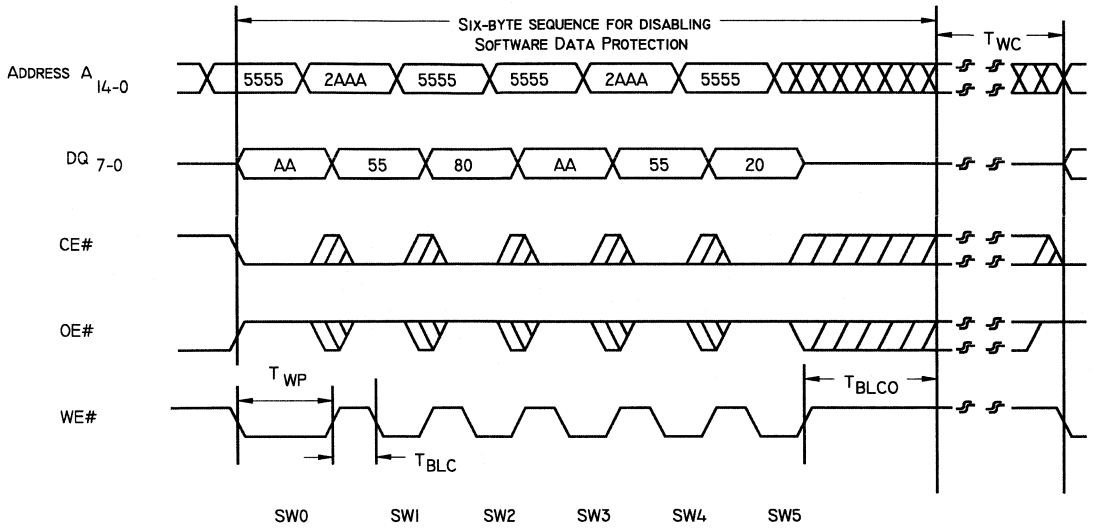


Figure 9: Software Data Protect Disable Timing Diagram

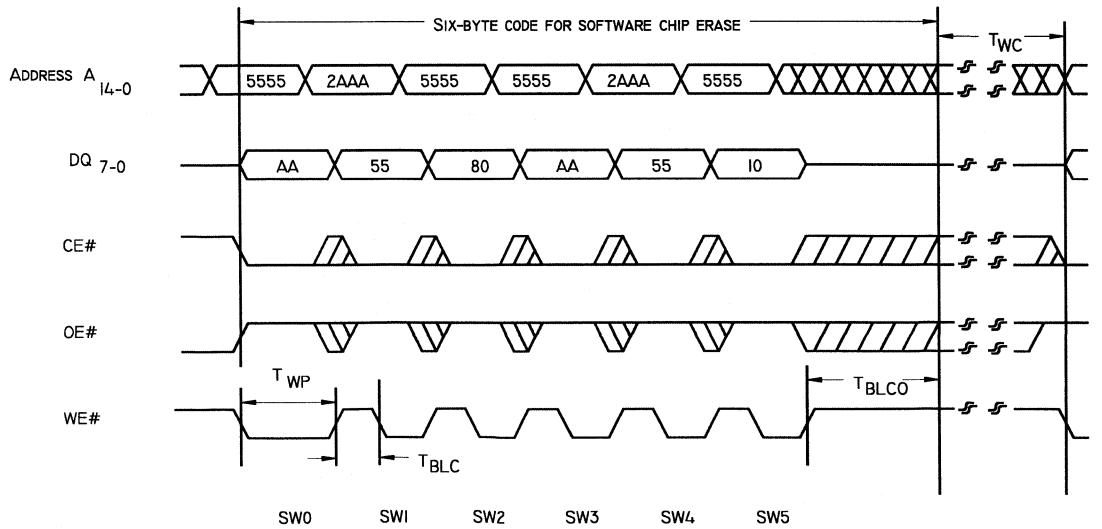


Figure 10: Software Chip Erase Timing Diagram

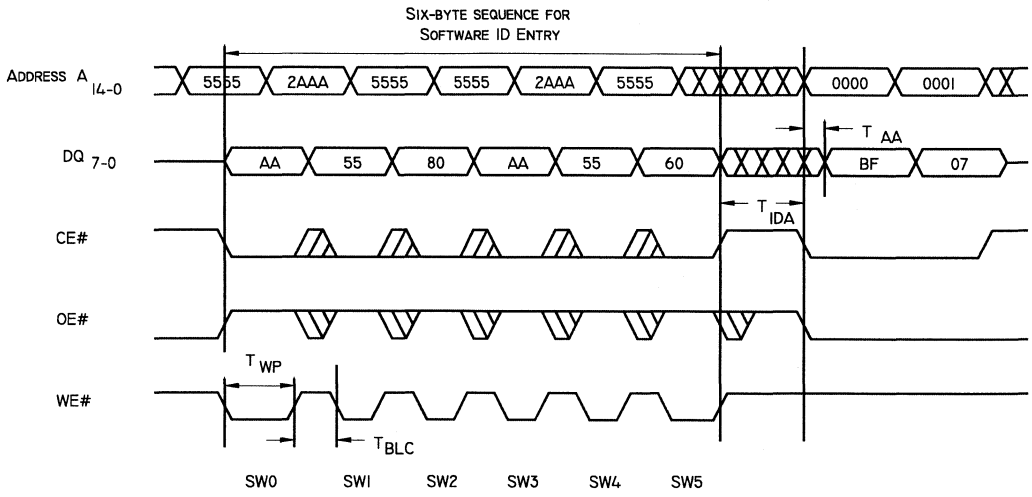


Figure 11: Software ID Entry and Read

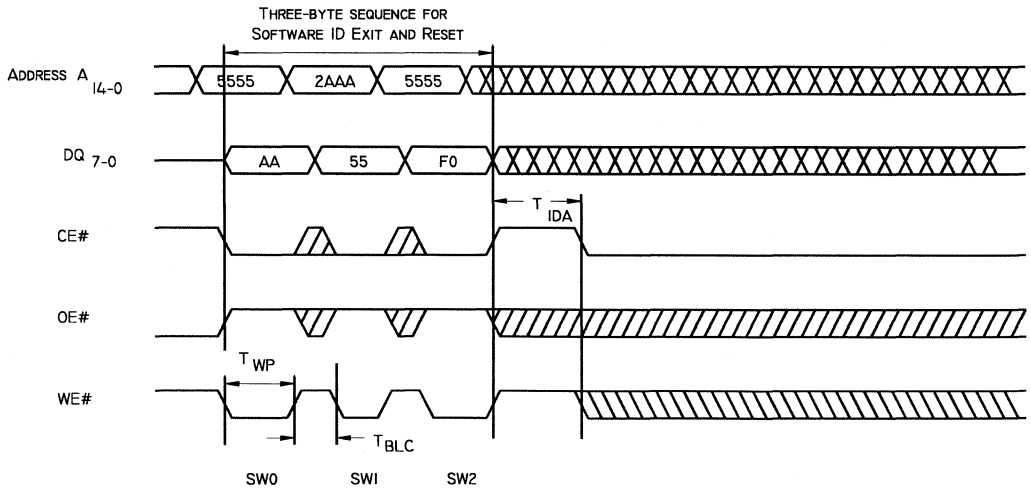
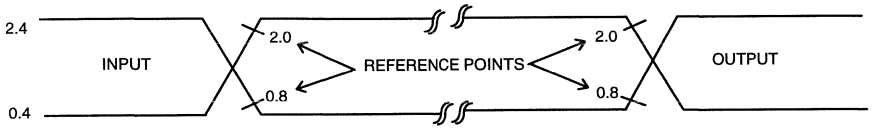


Figure 12: Software ID Exit and Reset



AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a logic "1" and V_{OL} (0.4 V_{TTL}) for a logic "0". Measurement reference points for inputs and outputs are V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Inputs rise and fall times (10% ↔ 90%) are <10 ns.

Figure 13: AC Input/Output Reference Waveforms

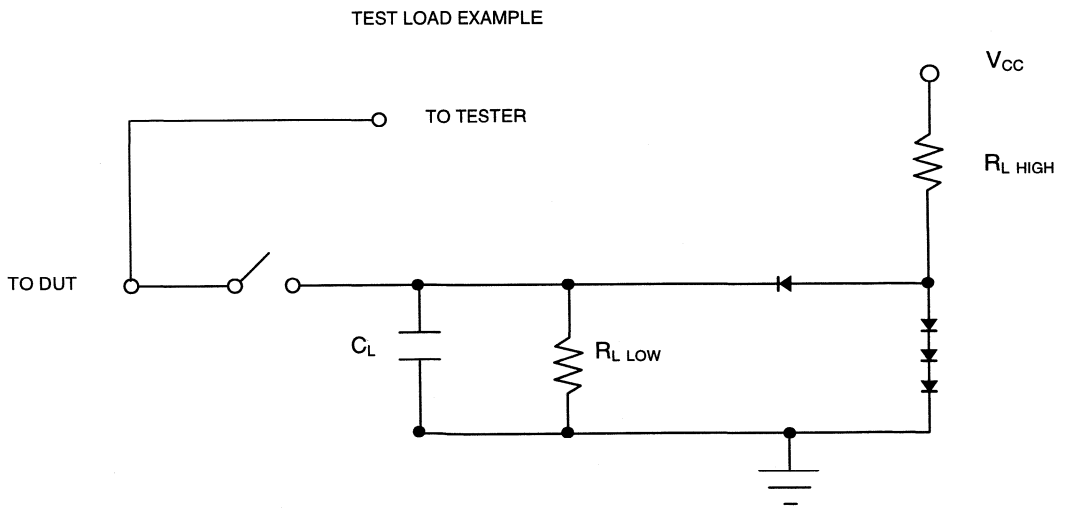


Figure 14: Test Load Example

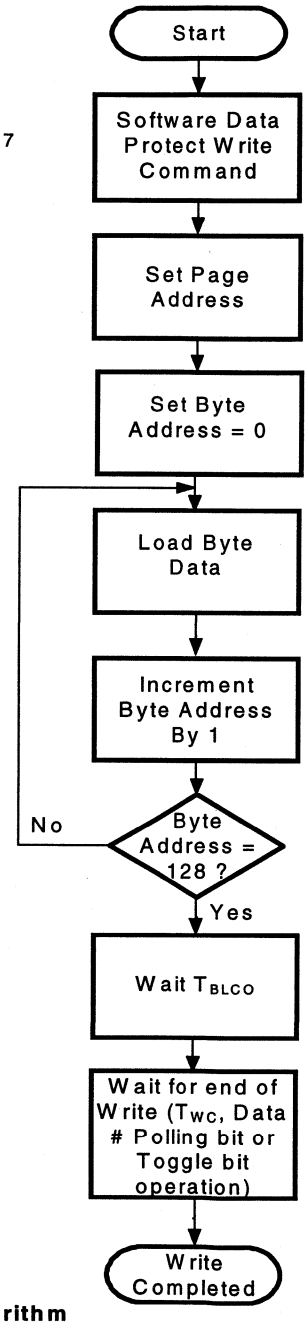


Figure 15: Write Algorithm

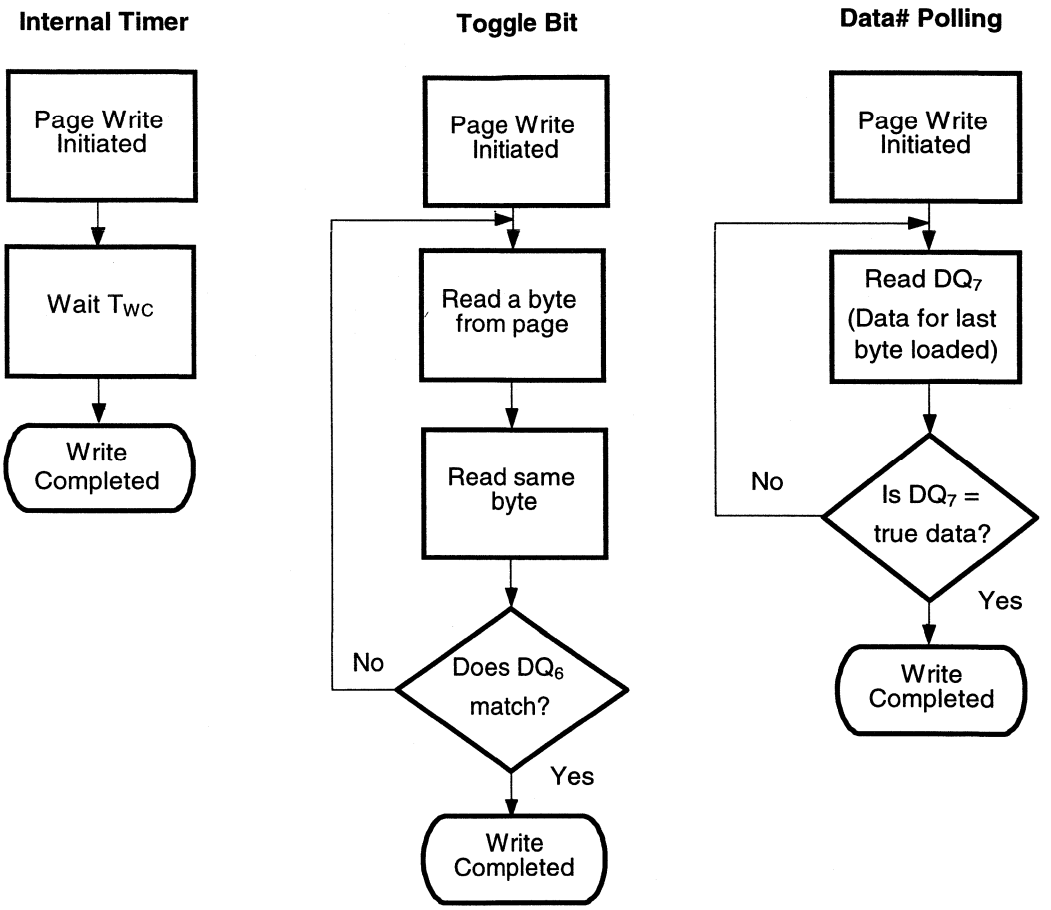


Figure 16: Wait Options

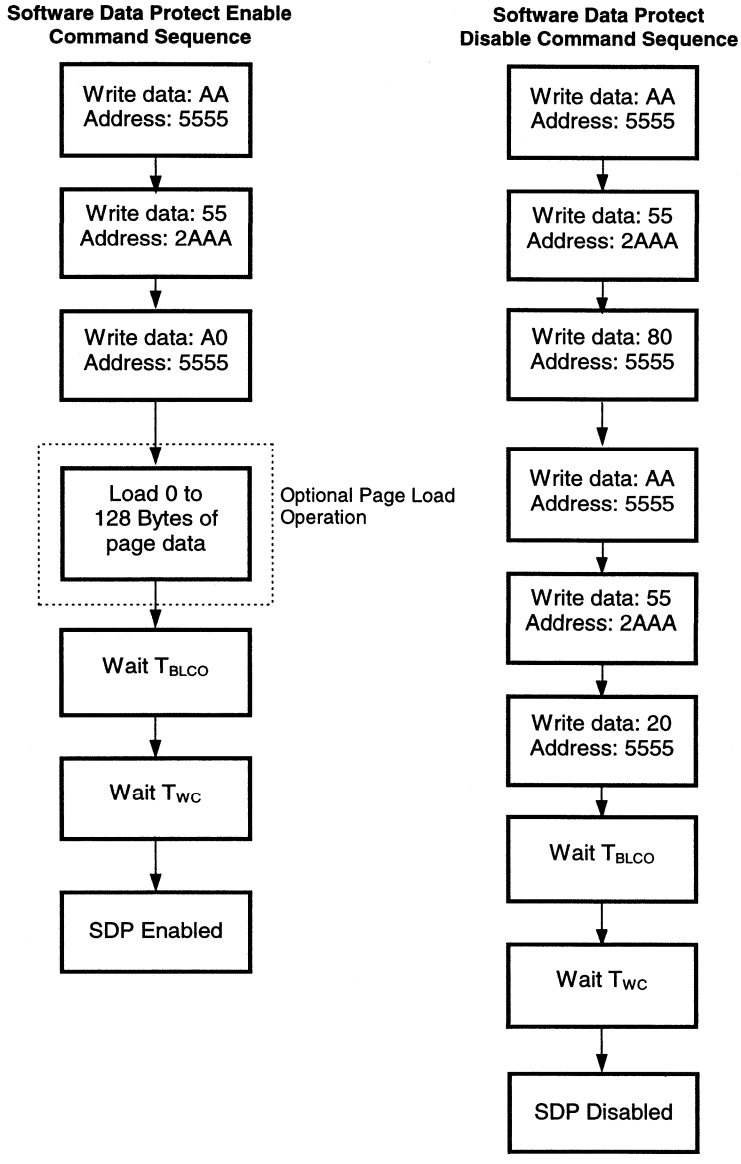


Figure 17: Software Data Protection Flowcharts

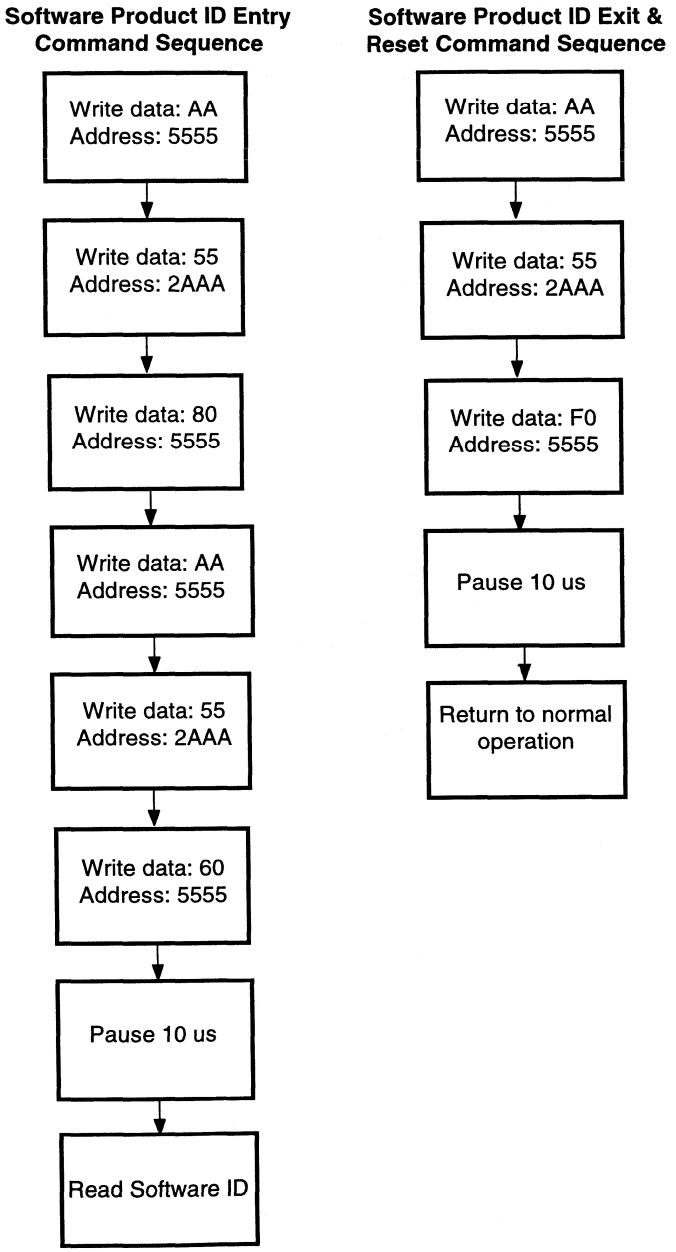


Figure 18: Software Product Command Flowcharts

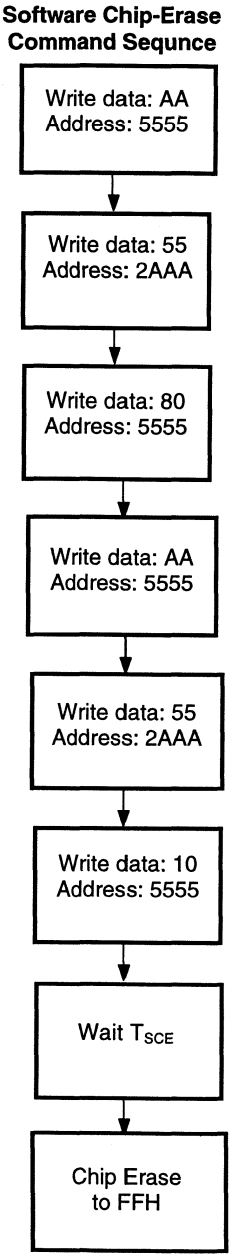
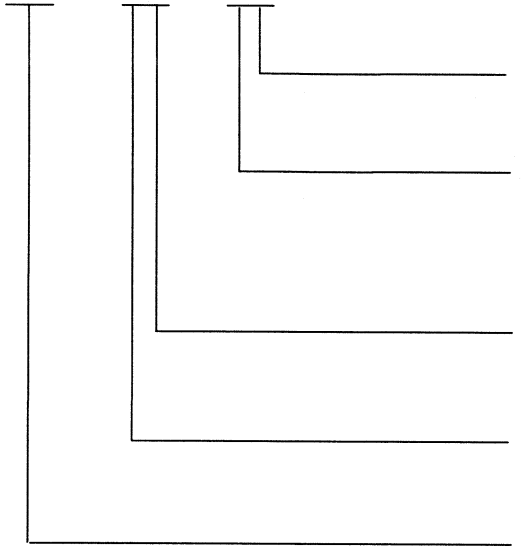


Figure 19: Software Chip Erase Command Codes

Product Ordering Information

Device		Speed		Suffix1		Suffix2
SST29EE010	-	XXX	-	XX	-	XX



Package Modifier
H = 32 leads
Numeric = Die modifier

Package Type
P = PDIP
N = PLCC
E = TSOP (die up)
U = Unencapsulated die

Operating Temperature
C = Commercial = 0° to 70°C
I = Industrial = -40° to 85°C

Minimum Endurance
3 = 1000 cycles
4 = 10,000 cycles

Read Access Speed
150 = 150 ns
120 = 120 ns
90 = 90 ns

Valid combinations

SST29EE010- 90-4C- EH	SST29EE010- 90-4C- NH	SST29EE010- 90-4C- PH
SST29EE010-120-4C- EH	SST29EE010-120-4C- NH	SST29EE010-120-4C- PH
SST29EE010-150-4C- EH	SST29EE010-150-4C- NH	SST29EE010-150-4C- PH
SST29EE010- 90-3C- EH	SST29EE010- 90-3C- NH	SST29EE010- 90-3C- PH
SST29EE010-120-3C- EH	SST29EE010-120-3C- NH	SST29EE010-120-3C- PH
SST29EE010-150-3C- EH	SST29EE010-150-3C- NH	SST29EE010-150-3C- PH
SST29EE010- 90-4I-EH	SST29EE010- 90-4I-NH	
SST29EE010-120-4I-EH	SST29EE010-120-4I-NH	SST29EE010-150-4C-U1
SST29EE010-150-4I-EH	SST29EE010-150-4I-NH	
SST29EE010- 90-3I-EH	SST29EE010- 90-3I-NH	
SST29EE010-120-3I-EH	SST29EE010-120-3I-NH	SST29EE010-150-3C-U1
SST29EE010-150-3I-EH	SST29EE010-150-3I-NH	

Example: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Data Sheet

SST 29LE010
3.0V-only 1 Megabit
Page Mode EEPROM

July 1996

SST 29LE010
3.0V-only 1 Megabit
Page Mode EEPROM

Features:

Single 3.0-Volt Read and Write Operations
CMOS SuperFlash EEPROM Technology
- Endurance: 100,000 Cycles (typical)
- Greater than 100 years Data Retention

Low Power Consumption:
- Active Current: 10 mA (typical)
- Standby Current: 10 µA (typical)

Fast Page-Write Operation
- 128 Bytes per Page, 1024 Pages
- Page-Write Cycle: 5 ms (typical)
- Complete Memory Rewrite: 5 sec (typical)
- Effective Byte-write Cycle Time: 39 µs (typical)

Fast Access Time: 150 and 200 ns
Latched Address and Data
Automatic Write Timing with Internal V_{pp} Generation
End of Write Detection
- Toggle Bit
- Data# Polling

Hardware and Software Data Protection
TTL I/O Compatibility
JEDEC Standard Byte-wide EEPROM Pinouts
Packages Available
- 32-Pin TSOP
- 32-Lead PLCC
- 32 Pin Plastic DIP

Product Description

The 29LE010 is a 128K x 8 CMOS page mode EEPROM manufactured with SST's proprietary, high performance CMOS SuperFlash technology. The split gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The 29LE010 writes with a 3.0-volt-only power supply. (V_{CC}: 3.0V to 3.6V) Internal erase/program is transparent to the user. The 29LE010 conforms to JEDEC standard pinouts for byte-wide memories.

Featuring high performance page write, the 29LE010 provides a typical byte-write time of 39 µsec. The entire memory, i.e., 128K bytes, can be written page by page in as little as 5 seconds, when using interface features such as Toggle Bit or Data# Polling to indicate the completion of a write cycle. To protect against inadvertent write, the 29LE010 has on-chip hardware and software data protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, the 29LE010 is offered with a guaranteed page-write endurance of 10^4 or 10^3 cycles. Data retention is rated at greater than 100 years.

The 29LE010 is suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, the 29LE010 significantly improves performance and reliability, while lowering power consumption, when compared with 5 volt EEPROM or EPROM approaches. The 29LE010 improves flexibility while lowering the cost for program, data, and configuration storage applications.

To meet high density, surface mount requirements, the 29LE010 is offered in 32-pin TSOP and 32-lead PLCC packages. A 600-mil, 32-pin PDIP package is also available. See Figures 2A and 2B for pinouts.

Device Operation

The SST page mode EEPROM offers in-circuit electrical write capability. The 29LE010 does not require separate erase and program operations. The internally timed write cycle executes both erase and program transparently to the user. The 29LE010 has industry standard optional Software Data Protection, which SST recommends always to be enabled. The 29LE010 is compatible with industry standard EEPROM pinouts and functionality.

Read

The read operation of the 29LE010 is controlled by CE# and OE#, both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the read cycle timing diagram for further details (Figure 3).

Write

The write operation consists of three steps. The first step is the optional three byte load sequence for Software Data Protection. This is an optional first step in the write operation, but highly recommended to ensure proper data integrity. Step 2 is the byte-load cycle to a page buffer of the 29LE010. Step 3 is an internally controlled write cycle for writing the data loaded in the page buffer into the memory array for nonvolatile storage. During the byte-load cycle, the addresses are latched by the falling edge of either CE# or WE#, whichever occurs last. The data is latched by the rising edge of either CE# or WE#, whichever occurs first. The internal write cycle is initiated by a timer after the rising edge of WE# or CE#, whichever occurs first. The write cycle, once initiated, will continue to completion, typically within 5 ms. See Figures 4 and 5 for WE# and CE# controlled page write cycle timing diagrams and Figures 15 and 17 for flowcharts.

The write operation has three functional cycles: the optional Software Data Protection load sequence, the page load cycle, and the internal write cycle. The Software Data Protection consists of a specific three byte load sequence that will leave the 29LE010 protected at the end of the page write. The page load cycle consists of loading 1 to 128 bytes of data into the page buffer. The internal write cycle consists of the T_{BLCO} time-out and the write timer operation. During the write operation, the only valid reads are Data# Polling and Toggle Bit.

The page-write operation allows the loading of up to 128 bytes of data into the page buffer of the 29LE010 before the initiation of the internal write cycle. During the internal write cycle, all the data in the page buffer is written simultaneously into the memory array. Hence, the page-write feature of 29LE010 allows the entire memory to be written in as little as 5 seconds. During the internal write cycle, the host is free to perform additional tasks, such as to fetch data from other locations in the system to set up the write to the next page. In each page-write operation, all the bytes that are loaded into the page buffer must have the same page address, i.e., A_7 through A_{16}. Any byte not loaded with user data will be written to FF.

See Figures 4, 5, and 8 for the page-write cycle timing diagrams. If after the initial byte-load cycle, the host loads a second byte into the page buffer within a byte-load cycle time (T_{BLC}) of 100 µs, the 29LE010 will stay in the page load cycle. Additional bytes are then loaded consecutively. The page load cycle will be terminated if no additional byte is loaded into the page buffer within 200 µs (T_{BLCO}) from the last byte-load cycle, i.e., no subsequent WE# or CE# high-to-low transition after the last rising edge of WE# or CE#. Data in the page buffer can be changed by a subsequent byte-load cycle. The page load period can continue indefinitely, as long as the host continues to load the device within the byte-load cycle time of 100 µs. The page to be loaded is determined by the page address of the last byte loaded.

Software Chip-Erase

The 29LE010 provides a chip-erase operation, which allows the user to simultaneously clear the entire memory array to the "1" state. This is useful when the entire device must be quickly erased.

The Software Chip-Erase operation is initiated by using a specific six byte-load sequence. After the load sequence, the device enters into an internally timed cycle similar to the write cycle. During the erase operation, the only valid read is Toggle Bit. See Table 4 for the load sequence, Figure 10 for timing diagram, and Figure 19 for the flowchart.

Write Operation Status Detection

The 29LE010 provides two software means to detect the completion of a write cycle, in order to optimize the system write cycle time. The software detection includes two status bits: Data# Polling (DQ_7) and Toggle Bit (DQ_6). The end of write detection mode is enabled after the rising WE# or CE# whichever occurs first, which initiates the internal write cycle.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the

accessed location an additional two (2) times. If both reads are valid, then the device has completed the write cycle, otherwise the rejection is valid.

Data# Polling (DQ_7)

When the 29LE010 is in the internal write cycle, any attempt to read DQ_7 of the last byte loaded during the byte-load cycle will receive the complement of the true data. Once the write cycle is completed, DQ_7 will show true data. The device is then ready for the next operation. See Figure 6 for Data# Polling timing diagram and Figure 16 for a flowchart.

Toggle Bit (DQ_6)

During the internal write cycle, any consecutive attempts to read DQ_6 will produce alternating 0's and 1's, i.e., toggling between 0 and 1. When the write cycle is completed, the toggling will stop. The device is then ready for the next operation. See Figure 7 for Toggle Bit timing diagram and Figure 16 for a flowchart. The initial read of the Toggle Bit will be a "1".

Data Protection

The 29LE010 provides both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a write cycle.

V_{CC} Power Up/Down Detection: The write operation is inhibited when V_{CC} is less than 2.5V.

Write Inhibit Mode: Forcing OE# low, CE# high, or WE# high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down.

Software Data Protection (SDP)

The 29LE010 provides the JEDEC approved optional software data protection scheme for all data alteration operations, i.e., write and chip erase. With this scheme, any write operation requires the inclusion of a series of three byte-load operations to precede the data loading operation. The three byte-load sequence is used to initiate the write cycle, providing optimal protection from inadvertent write operations, e.g., during the system power-up or power-down. The 29LE010 is shipped with the software data protection disabled.

The software protection scheme can be enabled by applying a three-byte sequence to the device, during a page-load cycle (Figure 8). The device will then be automatically set into the data protect mode. Any subsequent write operation will require the preceding three-byte sequence. See Table 4 for the specific software command codes and Figure 8 for the timing diagram. To set the device into the unprotected mode, a six-byte sequence is required. See Table 4 for the specific codes and Figure 9 for the timing diagram. If a write is attempted while SDP is enabled the device will be in a non-accessible state for ~ 300 µs. SST recommends Software Data Protection always be enabled. See Figure 17 for flowcharts.

The 29LE010 Software Data Protection is a global command, protecting (or unprotecting) all pages in the entire memory array once enabled (or disabled). Therefore using SDP for a single page write will enable SDP for the entire array. Single pages by themselves cannot be SDP enabled or disabled.

Single power supply reprogrammable nonvolatile memories may be unintentionally altered. SST strongly recommends that Software Data Protection (SDP) always be enabled. The 29LE010 should be programmed using the SDP command sequence. SST recommends the SDP Disable Command Sequence not be issued to the device prior to writing.

Product Identification

The product identification mode identifies the device as the 29LE010 and manufacturer as SST. This mode may be accessed by hardware or software operations. The hardware operation is typically used by a programmer to identify the correct algorithm for the 29LE010. Users may wish to use the software product identification operation to identify the part (i.e., using the device code) when using multiple manufacturers in the same socket. For details, see Table 3 for hardware operation or Table 4 for software operation, Figure 11 for the software ID entry and read timing diagram and Figure 18 for the ID entry command sequence flowchart. The manufacturer and device codes are the same for both operations.

Table 1: Product Identification Table

	Byte	Data
Manufacturers Code	0000 H	BF H
Device Code	0001 H	07 H

Product Identification Mode Exit

In order to return to the standard read mode, the Software Product Identification mode must be exited. Exiting is accomplished by issuing the Software ID Exit (reset) operation, which returns the device to the read operation. The reset operation may also be used to reset the device to the read mode after an inadvertent transient condition that apparently causes the device to behave abnormally, e.g., not read correctly. See Table 4 for software command codes, Figure 12 for timing wavefrom and Figure 18 for a flowchart.

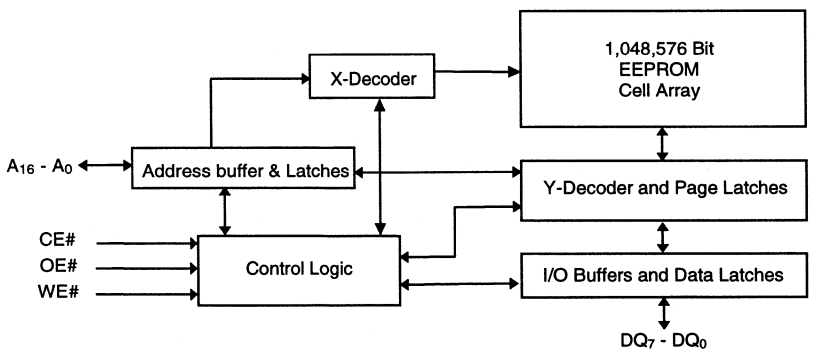


Figure 1: Functional Block Diagram of SST 29LE010

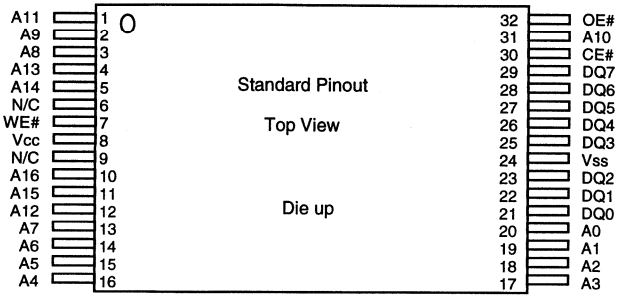


Figure 2A: Pin Assignments for 32-pin TSOP Packages

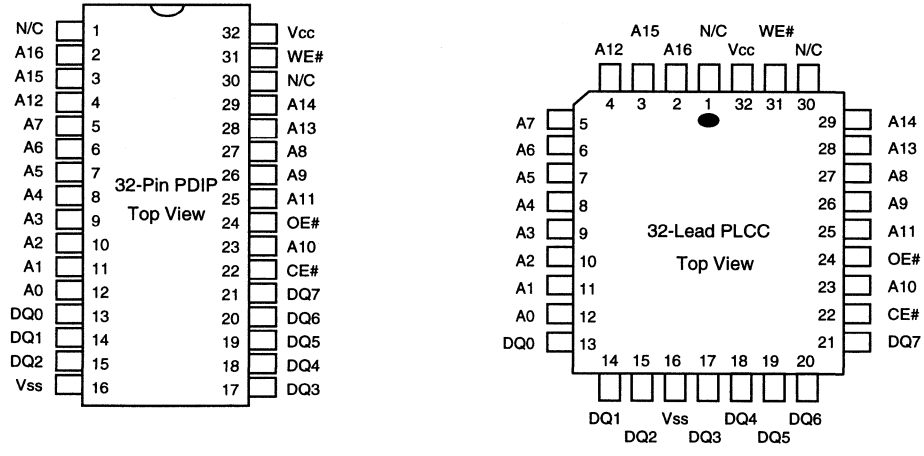


Figure 2B: Pin Assignments for 32-pin Plastic DIPs and 32-lead PLCCs

Table 2: Pin Description

Symbol	Pin Name	Functions
A_{16}-A_7	Row Address Inputs	To provide memory addresses. Row addresses define a page for a write cycle.
A_6-A_0	Column Address Inputs	Column Addresses are toggled to load page data.
DQ_7-DQ_0	Data Input/output	To output data during read cycles and receive input data during write cycles. Data is internally latched during a write cycle. The outputs are in tri-state when OE# or CE# is high.
CE#	Chip Enable	To activate the device when CE# is low.
OE#	Output Enable	To gate the data output buffers.
WE#	Write Enable	To control the write operations
Vcc	Power Supply	To provide 3.3-volt supply (± 0.3V)
Vss	Ground	
NC	No Connection	Unconnected pins.

Table 3: Operation Modes Selection

Mode	CE#	OE#	WE#	DQ	Address
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	A_{IN}
Page Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}
Standby	V_{IH}	X	X	High Z	X
Write Inhibit	X	V_{IL}	X	High Z/ D_{OUT}	X
Write Inhibit	X	X	V_{IH}	High Z/ D_{OUT}	X
Software Chip Erase	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}, See Table 4
Product Identification					
Hardware Mode	V_{IL}	V_{IL}	V_{IH}	Manufacturer Code (BF) Device Code (07)	A_{16} - A_1 = V_{IL}, A_9 = V_H, A_0 = V_{IL} A_{16} - A_1 = V_{IL}, A_9 = V_H, A_0= V_{IH}
Software Mode	V_{IL}	V_{IH}	V_{IL}		See Table 4
SDP Enable Mode	V_{IL}	V_{IH}	V_{IL}		See Table 4
SDP Disable Mode	V_{IL}	V_{IH}	V_{IL}		See Table 4

Table 4: Software Command Codes

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data
Software Data Protect Enable & Page Write	5555H	AAH	2AAAH	55H	5555H	A0H	Addr[2]	Data				
Software Data Protect Disable	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	20H
Software Chip Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	60H
Software ID Exit	5555H	AAH	2AAAH	55H	5555H	F0H						

Notes: (1) Address format A_{14}-A_0 (Hex), Addresses A_{15} and A_{16} are a "Don't Care".

(2) Page Write consists of loading up to 128 bytes (A_6 - A_0).

Notes for Software Product ID Command Code:

1. With A_{14} -A_1 =0; SST Manufacturer Code = BFH, is read with A_0 = 0,
   29LE010 Device Code = 07H, is read with A_0 = 1.
2. The device does not remain in Software Product ID Mode if powered down.

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential ..... -0.5V to V_{CC}+ 0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential ..... -1.0V to V_{CC}+ 1.0V
Voltage on A_9 Pin to Ground Potential ..... -0.5V to 14.0V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Through Hole Lead Soldering Temperature (10 Seconds) ..... 300°C
Surface Mount Lead Soldering Temperature (3 Seconds) ..... 240°C
Output Short Circuit Current[1] ..... 100 mA

Note: [1] Outputs shorted for no more than one second. No more than one output shorted at a time.

Operating Range

Range	Ambient Temp	V_{CC}
Commercial	0 °C to +70 °C	3.0V to 3.6V
Industrial	-40 °C to +85 °C	3.0V to 3.6V

AC Conditions of Test

Input Rise/Fall Time.....10 ns
Output Load.....1 TTL Gate and C_L = 100 pF
See Figures 13 and 14

Table 5: DC Operating Characteristics

Symbol	Parameter	Limits Min	Limits Max	Units	Test Conditions
I_{CC}	Power Supply Current				CE#=OE#=V_{IL},WE#=V_{IH}, all I/Os open,
	Read		12	mA	Address input = V_{IL}/V_{IH}, at f=1/T_{RC} Min., V_{CC}=V_{CC} Max
	Write		15	mA	CE#=WE#=V_{IL}, OE#=V_{IH}, V_{CC}=V_{CC} Max.
I_{SB1}	Standby V_{CC} Current (TTL input)		1	mA	CE#=OE#=WE#=V_{IH}, V_{CC}=V_{CC} Max.
I_{SB2}	Standby V_{CC} Current (CMOS input)		15	µA	CE#=OE#=WE#=V_{CC} -0.3V. V_{CC} = V_{CC} Max.
I_{LI}	Input Leakage Current		1	µA	V_{IN} =GND to V_{CC}, V_{CC} = V_{CC} Max.
I_{LO}	Output Leakage Current		10	µA	V_{OUT} =GND to V_{CC}, V_{CC} = V_{CC} Max.
V_{IL}	Input Low Voltage		0.8	V	V_{CC} = V_{CC} Max.
V_{IH}	Input High Voltage	2.0		V	V_{CC} = V_{CC} Max.
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 100 µA, V_{CC} = V_{CC} Min.
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -100 µA, V_{CC} = V_{CC} Min.
V_H	Supervoltage for A_9	11.6	12.4	V	CE# = OE# =V_{IL}, WE# = V_{IH}
I_H	Supervoltage Current for A_9		100	µA	CE# = OE# = V_{IL}, WE# = V_{IH}, A_9 = V_H Max.

Table 6: Power-up Timings

Symbol	Parameter	Maximum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$[1]	Power-up to Write Operation	5	ms

Table 7: Capacitance (Ta = 25 °C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0v	6 pF

Note: [1]This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 8: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}	Endurance	1,000 & 10,000[2]	Cycles	MIL-STD-883, Method 1033
T_{DR}[1]	Data Retention	100	Years	MIL-STD-883, Method 1008
V_{ZAP_HBM}[1]	ESD Susceptibility Human Body Model	1000	Volts	JEDEC Standard A114
V_{ZAP_MM}[1]	ESD Susceptibility Machine Model	200	Volts	JEDEC
I_{LTH}[1]	Latch Up	100	mA	JEDEC Standard 17

Note: [1]This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

[2]See Ordering Information for desired type.

AC Characteristics

Table 9: Read Cycle Timing Parameters

Symbol	Parameter	29LE010-150		29LE010-200		Units
		Min	Max	Min	Max	
T_{RC}	Read Cycle time	150		200		ns
T_{CE}	Chip Enable Access Time		150		200	ns
T_{AA}	Address Access Time		150		200	ns
T_{OE}	Output Enable Access Time		60		100	ns
T_{CLZ}[1]	CE# Low to Active Output	0		0		ns
T_{OLZ}[1]	OE# Low to Active Output	0		0		ns
T_{CHZ}[1]	CE# High to High-Z Output		30		50	ns
T_{OHZ}[1]	OE# High to High-Z Output		30		50	ns
T_{OH}[1]	Output Hold from Address Change	0		0		ns

Table 10: Page-Write Cycle Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{WC}	Write Cycle (erase and program)		10	ms
T_{AS}	Address Setup Time	0		ns
T_{AH}	Address Hold Time	50		ns
T_{CS}	WE# and CE# Setup Time	0		ns
T_{CH}	WE# and CE# Hold Time	0		ns
T_{OES}	OE# High Setup Time	0		ns
T_{OEH}	OE# High Hold Time	0		ns
T_{CP}	CE# Pulse Width	70		ns
T_{WP}	WE# Pulse Width	70		ns
T_{DS}	Data Setup Time	35		ns
T_{DH}	Data Hold Time	0		ns
T_{BLC}[1]	Byte Load Cycle Time	0.05	100	µs
T_{BLCO}[1]	Byte Load Cycle Time	200		µs
T_{IDA}	Software ID Access and Exit Time		10	µs
T_{SCE}	Software Chip Erase		20	ms

Note: [1]This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.

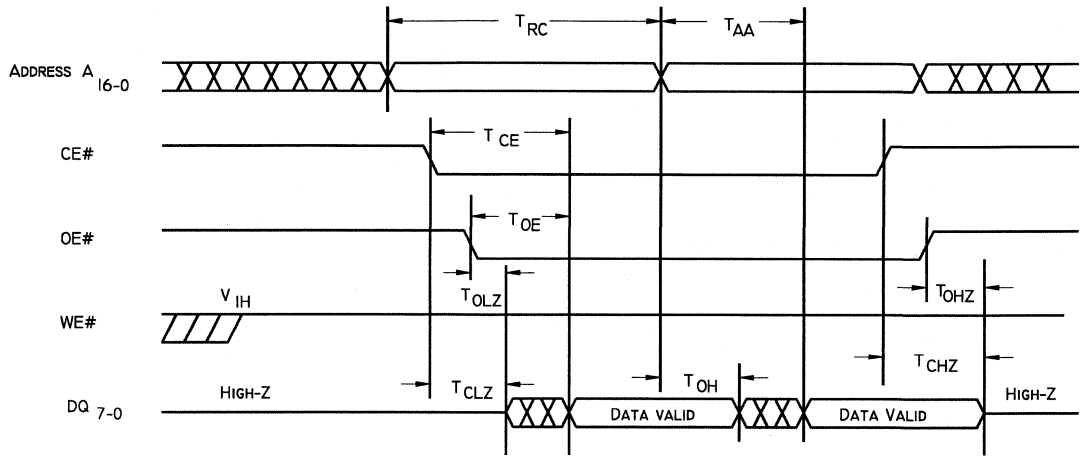


Figure 3: Read Cycle Timing Diagram

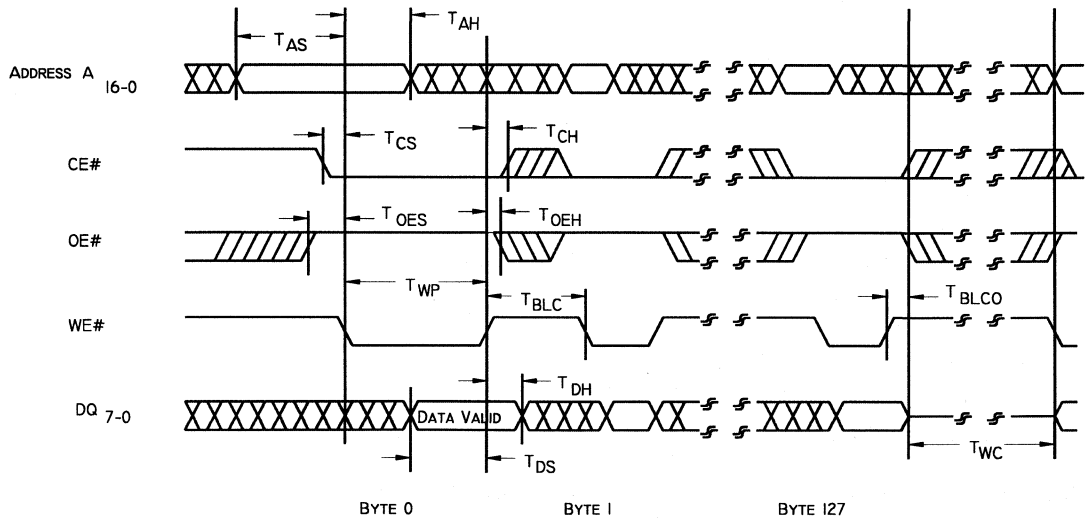


Figure 4: WE# Controlled Page Write Cycle Timing Diagram

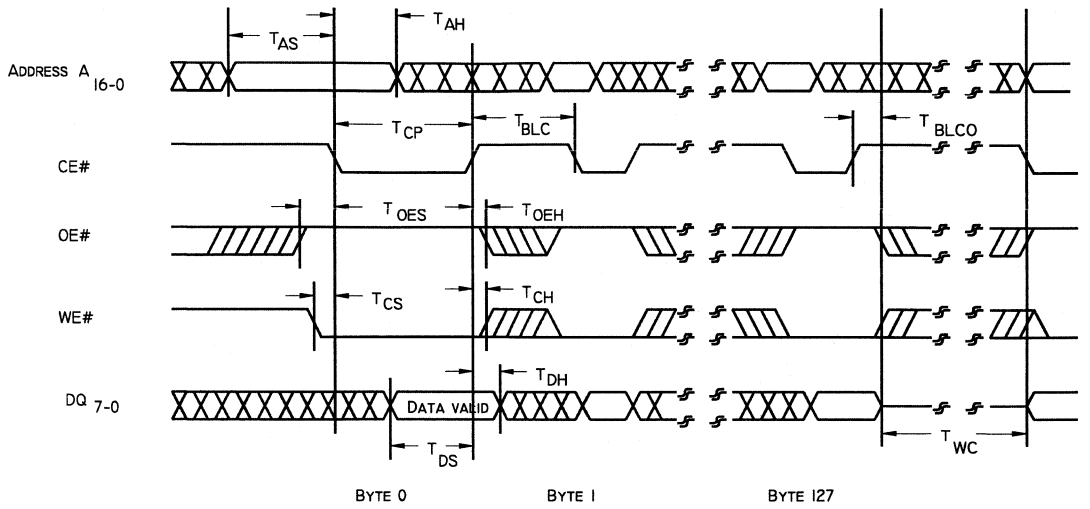


Figure 5: CE# Controlled Page Write Cycle Timing Diagram

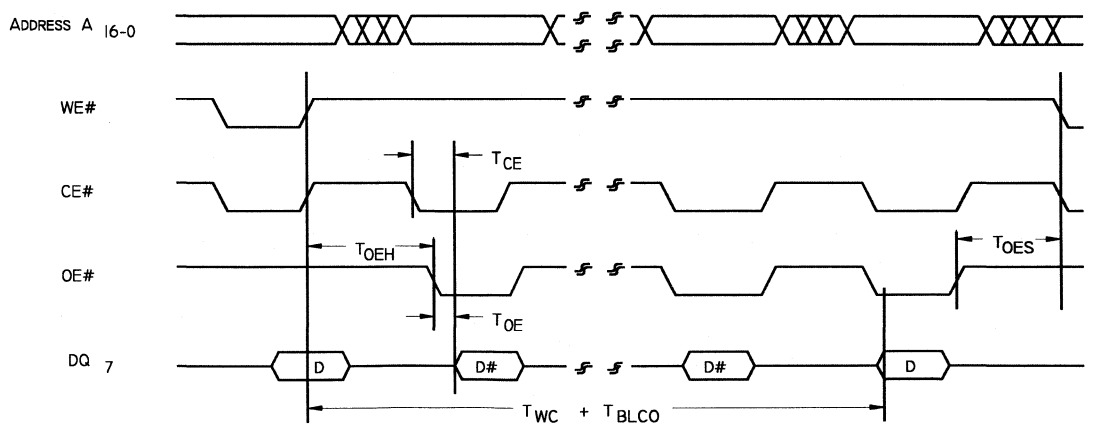


Figure 6: Data# Polling Timing Diagram

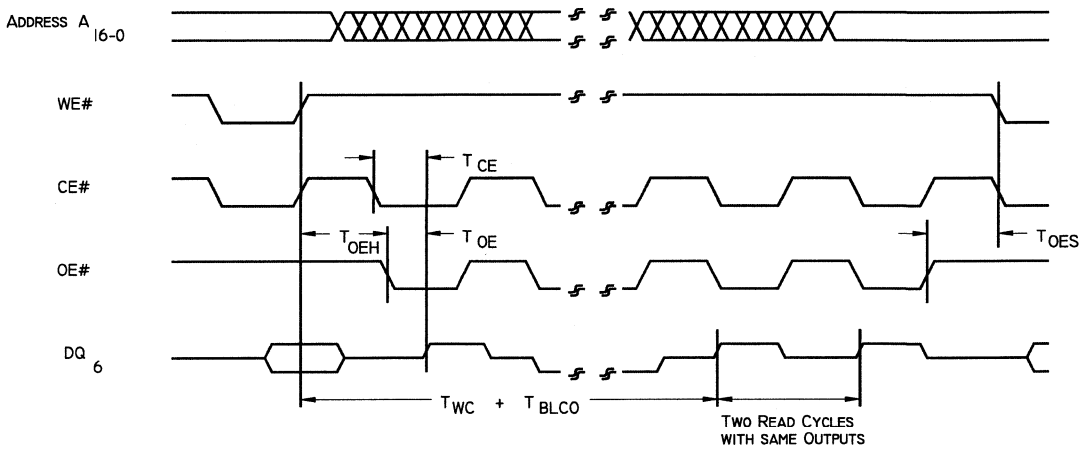
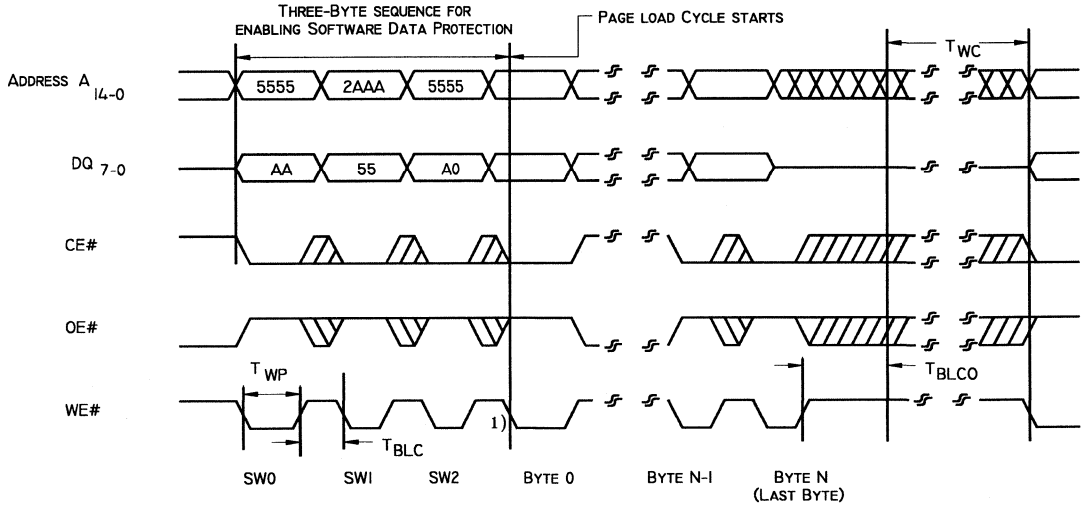


Figure 7: Toggle Bit Timing Diagram



NOTE 1): THE TIME BETWEEN ENABLING SOFTWARE DATA PROTECT AND THE PAGE LOAD MUST BE LESS THAN T_{BLCO}

Figure 8: Software Data Protection Page Write Timing Diagram

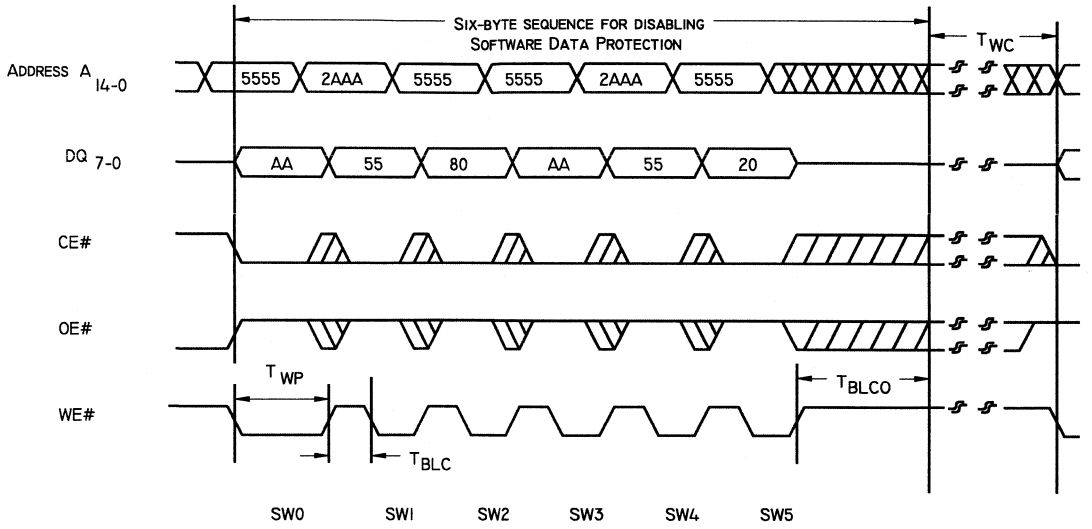


Figure 9: Software Data Protect Disable Timing Diagram

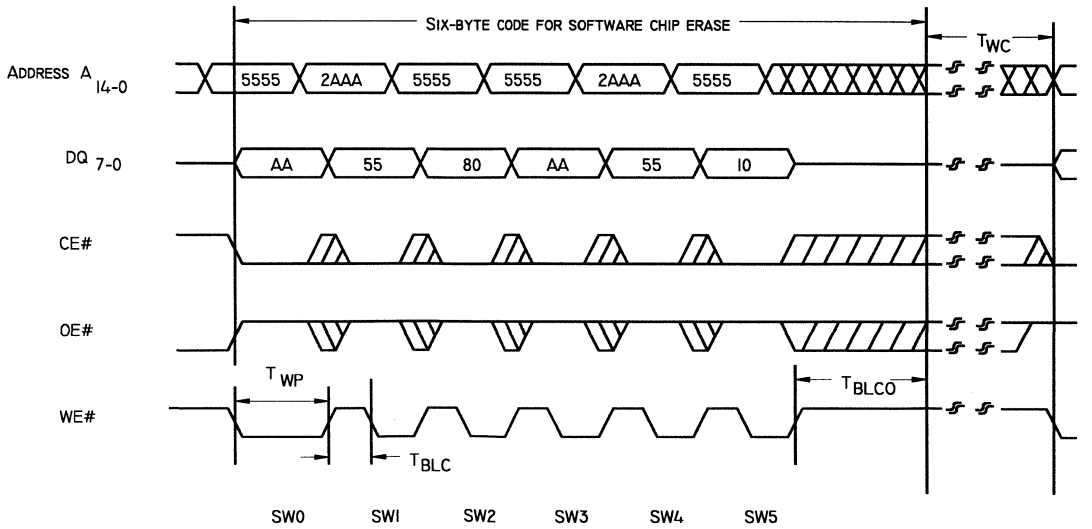


Figure 10: Software Chip Erase Timing Diagram

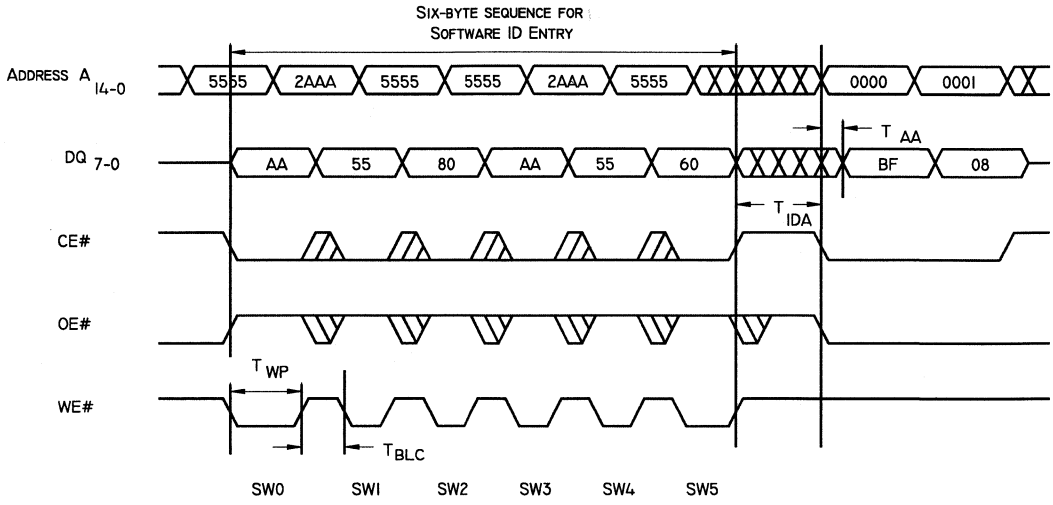


Figure 11: Software ID Entry and Read

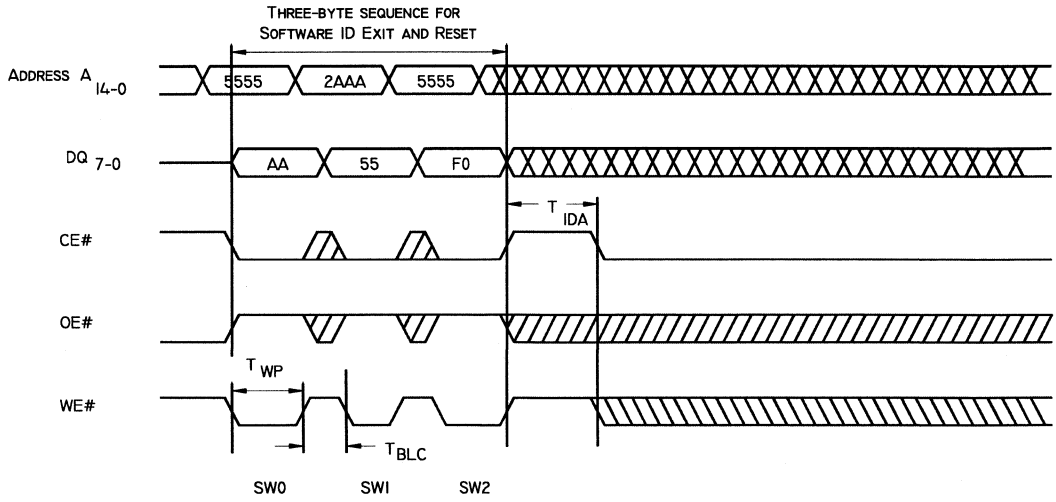
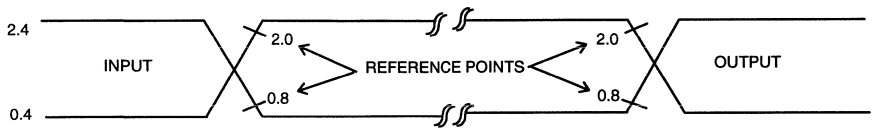


Figure 12: Software ID Exit and Reset



AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a logic "1" and V_{OL} (0.4 V_{TTL}) for a logic "0". Measurement reference points for inputs or outputs are V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Inputs rise and fall times (10% ↔ 90%) are <10 ns.

Figure 13: AC Input/Output Reference Waveforms

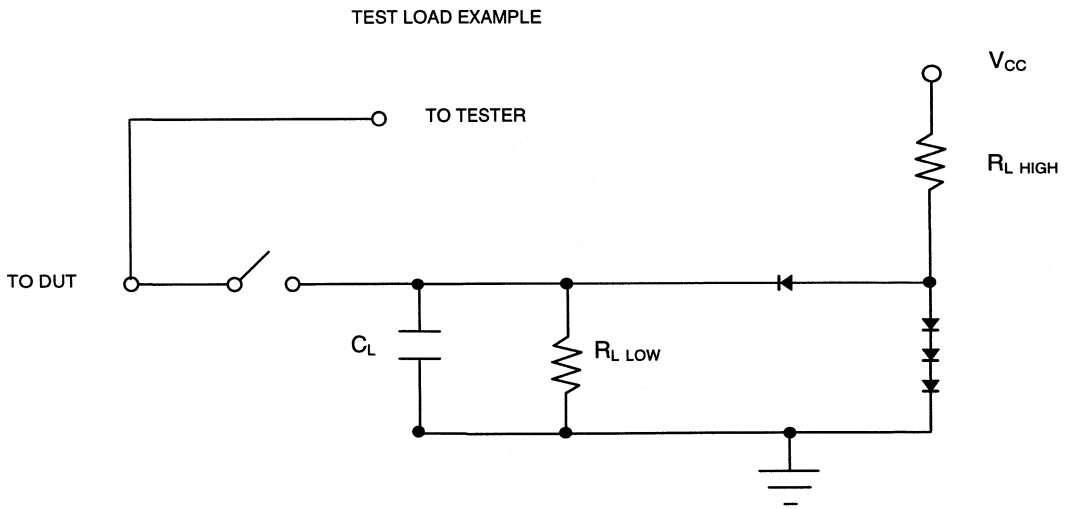


Figure 14: Test Load Example

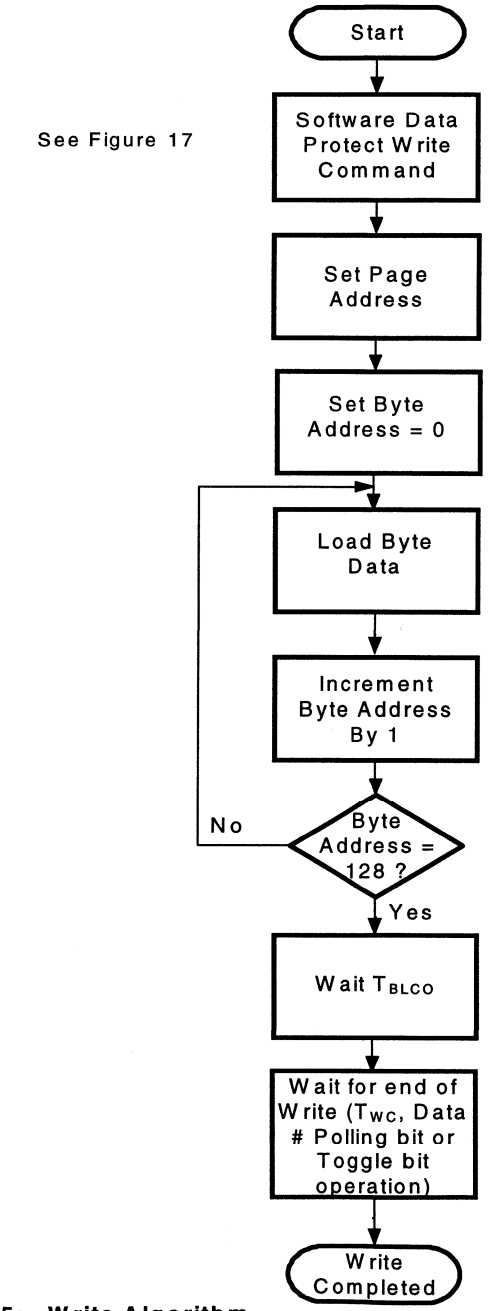


Figure 15: Write Algorithm

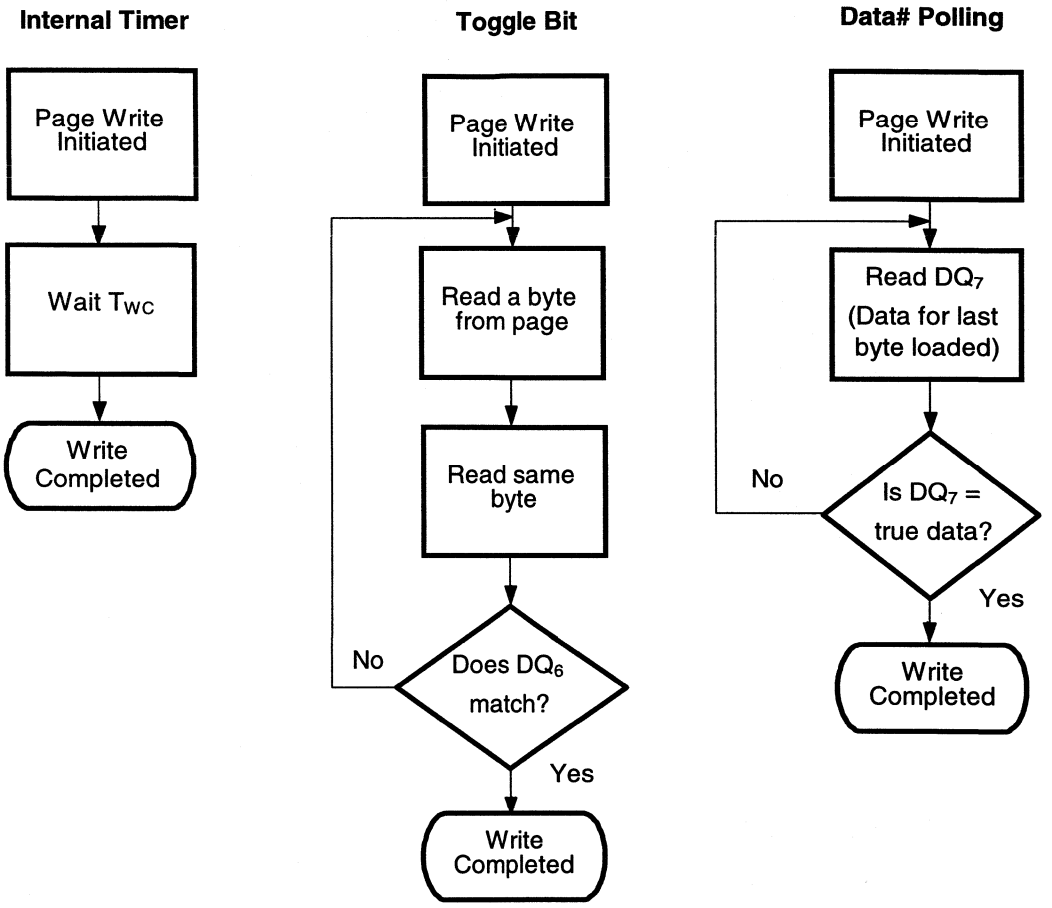


Figure 16: Wait Options

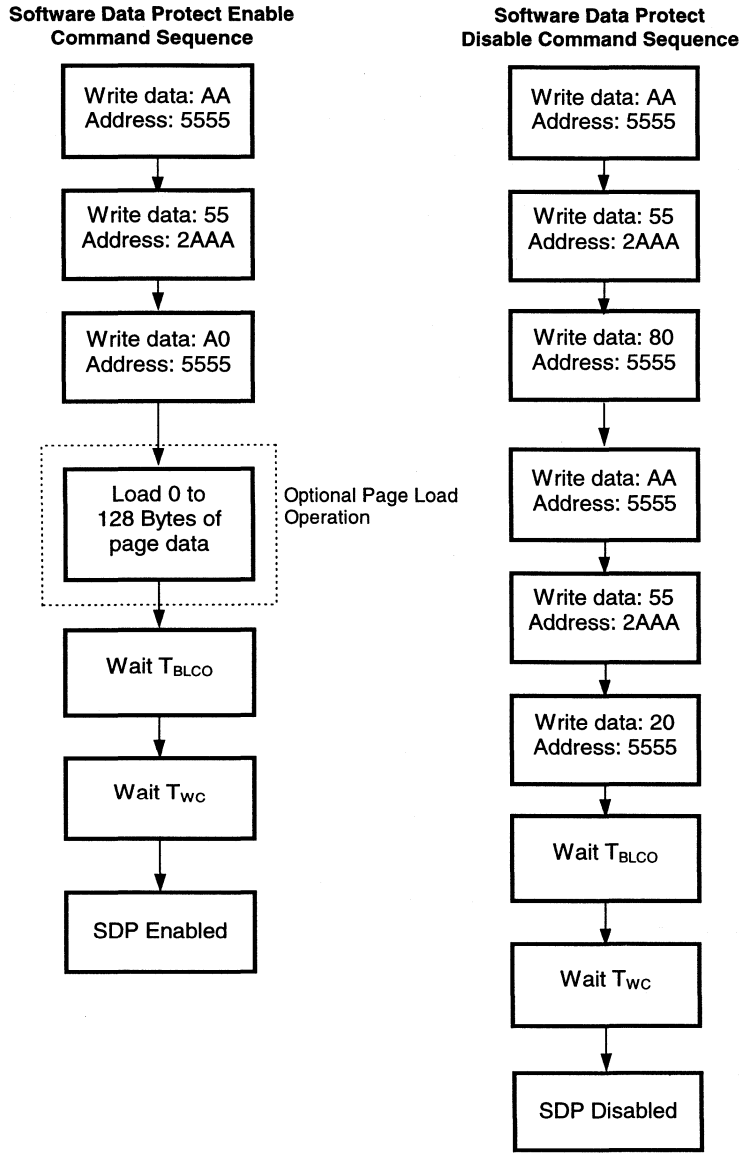


Figure 17: Software Data Protection Flowcharts

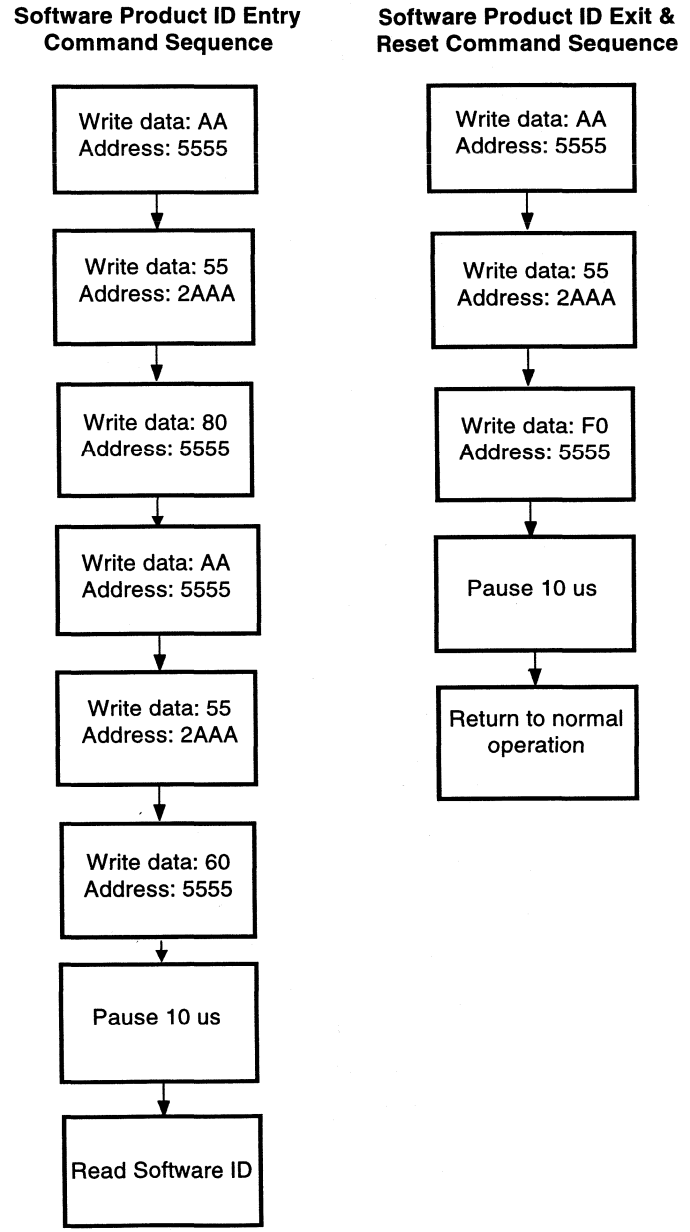


Figure 18: Software Product Command Flowcharts

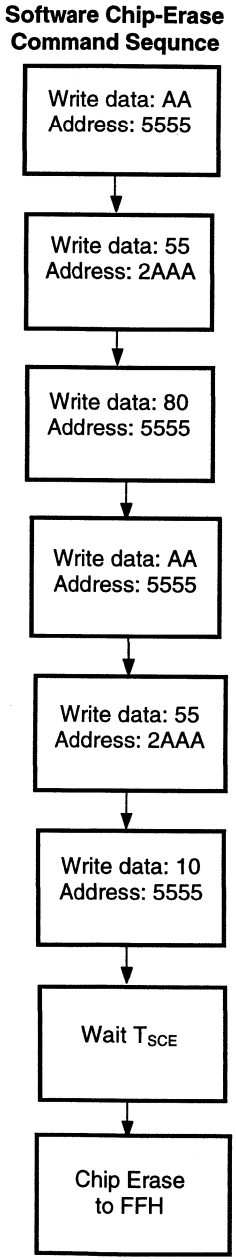
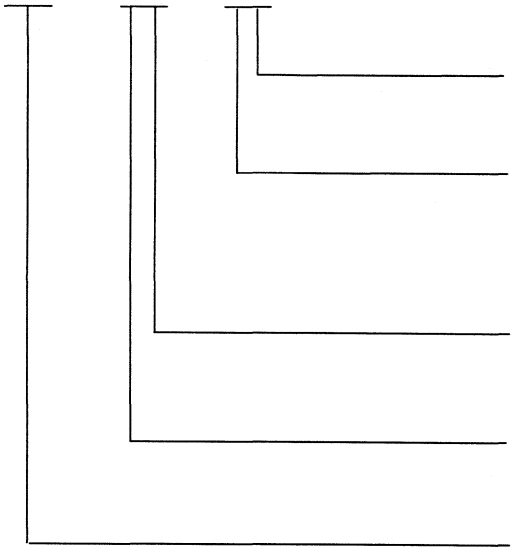


Figure 19: Software Chip Erase Command Codes

Product Ordering Information

Device		Speed		Suffix1		Suffix2
SST29LE010	-	XXX	-	XX	-	XX



Package Modifier
H = 32 leads
Numeric = Die modifier

Package Type
P = PDIP
N = PLCC
E = TSOP (die up)
U = Unencapsulated die

Operating Temperature
C = Commercial = 0° to 70°C
I = Industrial = -40° to 85°C

Minimum Endurance
3 = 1000 cycles
4 = 10,000 cycles

Read Access Speed
150 = 150 ns
200 = 200 ns

Valid combinations

SST29LE010-150-4C- EH	SST29LE010-150-4C- NH	SST29LE010-150-4C- PH
SST29LE010-200-4C- EH	SST29LE010-200-4C- NH	SST29LE010-200-4C- PH
SST29LE010-150-3C- EH	SST29LE010-150-3C- NH	SST29LE010-150-3C- PH
SST29LE010-200-3C- EH	SST29LE010-200-3C- NH	SST29LE010-200-3C- PH
SST29LE010-150-4I-EH	SST29LE010-150-4I-NH	
SST29LE010-200-4I-EH	SST29LE010-200-4I-NH	SST29LE010-200-4C-U1
SST29LE010-150-3I-EH	SST29LE010-150-3I-NH	
SST29LE010-200-3I-EH	SST29LE010-200-3I-NH	SST29LE010-200-3C-U1

Example: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Data Sheet

SST 29VE010
2.7V-only 1 Megabit
Page Mode EEPROM

July 1996

SST 29VE010
2.7V-only 1 Megabit
Page Mode EEPROM

Features:

Single 2.7-Volt Read and Write Operations
CMOS SuperFlash EEPROM Technology
- Endurance: 100,000 Cycles (typical)
- Greater than 100 years Data Retention

Low Power Consumption:
- Active Current: 10 mA (typical)
- Standby Current: 10 µA (typical)

Fast Page-Write Operation
- 128 Bytes per Page, 1024 Pages
- Page-Write Cycle: 5 ms (typical)
- Complete Memory Rewrite: 5 sec (typical)
- Effective Byte-write Cycle Time: 39 µs (typical)

Fast Access Time: 200 and 250 ns
Latched Address and Data
Automatic Write Timing with Internal V_{PP} Generation
End of Write Detection
- Toggle Bit
- Data# Polling

Hardware and Software Data Protection
TTL I/O Compatibility
JEDEC Standard Byte-wide EEPROM Pinouts
Packages Available
- 32-Pin TSOP
- 32-Lead PLCC
- 32 Pin Plastic DIP

Product Description

The 29VE010 is a 128K x 8 CMOS page mode EEPROM manufactured with SST's proprietary, high performance CMOS SuperFlash technology. The split gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The 29VE010 writes with a 2.7-volt-only power supply. (V_{CC}: 2.7V to 3.6V) Internal erase/program is transparent to the user. The 29VE010 conforms to JEDEC standard pinouts for byte-wide memories.

Featuring high performance page write, the 29VE010 provides a typical byte-write time of 39 µsec. The entire memory, i.e., 128K bytes, can be written page by page in as little as 5 seconds, when using interface features such as Toggle Bit or Data# Polling to indicate the completion of a write cycle. To protect against inadvertent write, the 29VE010 has on-chip hardware and software data protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, the 29VE010 is offered with a guaranteed page-write endurance of 10^4 or 10^3 cycles. Data retention is rated at greater than 100 years.

The 29VE010 is suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, the 29VE010 significantly improves performance and reliability, while lowering power consumption, when compared with 5 volt EEPROM or EPROM approaches. The 29VE010 improves flexibility while lowering the cost for program, data, and configuration storage applications.

To meet high density, surface mount requirements, the 29VE010 is offered in 32-pin TSOP and 32-lead PLCC packages. A 600-mil, 32-pin PDIP package is also available. See Figures 2A and 2B for pinouts.

Device Operation

The SST page mode EEPROM offers in-circuit electrical write capability. The 29VE010 does not require separate erase and program operations. The internally timed write cycle executes both erase and program transparently to the user. The 29VE010 has industry standard optional Software Data Protection, which SST recommends always to be enabled. The 29VE010 is compatible with industry standard EEPROM pinouts and functionality.

Read

The read operation of the 29VE010 is controlled by CE# and OE#, both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the read cycle timing diagram for further details (Figure 3).

Write

The write operation consists of three steps. The first step is the optional three byte load sequence for Software Data Protection. This is an optional first step in the write operation, but highly recommended to ensure proper data integrity. Step 2 is the byte-load cycle to a page buffer of the 29VE010. Step 3 is an internally controlled write cycle for writing the data loaded in the page buffer into the memory array for nonvolatile storage. During the byte-load cycle, the addresses are latched by the falling edge of either CE# or WE#, whichever occurs last. The data is latched by the rising edge of either CE# or WE#, whichever occurs first. The internal write cycle is initiated by a timer after the rising edge of WE# or CE#, whichever occurs first. The write cycle, once initiated, will continue to completion, typically within 5 ms. See Figures 4 and 5 for WE# and CE# controlled page write cycle timing diagrams and Figures 15 and 17 for flowcharts.

The write operation has three functional cycles: the optional Software Data Protection load sequence, the page load cycle and the internal write cycle. The Software Data Protection consists of a specific three byte load sequence that will leave the 29VE010 protected at the end of the page write. The page load cycle consists of loading 1 to 128 bytes of data into the page buffer. The internal write cycle consists of the T_{BLCO} time-out and the write timer operation. During the write operation, the only valid reads are Data# Polling and Toggle Bit.

The page-write operation allows the loading of up to 128 bytes of data into the page buffer of the 29VE010 before the initiation of the internal write cycle. During the internal write cycle, all the data in the page buffer is written simultaneously into the memory array. Hence, the page-write feature of 29VE010 allows the entire memory to be written in as little as 5 seconds. During the internal write cycle, the host is free to perform additional tasks, such as to fetch data from other locations in the system to set up the write to the next page. In each page-write operation, all the bytes that are loaded into the page buffer must have the same page address, i.e., A_7 through A_{16}. Any byte not loaded with user data will be written to FF.

See Figures 4, 5, and 8 for the page-write cycle timing diagrams. If after the initial byte-load cycle, the host loads a second byte into the page buffer within a byte-load cycle time (T_{BLC}) of 100 µs, the 29VE010 will stay in the page load cycle. Additional bytes are then loaded consecutively. The page load cycle will be terminated if no additional byte is loaded into the page buffer within 200 µs (T_{BLCO}) from the last byte-load cycle, i.e., no subsequent WE# or CE# high-to-low transition after the last rising edge of WE# or CE#. Data in the page buffer can be changed by a subsequent byte-load cycle. The page load period can continue indefinitely, as long as the host continues to load the device within the byte-load cycle time of 100 µs. The page to be loaded is determined by the page address of the last byte loaded.

Software Chip-Erase

The 29VE010 provides a chip-erase operation, which allows the user to simultaneously clear the entire memory array to the "1" state. This is useful when the entire device must be quickly erased.

The Software Chip-Erase operation is initiated by using a specific six byte-load sequence. After the load sequence, the device enters into an internally timed cycle similar to the write cycle. During the erase operation, the only valid read is Toggle Bit. See Table 4 for the load sequence, Figure 10 for timing diagram, and Figure 19 for the flowchart.

Write Operation Status Detection

The 29VE010 provides two software means to detect the completion of a write cycle, in order to optimize the system write cycle time. The software detection includes two status bits: Data# Polling (DQ_7) and Toggle Bit (DQ_6). The end of write detection mode is enabled after the rising WE# or CE# whichever occurs first, which initiates the internal write cycle.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the

accessed location an additional two (2) times. If both reads are valid, then the device has completed the write cycle, otherwise the rejection is valid.

Data# Polling (DQ_7)

When the 29VE010 is in the internal write cycle, any attempt to read DQ_7 of the last byte loaded during the byte-load cycle will receive the complement of the true data. Once the write cycle is completed, DQ_7 will show true data. The device is then ready for the next operation. See Figure 6 for Data# Polling timing diagram and Figure 16 for a flowchart.

Toggle Bit (DQ_6)

During the internal write cycle, any consecutive attempts to read DQ_6 will produce alternating 0's and 1's, i.e., toggling between 0 and 1. When the write cycle is completed, the toggling will stop. The device is then ready for the next operation. See Figure 7 for Toggle Bit timing diagram and Figure 16 for a flowchart. The read of the Toggle Bit will be a "1".

Data Protection

The 29VE010 provides both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a write cycle.

V_{CC} Power Up/Down Detection: The write operation is inhibited when V_{CC} is less than 2.5V.

Write Inhibit Mode: Forcing OE# low, CE# high, or WE# high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down.

Software Data Protection (SDP)

The 29VE010 provides the JEDEC approved optional software data protection scheme for all data alteration operations, i.e., write and chip erase. With this scheme, any write operation requires the inclusion of a series of three byte-load operations to precede the data loading operation. The three byte-load sequence is used to initiate the write cycle, providing optimal protection from inadvertent write operations, e.g., during the system power-up or power-down. The 29VE010 is shipped with the software data protection disabled.

The software protection scheme can be enabled by applying a three-byte sequence to the device, during a page-load cycle (Figure 8). The device will then be automatically set into the data protect mode. Any subsequent write operation will require the preceding three-byte sequence. See Table 4 for the specific software command codes and Figure 8 for the timing diagram. To set the device into the unprotected mode, a six-byte sequence is required. See Table 4 for the specific codes and Figure 9 for the timing diagram. If a write is attempted while SDP is enabled the device will be in a non-accessible state for ~ 300 µs. SST recommends Software Data Protection always be enabled. See Figure 17 for flowcharts.

The 29VE010 Software Data Protection is a global command, protecting (or unprotecting) all pages in the entire memory array once enabled (or disabled). Therefore using SDP for a single page write will enable SDP for the entire array. Single pages by themselves cannot be SDP enabled or disabled.

Single power supply reprogrammable nonvolatile memories may be unintentionally altered. SST strongly recommends that Software Data Protection (SDP) always be enabled. The 29VE010 should be programmed using the SDP command sequence. SST recommends the SDP Disable Command Sequence not be issued to the device prior to writing.

Product Identification

The product identification mode identifies the device as the 29VE010 and manufacturer as SST. This mode may be accessed by hardware or software operations. The hardware operation is typically used by a programmer to identify the correct algorithm for the 29VE010. Users may wish to use the software product identification operation to identify the part (i.e., using the device code) when using multiple manufacturers in the same socket. For details, see Table 3 for hardware operation or Table 4 for software operation, Figure 11 for the software ID entry and read timing diagram and Figure 18 for the ID entry command sequence flowchart. The manufacturer and device codes are the same for both operations.

Table 1: Product Identification Table

	Byte	Data
Manufacturers Code	0000 H	BF H
Device Code	0001 H	07 H

Product Identification Mode Exit

In order to return to the standard read mode, the Software Product Identification mode must be exited. Exiting is accomplished by issuing the Software ID Exit (reset) operation, which returns the device to the read operation. The reset operation may also be used to reset the device to the read mode after an inadvertent transient condition that apparently causes the device to behave abnormally, e.g., not read correctly. See Table 4 for software command codes, Figure 12 for timing waveform and Figure 18 for a flowchart.

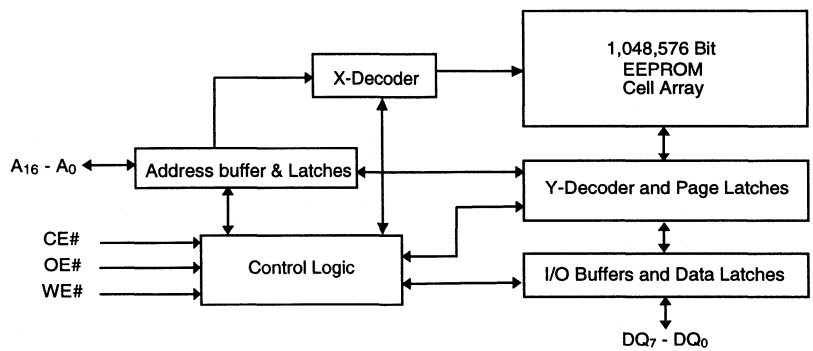


Figure 1: Functional Block Diagram of SST 29VE010

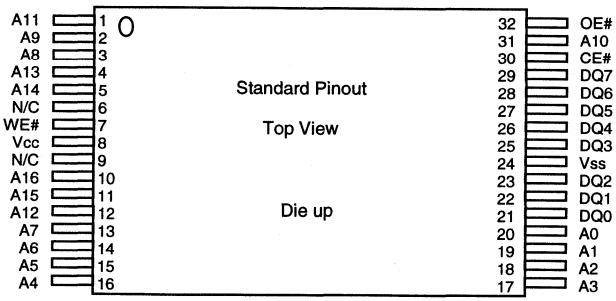


Figure 1A: Pin Assignments for 32-pin TSOP Packages

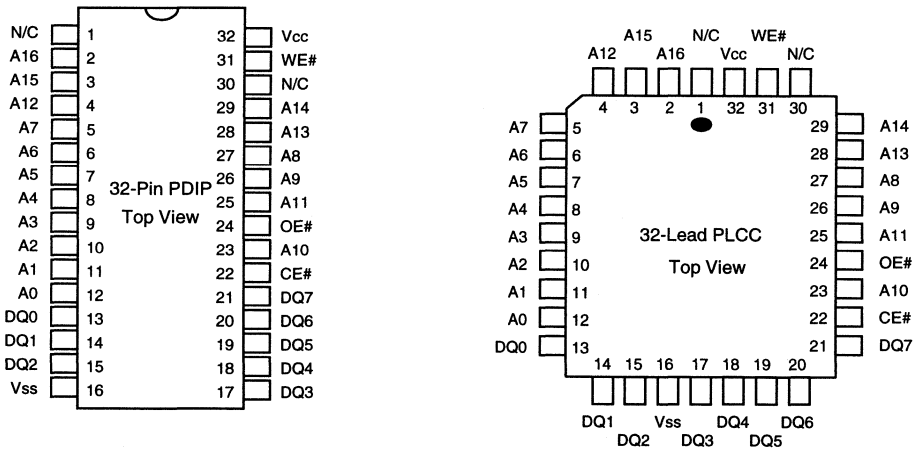


Figure 2B: Pin Assignments for 32-pin Plastic DIPs and 32-lead PLCCs

Table 2: Pin Description

Symbol	Pin Name	Functions
A_{16}-A_7	Row Address Inputs	To provide memory addresses. Row addresses define a page for a write cycle.
A_6-A_0	Column Address Inputs	Column Addresses are toggled to load page data.
DQ_7-DQ_0	Data Input/output	To output data during read cycles and receive input data during write cycles. Data is internally latched during a write cycle. The outputs are in tri-state when OE# or CE# is high.
CE#	Chip Enable	To activate the device when CE# is low.
OE#	Output Enable	To gate the data output buffers.
WE#	Write Enable	To control the write operations
Vcc	Power Supply	To provide 3.0-volt supply (2.7 - 3.6V)
Vss	Ground	
NC	No Connection	Unconnected pins.

Table 3: Operation Modes Selection

Mode	CE#	OE#	WE#	DQ	Address
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	A_{IN}
Page Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}
Standby	V_{IH}	X	X	High Z	X
Write Inhibit	X	V_{IL}	X	High Z/ D_{OUT}	X
Write Inhibit	X	X	V_{IH}	High Z/ D_{OUT}	X
Software Chip Erase	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}, See Table 4
Product Identification					
Hardware Mode	V_{IL}	V_{IL}	V_{IH}	Manufacturer Code (BF)	A_{16} - A_1 = V_{IL}, A_9 = V_H, A_0 = V_{IL}
				Device Code (07)	A_{16} - A_1 = V_{IL}, A_9 = V_H, A_0= V_{IH}
Software Mode	V_{IL}	V_{IH}	V_{IL}		See Table 4
SDP Enable Mode	V_{IL}	V_{IH}	V_{IL}		See Table 4
SDP Disable Mode	V_{IL}	V_{IH}	V_{IL}		See Table 4

Table 4: Software Command Codes

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data
Software Data Protect Enable & Page Write	5555H	AAH	2AAAH	55H	5555H	A0H	Addr[2]	Data				
Software Data Protect Disable	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	20H
Software Chip Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	60H
Software ID Exit	5555H	AAH	2AAAH	55H	5555H	F0H						

Notes: (1) Address format A_{14}-A_0 (Hex), Addresses A_{15} and A_{16} are a "Don't Care".

(2) Page Write consists of loading up to 128 bytes (A_6 - A_0).

Notes for Software Product ID Command Code:

1. With A_{14}-A_1 =0; SST Manufacturer Code = BFH, is read with A_0 = 0,
   29VE010 Device Code = 07H, is read with A_0 = 1.
2. The device does not remain in Software Product ID Mode if powered down.

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential ..... -0.5V to V_{CC}+ 0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential ..... -1.0V to V_{CC}+ 1.0V
Voltage on A_9 Pin to Ground Potential ..... -0.5V to 14.0V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Through Hole Lead Soldering Temperature (10 Seconds) ..... 300°C
Surface Mount Lead Soldering Temperature (3 Seconds) ..... 240°C
Output Short Circuit Current[1] ..... 100 mA

Note: [1] Outputs shorted for no more than one second. No more than one output shorted at a time.

Operating Range

Range	Ambient Temp	V_{CC}
Commercial	0 °C to +70 °C	2.7V to 3.6V
Industrial	-40 °C to +85 °C	2.7V to 3.6V

AC Conditions of Test

Input Rise/Fall Time.....10 ns
Output Load.....1 TTL Gate and C_L = 100 pF
See Figures 13 and 14

Table 5: DC Operating Characteristics

Symbol	Parameter	Limits Min	Limits Max	Limits Units	Test Conditions
I_{CC}	Power Supply Current				CE#=OE#=V_{IL},WE#=V_{IH}, all I/Os open,
	Read		12	mA	Address input = V_{IL}/V_{IH}, at f=1/T_{RC} Min., V_{CC}=V_{CC} Max
	Write		15	mA	CE#=WE#=V_{IL}, OE#=V_{IH}, V_{CC} =V_{CC} Max.
I_{SB1}	Standby V_{CC} Current (TTL input)		1	mA	CE#=OE#=WE#=V_{IH}, V_{CC} =V_{CC} Max.
I_{SB2}	Standby V_{CC} Current (CMOS input)		15	µA	CE#=OE#=WE#=V_{CC} -0.3V. V_{CC} = V_{CC} Max.
I_{LI}	Input Leakage Current		1	µA	V_{IN} =GND to V_{CC}, V_{CC} = V_{CC} Max.
I_{LO}	Output Leakage Current		10	µA	V_{OUT} =GND to V_{CC}, V_{CC} = V_{CC} Max.
V_{IL}	Input Low Voltage		0.8	V	V_{CC} = V_{CC} Max.
V_{IH}	Input High Voltage	2.0		V	V_{CC} = V_{CC} Max.
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 100 µA, V_{CC} = V_{CC} Min.
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -100 µA, V_{CC} = V_{CC} Min.
V_H	Supervoltage for A_9	11.6	12.4	V	CE# = OE# =V_{IL}, WE# = V_{IH}
I_H	Supervoltage Current for A_9		100	µA	CE# = OE# = V_{IL}, WE# = V_{IH}, A_9 = V_H Max.

Table 6: Power-up Timings

Symbol	Parameter	Maximum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$[1]	Power-up to Write Operation	5	ms

Table 7: Capacitance (Ta = 25 °C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0v	6 pF

Note: [1]This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 8: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}	Endurance	1,000 & 10,000[2]	Cycles	MIL-STD-883, Method 1033
T_{DR}[1]	Data Retention	100	Years	MIL-STD-883, Method 1008
V_{ZAP_HBM}[1]	ESD Susceptibility Human Body Model	1000	Volts	JEDEC Stadard A114
V_{ZAP_MM}[1]	ESD Susceptibility Machine Model	200	Volts	JEDEC
I_{LTH}[1]	Latch Up	100	mA	JEDEC Standard 17

Note: [1]This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

[2]See Ordering Information for desired type.

AC Characteristics

Table 9: Read Cycle Timing Parameters

Symbol	Parameter	29VE010-200		29VE010-250		Units
		Min	Max	Min	Max	
T_{RC}	Read Cycle time	200		250		ns
T_{CE}	Chip Enable Access Time		200		250	ns
T_{AA}	Address Access Time		200		250	ns
T_{OE}	Output Enable Access Time		100		120	ns
T_{CLZ}[1]	CE# Low to Active Output	0		0		ns
T_{OLZ}[1]	OE# Low to Active Output	0		0		ns
T_{CHZ}[1]	CE# High to High-Z Output		50		50	ns
T_{OHZ}[1]	OE# High to High-Z Output		50		50	ns
T_{OH}[1]	Output Hold from Address Change	0		0		ns

Table 10: Page-Write Cycle Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{WC}	Write Cycle (erase and program)		10	ms
T_{AS}	Address Setup Time	0		ns
T_{AH}	Address Hold Time	50		ns
T_{CS}	WE# and CE# Setup Time	0		ns
T_{CH}	WE# and CE# Hold Time	0		ns
T_{OES}	OE# High Setup Time	0		ns
T_{OEH}	OE# High Hold Time	0		ns
T_{CP}	CE# Pulse Width	70		ns
T_{WP}	WE# Pulse Width	70		ns
T_{DS}	Data Setup Time	35		ns
T_{DH}	Data Hold Time	0		ns
T_{BLC}[1]	Byte Load Cycle Time	0.05	100	µs
T_{BLCO}[1]	Byte Load Cycle Time	200		µs
T_{IDA}	Software ID Access and Exit Time		10	µs
T_{SCE}	Software Chip Erase		20	ms

Note: [1]This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.

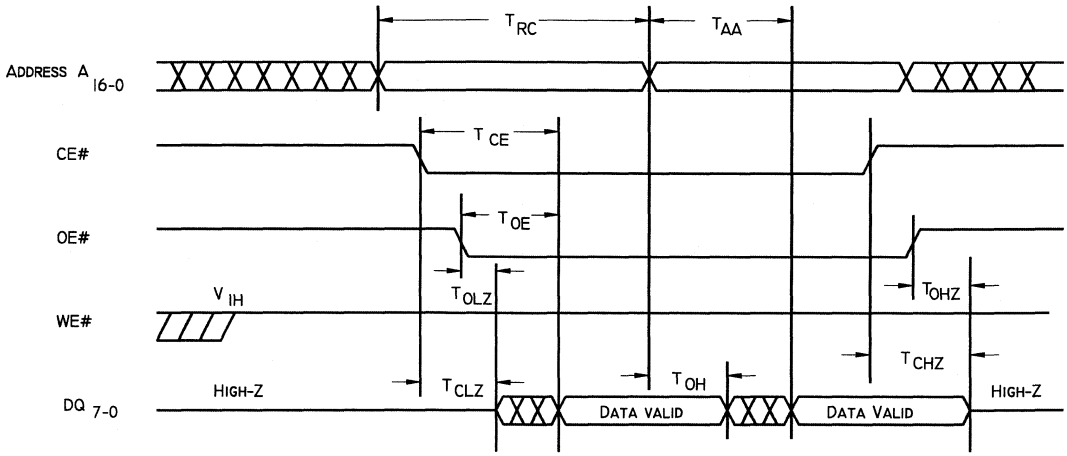


Figure 3: Read Cycle Timing Diagram

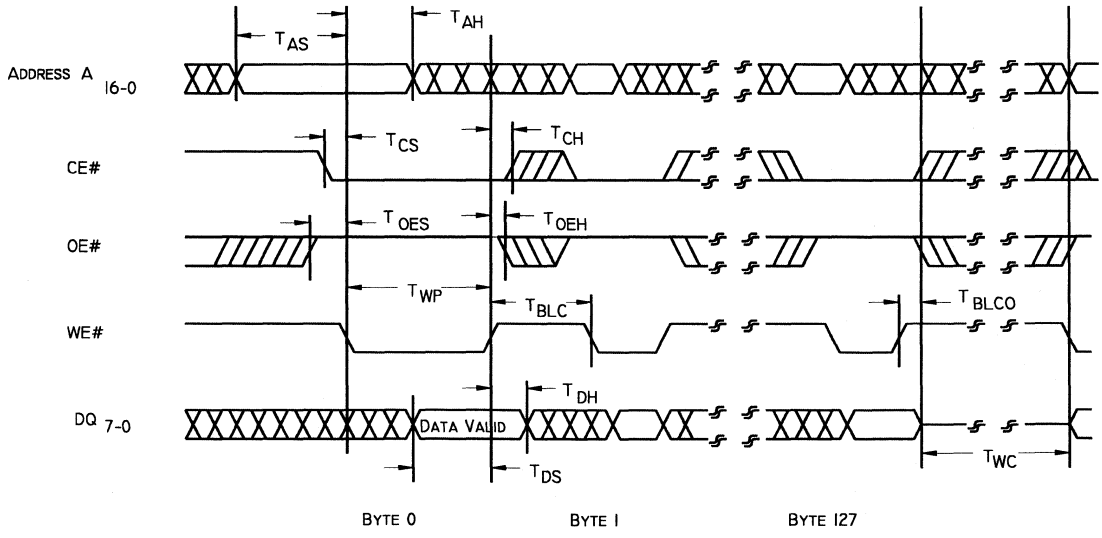


Figure 4: WE# Controlled Page Write Cycle Timing Diagram

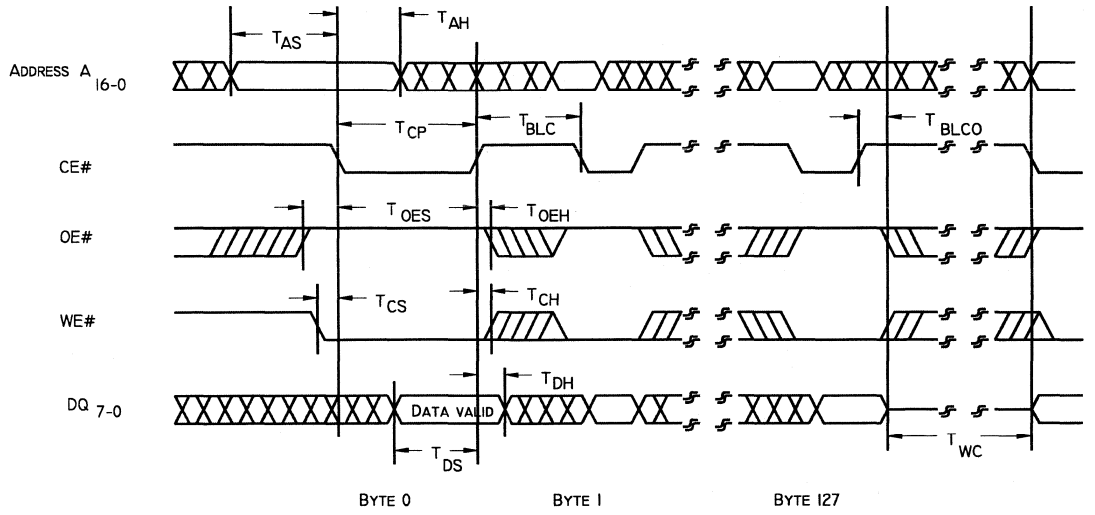


Figure 5: CE# Controlled Page Write Cycle Timing Diagram

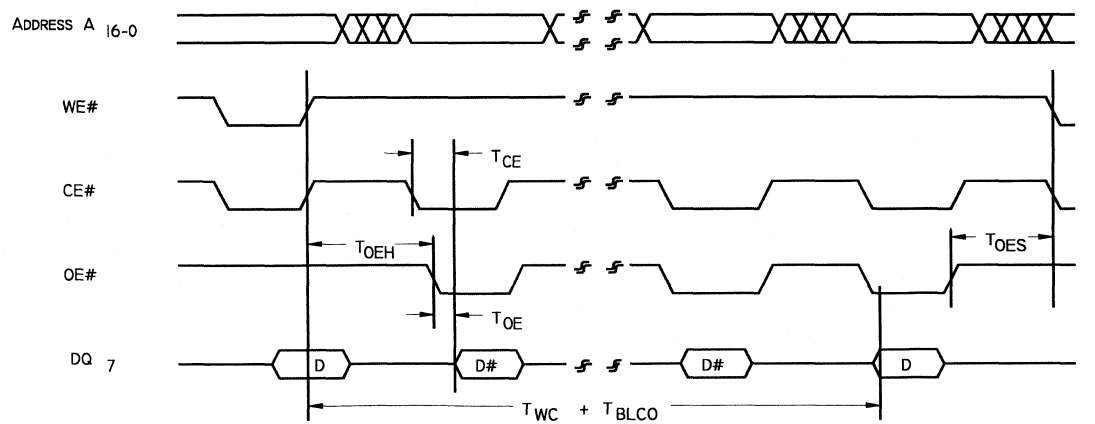


Figure 6: Data# Polling Timing Diagram

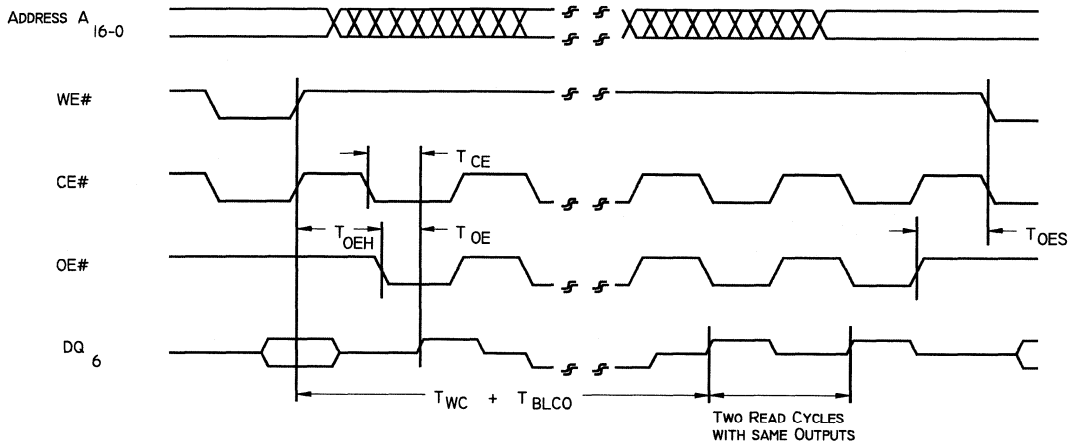
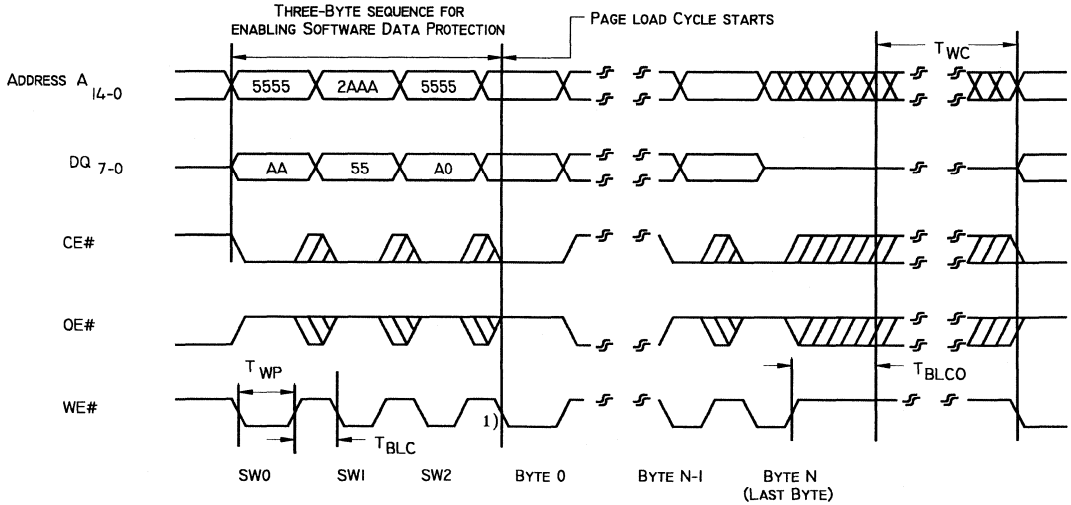


Figure 7: Toggle Bit Timing Diagram



NOTE 1): THE TIME BETWEEN ENABLING SOFTWARE DATA PROTECT AND THE PAGE LOAD MUST BE LESS THAN T_{BLCO}

Figure 8: Software Data Protection Page Write Timing Diagram

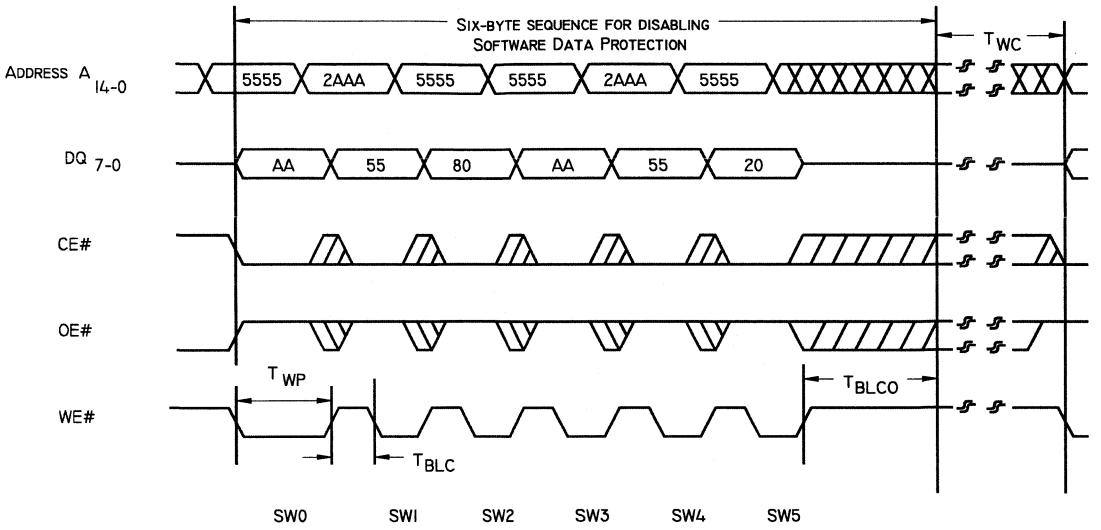


Figure 9: Software Data Protect Disable Timing Diagram

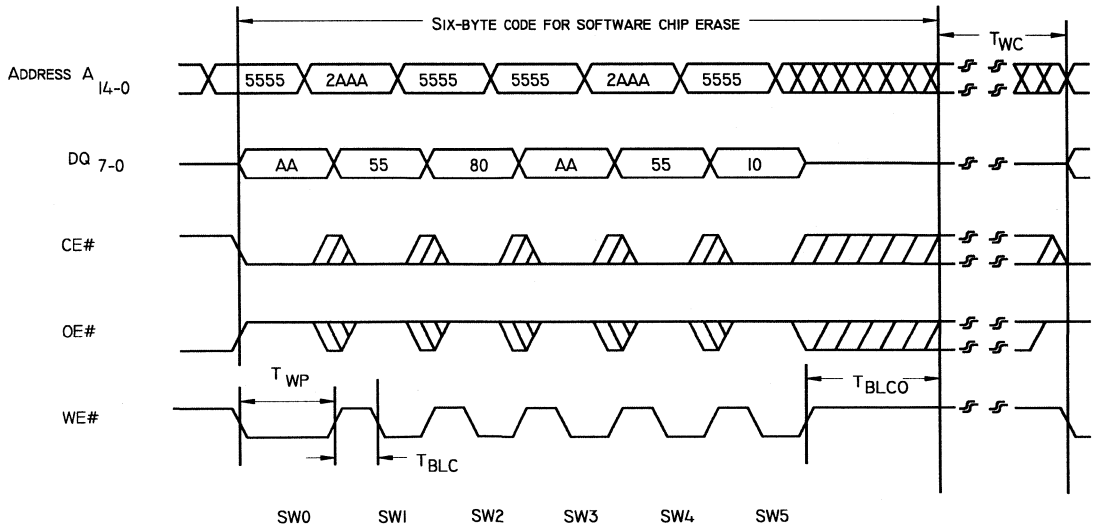


Figure 10: Software Chip Erase Timing Diagram

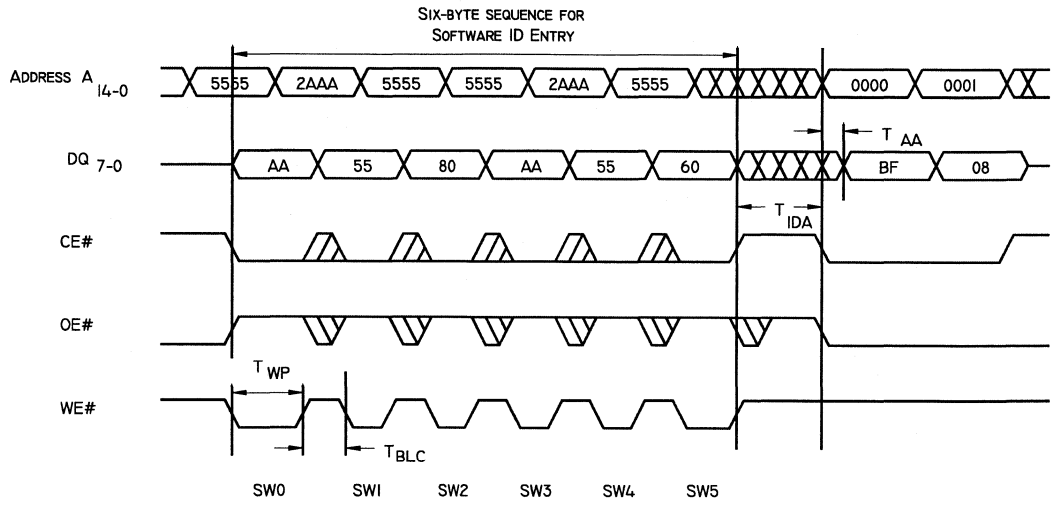


Figure 11: Software ID Entry and Read

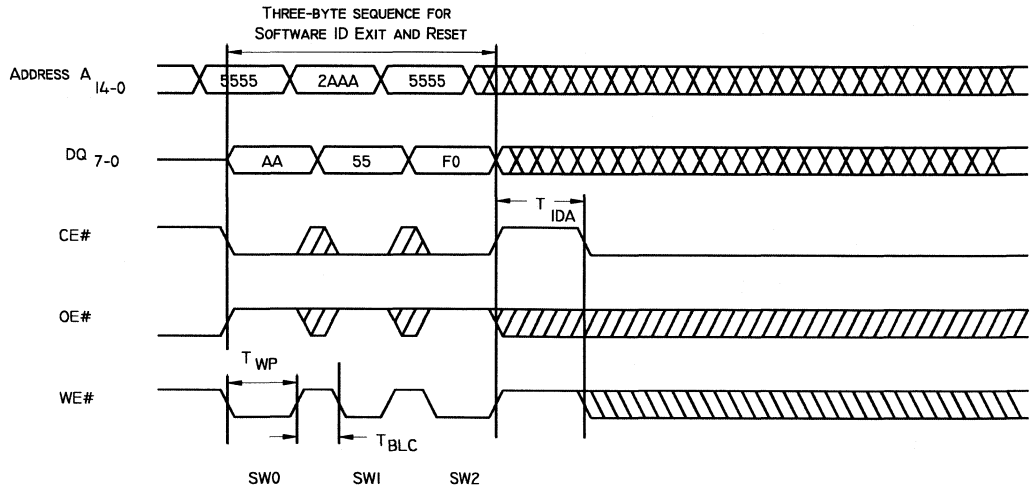
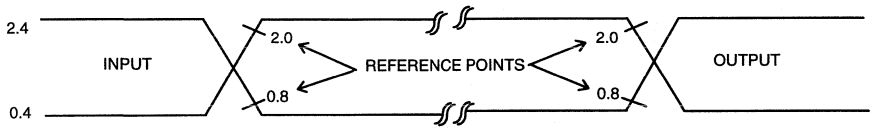


Figure 12: Software ID Exit and Reset



AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a logic "1" and V_{OL} (0.4 V_{TTL}) for a logic "0". Measurement reference points for inputs and outputs are V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Inputs rise and fall times (10% ↔ 90%) are <10 ns.

Figure 13: AC Input/Output Reference Waveforms

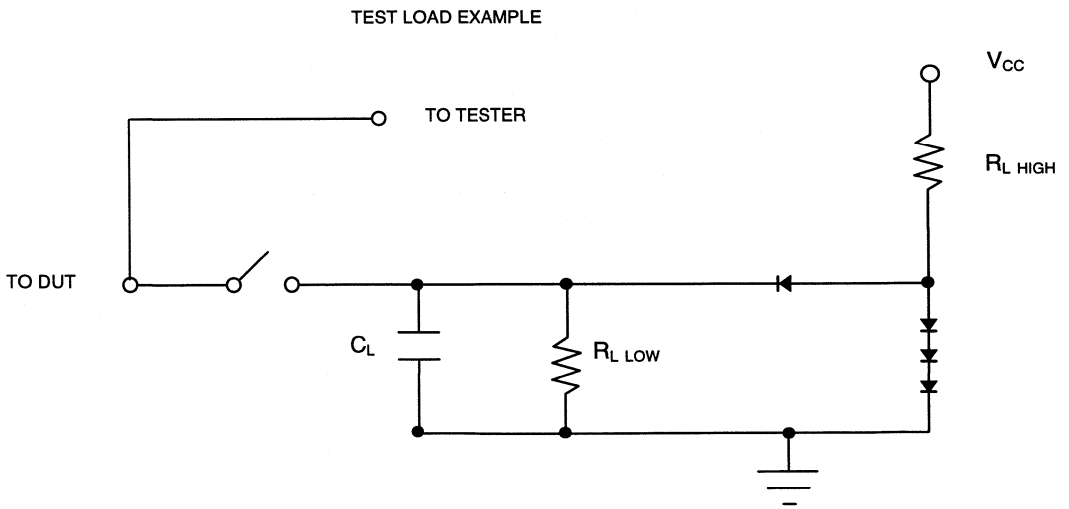


Figure 14: Test Load Example

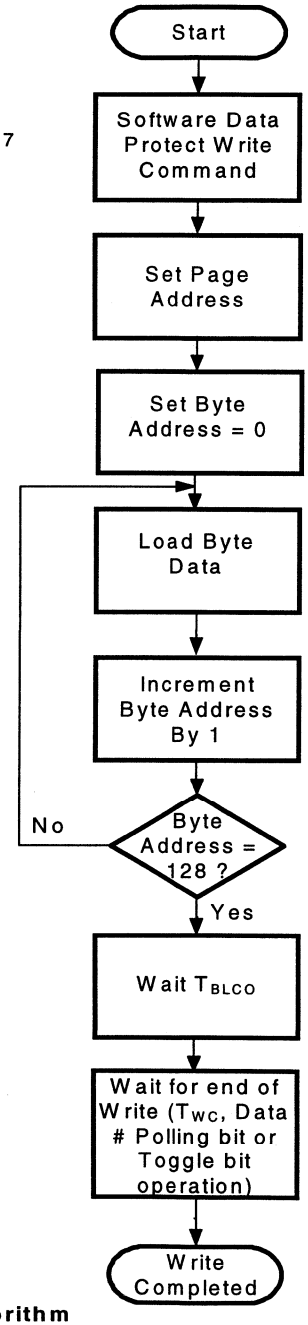


Figure 15: Write Algorithm

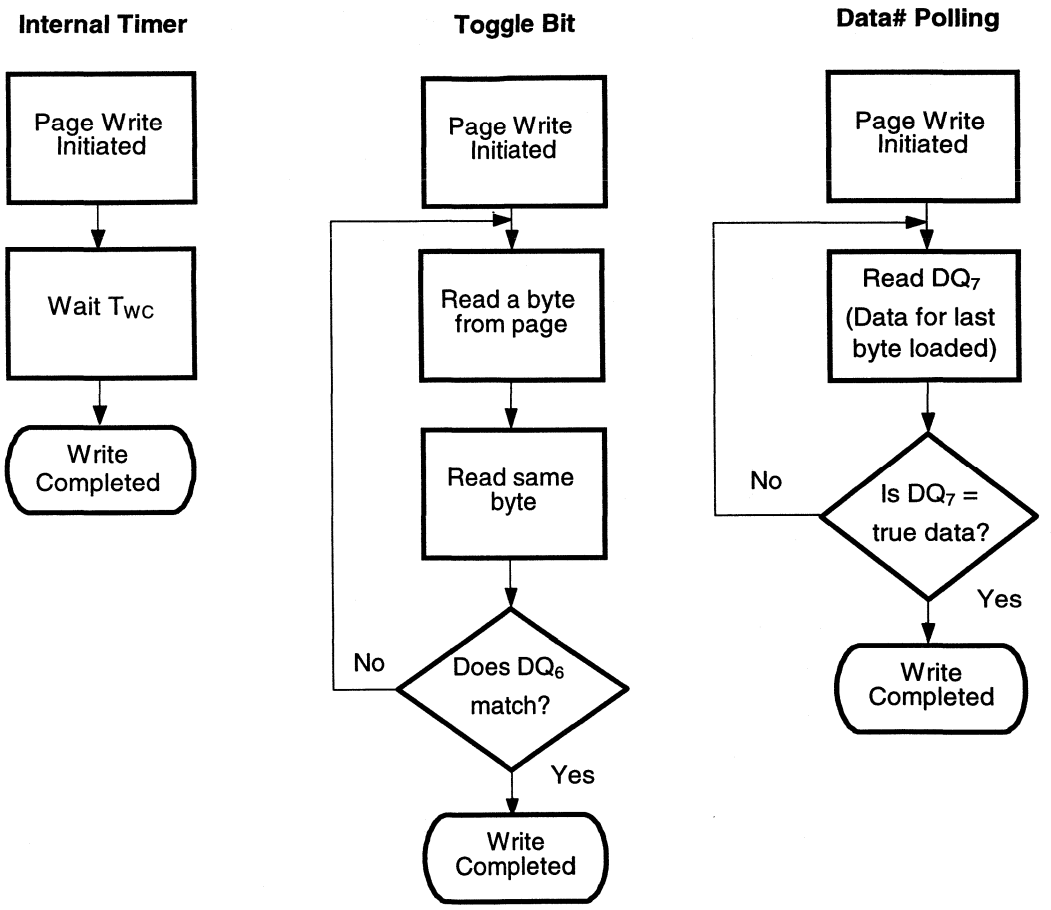


Figure 16: Wait Options

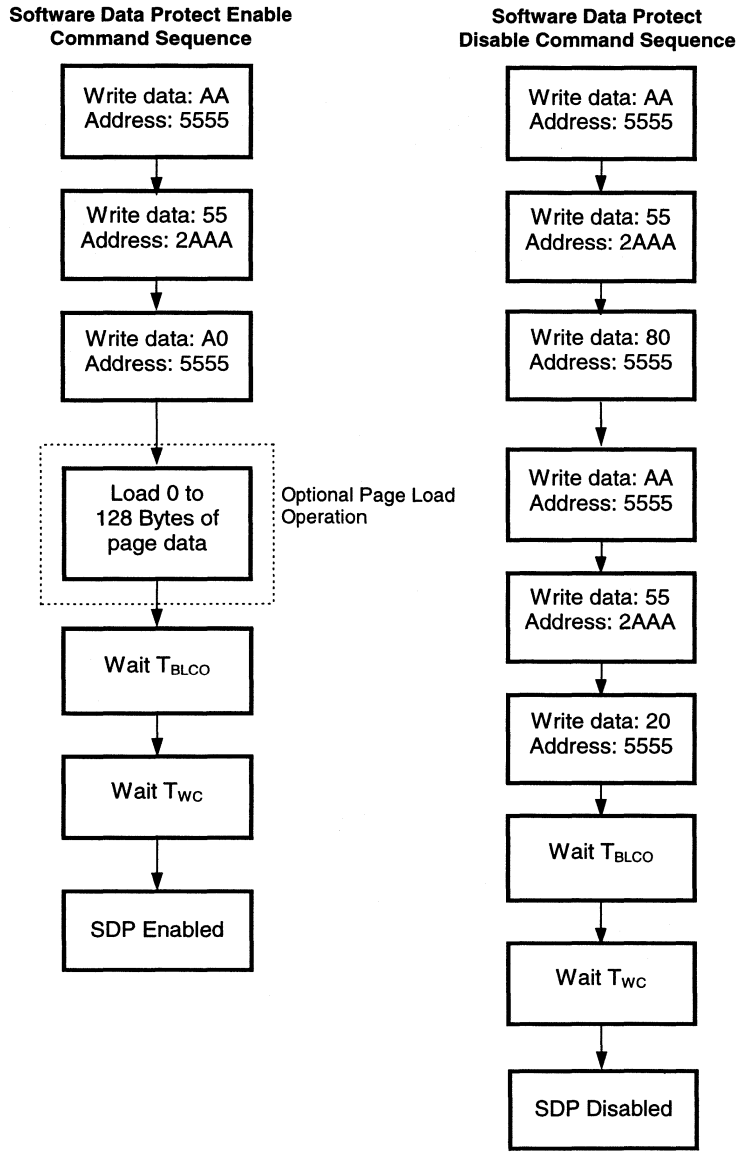


Figure 17: Software Data Protection Flowcharts

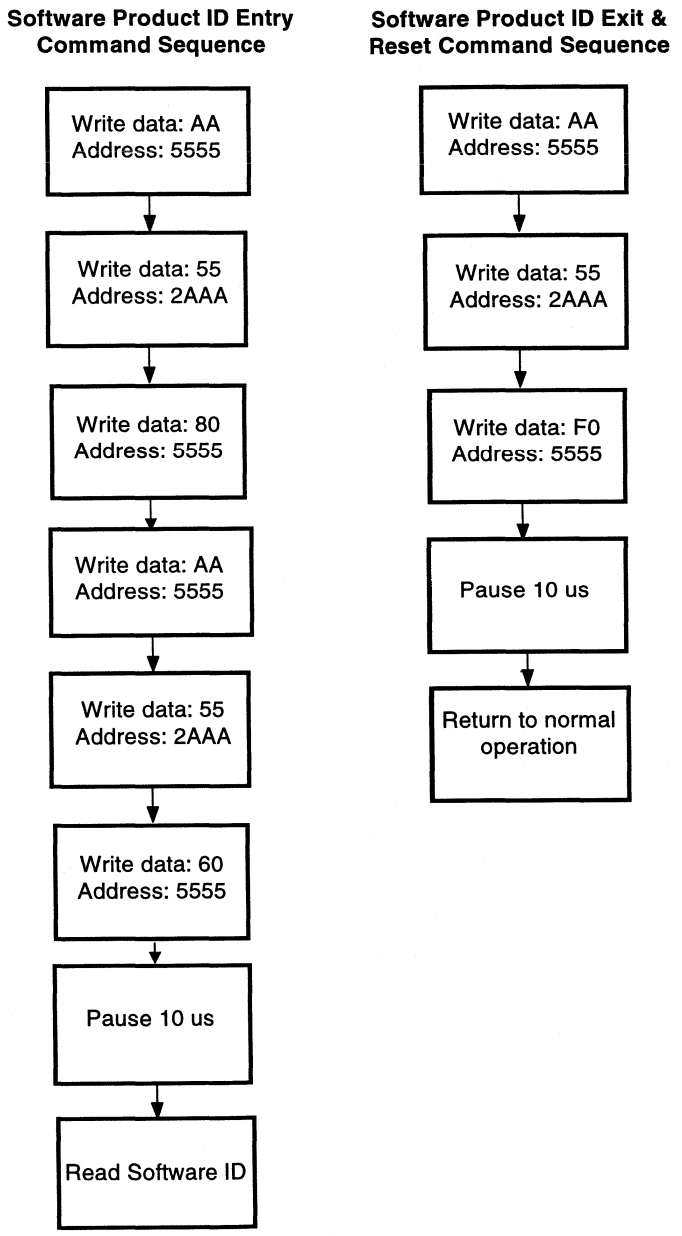


Figure 18: Software Product Command Flowcharts

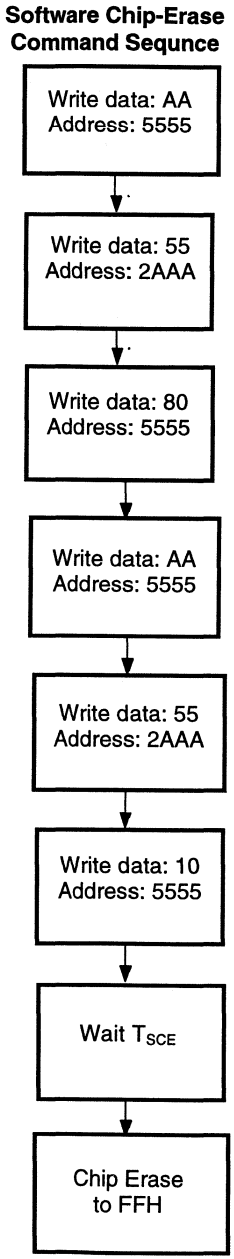
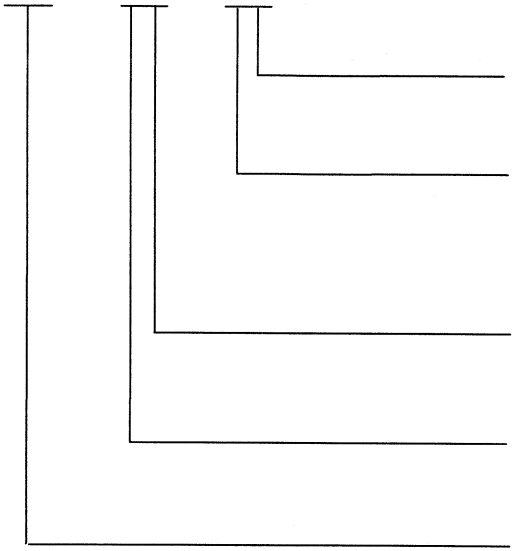


Figure 19: Software Chip Erase Command Codes

Product Ordering Information

Device		Speed		Suffix1		Suffix2
SST29VE010	-	XXX	-	XX	-	XX



Package Modifier
H = 32 leads
Numeric = Die modifier

Package Type
P = PDIP
N = PLCC
E = TSOP (die up)
U = Unencapsulated die

Operating Temperature
C = Commercial = 0° to 70°C
I = Industrial = -40° to 85°C

Minimum Endurance
3 = 1000 cycles
4 = 10,000 cycles

Read Access Speed
200 = 200 ns
250 = 250 ns

Valid combinations

SST29VE010-200-4C- EH	SST29VE010-200-4C- NH	SST29VE010-200-4C- PH
SST29VE010-250-4C- EH	SST29VE010-250-4C- NH	SST29VE010-250-4C- PH
SST29VE010-200-3C- EH	SST29VE010-200-3C- NH	SST29VE010-200-3C- PH
SST29VE010-250-3C- EH	SST29VE010-250-3C- NH	SST29VE010-250-3C- PH
SST29VE010-200-4I-EH	SST29VE010-200-4I-NH	
SST29VE010-250-4I-EH	SST29VE010-250-4I-NH	SST29VE010-250-4C-U1
SST29VE010-200-3I-EH	SST29VE010-200-3I-NH	
SST29VE010-250-3I-EH	SST29VE010-250-3I-NH	SST29VE010-250-3C-U1

Example: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Data Sheet

SST 29EE020
5.0V-only 2 Megabit
Page Mode EEPROM

July 1996

SST 29EE020
5.0V-only 2 Megabit
Page Mode EEPROM

Features:

Single 5.0-Volt Read and Write Operations
CMOS SuperFlash EEPROM Technology
- Endurance: 100,000 Cycles (typical)
- Greater than 100 years Data Retention

Low Power Consumption:
- Active Current: 20 mA (typical)
- Standby Current: 10 µA (typical)

Fast Page-Write Operation
- 128 Bytes per Page, 2048 Pages
- Page-Write Cycle: 5 ms (typical)
- Complete Memory Rewrite: 10 sec (typical)
- Effective Byte-write Cycle Time: 39 µs (typical)

Fast Access Time: 120 and 150 ns

Latched Address and Data
Automatic Write Timing with Internal V_{pp} Generation
End of Write Detection
- Toggle Bit
- Data# Polling

Hardware and Software Data Protection
TTL I/O Compatibility
JEDEC Standard Byte-wide EEPROM Pinouts
Packages Available
- 32-Pin TSOP
- 32-Lead PLCC
- 32-Pin Plastic DIP

Product Description

The 29EE020 is a 256K x 8 CMOS page mode EEPROM manufactured with SST's proprietary, high performance CMOS SuperFlash technology. The split gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The 29EE020 writes with a 5.0-volt-only power supply. Internal erase/program is transparent to the user. The 29EE020 conforms to JEDEC standard pinouts for byte-wide memories.

Featuring high performance page write, the 29EE020 provides a typical byte-write time of 39 µsec. The entire memory, i.e., 256K bytes, can be written page by page in as little as 10 seconds, when using interface features such as Toggle Bit or Data# Polling to indicate the completion of a write cycle. To protect against inadvertent write, the 29EE020 has on-chip hardware and software data protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, the 29EE020 is offered with a guaranteed page-write endurance of 10^4 or 10^3 cycles. Data retention is rated at greater than 100 years.

The 29EE020 is suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, the 29EE020 significantly improves performance and reliability, while lowering power consumption, when compared with floppy disk or EPROM approaches. The 29EE020 improves flexibility while lowering the cost for program, data, and configuration storage applications.

To meet high density, surface mount requirements, the 29EE020 is offered in 32-pin TSOP and 32-lead PLCC packages. A 600-mil, 32-pin PDIP package is also available. See Figures 2A and 2B for pinouts.

Device Operation

The SST page mode EEPROM offers in-circuit electrical write capability. The 29EE020 does not require separate erase and program operations. The internally timed write cycle executes both erase and program transparently to the user. The 29EE020 has industry standard optional Software Data Protection, which SST recommends always to be enabled. The 29EE020 is compatible with industry standard EEPROM pinouts and functionality.

Read

The read operation of the 29EE020 is controlled by CE# and OE#, both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the read cycle timing diagram for further details (Figure 3).

Write

The write operation consists of three steps. The first step is the optional three byte load sequence for Software Data Protection. This is an optional first step in the write operation, but highly recommended to ensure proper data integrity. Step 2 is the byte-load cycle to a page buffer of the 29EE020. Step 3 is an internally controlled write cycle for writing the data loaded in the page buffer into the memory array for nonvolatile storage. During the byte-load cycle, the addresses are latched by the falling edge of either CE# or WE#, whichever occurs last. The data is latched by the rising edge of either CE# or WE#, whichever occurs first. The internal write cycle is initiated by a timer after the rising edge of WE# or CE#, whichever occurs first. The write cycle, once initiated, will continue to completion, typically within 5 ms. See Figures 4 and 5 for WE# and CE# controlled page write cycle timing diagrams and Figures 15 and 17 for flowcharts.

The write operation has three functional cycles: the optional Software Data Protection load sequence, the page load cycle and the internal write cycle. The Software Data Protection consists of a specific three byte load sequence that will leave the 29EE020 protected at the end of the page write. The page load cycle consists of loading 1 to 128 bytes of data into the page buffer. The internal write cycle consists of the T_{BLCO} time-out and the write timer operation. During the write operation, the only valid reads are Data# Polling and Toggle Bit.

The page-write operation allows the loading of up to 128 bytes of data into the page buffer of the 29EE020 before the initiation of the internal write cycle. During the internal write cycle, all the data in the page buffer is written simultaneously into the memory array. Hence, the page-write feature of 29EE020 allows the entire memory to be written in as little as 10 seconds. During the internal write cycle, the host is free to perform additional tasks, such as to fetch data from other locations in the system to set up the write to the next page. In each page-write operation, all the bytes that are loaded into the page buffer must have the same page address, i.e., A_7 through A_{17}. Any byte not loaded with user data will be written to FF.

See Figures 4, 5, and 8 for the page-write cycle timing diagrams. If after the initial byte-load cycle, the host loads a second byte into the page buffer within a byte-load cycle time (T_{BLC}) of 100 µs, the 29EE020 will stay in the page load cycle. Additional bytes are then loaded consecutively. The page load cycle will be terminated if no additional byte is loaded into the page buffer within 200 µs (T_{BLCO}) from the last byte-load cycle, i.e., no subsequent WE# or CE# high-to-low transition after the last rising edge of WE# or CE#. Data in the page buffer can be changed by a subsequent byte-load cycle. The page load period can continue indefinitely, as long as the host continues to load the device within the byte-load cycle time of 100 µs. The page to be loaded is determined by the page address of the last byte loaded.

Software Chip-Erase

The 29EE020 provides a chip-erase operation, which allows the user to simultaneously clear the entire memory array to the "1" state. This is useful when the entire device must be quickly erased.

The Software Chip-Erase operation is initiated by using a specific six byte-load sequence. After the load sequence, the device enters into an internally timed cycle similar to the write cycle. During the erase operation, the only valid read is Toggle Bit. See Table 4 for the load sequence, Figure 10 for timing diagram, and Figure 19 for the flowchart.

Write Operation Status Detection

The 29EE020 provides two software means to detect the completion of a write cycle, in order to optimize the system write cycle time. The software detection includes two status bits: Data# Polling (DQ_7) and Toggle Bit (DQ_6). The end of write detection mode is enabled after the rising WE# or CE# whichever occurs first, which initiates the internal write cycle.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If

both reads are valid, then the device has completed the write cycle, otherwise the rejection is valid.

Data# Polling (DQ_7)

When the 29EE020 is in the internal write cycle, any attempt to read DQ_7 of the last byte loaded during the byte-load cycle will receive the complement of the true data. Once the write cycle is completed, DQ_7 will show true data. The device is then ready for the next operation. See Figure 6 for Data# Polling timing diagram and Figure 16 for a flowchart.

Toggle Bit (DQ_6)

During the internal write cycle, any consecutive attempts to read DQ_6 will produce alternating 0's and 1's, i.e., toggling between 0 and 1. When the write cycle is completed, the toggling will stop. The device is then ready for the next operation. See Figure 7 for Toggle Bit timing diagram and Figure 16 for a flowchart. The intial read of the Toggle Bit will be a "1".

Data Protection

The 29EE020 provides both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a write cycle.

V_{CC} Power Up/Down Detection: The write operation is inhibited when V_{CC} is less than 2.5V.

Write Inhibit Mode: Forcing OE# low, CE# high, or WE# high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down.

Software Data Protection (SDP)

The 29EE020 provides the JEDEC approved optional software data protection scheme for all data alteration operations, i.e., write and chip erase. With this scheme, any write operation requires the inclusion of a series of three byte-load operations to precede the data loading operation. The three byte-load sequence is used to initiate the write cycle, providing optimal protection from inadvertent write operations, e.g., during the system power-up or power-down. The 29EE020 is shipped with the software data protection disabled.

The software protection scheme can be enabled by applying a three-byte sequence to the device, during a page-load cycle (Figure 8). The device will then be automatically set into the data protect mode. Any subsequent write operation will require the preceding three-byte sequence. See Table 4 for the specific software command codes and Figure 8 for the timing diagram. To set the device into the unprotected mode, a six-byte sequence is required. See Table 4 for the specific codes and Figure 9 for the timing diagram. If a write is attempted while SDP is enabled the device will be in a non-accessible state for ~ 300 µs. SST recommends Software Data Protection always be enabled. See Figure 17 for flowcharts.

The 29EE020 Software Data Protection is a global command, protecting all pages in the entire memory array once enabled (or disabled). Therefore using SDP for a single page write will enable SDP for the entire array. Single pages by themselves cannot be SDP enabled or disabled.

Single power supply reprogrammable nonvolatile memories may be unintentionally altered. SST strongly recommends that Software Data Protection (SDP) always be enabled. The 29EE020 should be programmed using the SDP command sequence. SST recommends the SDP Disable Command Sequence not be issued to the device prior to writing.

Product Identification

The product identification mode identifies the device as the 29EE020 and manufacturer as SST. This mode may be accessed by hardware or software operations. The hardware operation is typically used by a programmer to identify the correct algorithm for the 29EE020. Users may wish to use the software product identification operation to identify the part (i.e., using the device code) when using multiple manufacturers in the same socket. For details, see Table 3 for hardware operation or Table 4 for software operation, Figure 11 for the software ID entry and read timing diagram and Figure 18 for the ID entry command sequence flowchart. The manufacturer and device codes are the same for both operations.

Table 1: Product Identification Table

	Byte	Data
Manufacturers Code	0000 H	BF H
Device Code	0001 H	10 H

Product Identification Mode Exit

In order to return to the standard read mode, the Software Product Identification mode must be exited. Exiting is accomplished by issuing the Software ID Exit (reset) operation, which returns the device to the read operation. The reset operation may also be used to reset the device to the read mode after an inadvertent transient condition that apparently causes the device to behave abnormally, e.g., not read correctly. See Table 4 for software command codes, Figure 12 for timing wavefrom and Figure 18 for a flowchart.

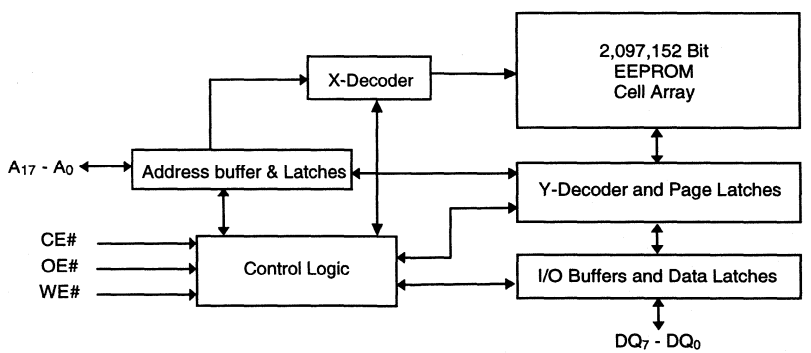


Figure 1: Functional Block Diagram of SST 29EE020

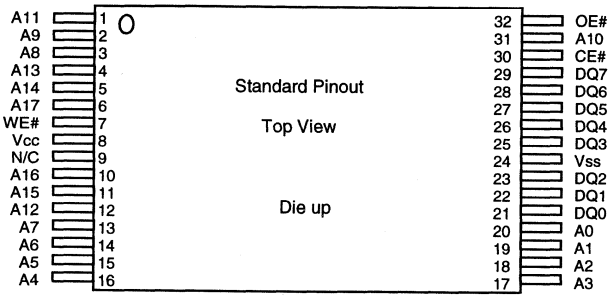


Figure 2A: Pin Assignments for 32-pin TSOP Packages

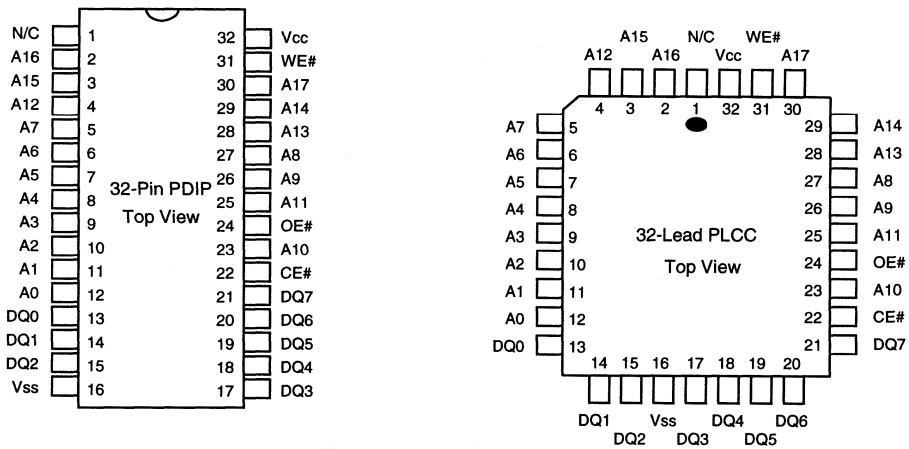


Figure 2B: Pin Assignments for 32-pin Plastic DIPs and 32-lead PLCCs

Table 2: Pin Description

Symbol	Pin Name	Functions
A_{17}-A_7	Row Address Inputs	To provide memory addresses. Row addresses define a page for a write cycle.
A_6-A_0	Column Address Inputs	Column Addresses are toggled to load page data.
DQ_7-DQ_0	Data Input/output	To output data during read cycles and receive input data during write cycles. Data is internally latched during a write cycle. The outputs are in tri-state when OE# or CE# is high.
CE#	Chip Enable	To activate the device when CE# is low.
OE#	Output Enable	To gate the data output buffers.
WE#	Write Enable	To control the write operations
Vcc	Power Supply	To provide 5-volt supply (± 10%)
Vss	Ground	
NC	No Connection	Unconnected pins.

Table 3: Operation Modes Selection

Mode	CE#	OE#	WE#	DQ	Address
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	A_{IN}
Page Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}
Standby	V_{IH}	X	X	High Z	X
Write Inhibit	X	V_{IL}	X	High Z/ D_{OUT}	X
Write Inhibit	X	X	V_{IH}	High Z/ D_{OUT}	X
Software Chip Erase	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}, See Table 4
Product Identification					
Hardware Mode	V_{IL}	V_{IL}	V_{IH}	Manufacturer Code (BF)	A_{17} - A_1 = V_{IL}, A_9 = V_H, A_0 = V_{IL}
				Device Code (10)	A_{17} - A_1 = V_{IL}, A_9 = V_H, A_0= V_{IH}
Software Mode	V_{IL}	V_{IH}	V_{IL}		See Table 4
SDP Enable Mode	V_{IL}	V_{IH}	V_{IL}		See Table 4
SDP Disable Mode	V_{IL}	V_{IH}	V_{IL}		See Table 4

Table 4: Software Command Codes

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data
Software Data Protect Enable & Page Write	5555H	AAH	2AAAH	55H	5555H	A0H	Addr[2]	Data				
Software Data Protect Disable	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	20H
Software Chip Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry	5555H	AAH	2AAAH	55H	5555H	90H						
Software ID Exit	5555H	AAH	2AAAH	55H	5555H	F0H						
Alternate Software ID Entry[3]	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	60H

Notes: (1) Address format A_{14}-A_0 (Hex), Address A_{15} is a "Don't Care".

(2) Page Write consists of loading up to 128 bytes (A_6 - A_0).

(3) Alternate 6 byte Software Product ID Command Code

Notes for Software Product ID Command Code:

1. With A_{14}-A_1 =0; SST Manufacturer Code = BFH, is read with A_0 = 0,
   29EE020 Device Code = 10H, is read with A_0 = 1.
2. The device does not remain in Software Product ID Mode if powered down.
3. This product supports both the JEDEC standard 3 byte command code sequence and SST's original 6 byte command code sequence. For new designs, SST recommends that the 3 byte command code sequence be used.

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential ..... -0.5V to V_{CC}+ 0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential ..... -1.0V to V_{CC}+ 1.0V
Voltage on A_9 Pin to Ground Potential ..... -0.5V to 14.0V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Through Hole Lead Soldering Temperature (10 Seconds) ..... 300°C
Surface Mount Lead Soldering Temperature (3 Seconds) ..... 240°C
Output Short Circuit Current[1] ..... 100 mA

Note: [1] Outputs shorted for no more than one second. No more than one output shorted at a time.

Operating Range

Range	Ambient Temp	V_{CC}
Commercial	0 °C to +70 °C	5V±10%
Industrial	-40 °C to +85 °C	5V±10%

AC Conditions of Test

Input Rise/Fall Time.....10 ns
Output Load.....1 TTL Gate and C_L = 100 pF
See Figures 13 and 14

Table 5: DC Operating Characteristics

Symbol	Parameter	Limits Min	Limits Max	Limits Units	Test Conditions
I_{CC}	Power Supply Current				CE#=OE#=V_{IL},WE#=V_{IH}, all I/Os open,
	Read		30	mA	Address input = V_{IL}/V_{IH}, at f=1/T_{RC} Min., V_{CC}=V_{CC} Max
	Write		50	mA	CE#=WE#=V_{IL}, OE#=V_{IH}, V_{CC} =V_{CC} Max.
I_{SB1}	Standby V_{CC} Current (TTL input)		3	mA	CE#=OE#=WE#=V_{IH}, V_{CC}=V_{CC} Max.
I_{SB2}	Standby V_{CC} Current (CMOS input)		50	µA	CE#=OE#=WE#=V_{CC} -0.3V. V_{CC} = V_{CC} Max.
I_{LI}	Input Leakage Current		1	µA	V_{IN} =GND to V_{CC}, V_{CC} = V_{CC} Max.
I_{LO}	Output Leakage Current		10	µA	V_{OUT} =GND to V_{CC}, V_{CC} = V_{CC} Max.
V_{IL}	Input Low Voltage		0.8	V	V_{CC} = V_{CC} Max.
V_{IH}	Input High Voltage	2.0		V	V_{CC} = V_{CC} Max.
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.1 mA, V_{CC} = V_{CC} Min.
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400µA, V_{CC} = V_{CC} Min.
V_H	Supervoltage for A_9	11.6	12.4	V	CE# = OE# =V_{IL}, WE# = V_{IH}
I_H	Supervoltage Current for A_9		200	µA	CE# = OE# = V_{IL}, WE# = V_{IH}, A_9 = V_H Max.

Table 6: Power-up Timings

Symbol	Parameter	Maximum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$[1]	Power-up to Write Operation	5	ms

Table 7: Capacitance (Ta = 25 °C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0v	6 pF

Note: [1]This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 8: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}	Endurance	1,000 & 10,000[2]	Cycles	MIL-STD-883, Method 1033
T_{DR}[1]	Data Retention	100	Years	MIL-STD-883, Method 1008
V_{ZAP_HBM}[1]	ESD Susceptibility Human Body Model	1000	Volts	JEDEC Standard A114
V_{ZAP_MM}[1]	ESD Susceptibility Machine Model	200	Volts	JEDEC
I_{LTH}[1]	Latch Up	100	mA	JEDEC Standard 17

Note: [1]This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

[2]See Ordering Information for desired type.

AC Characteristics

Table 9: Read Cycle Timing Parameters

Symbol	Parameter	29EE020-120		29EE020-150		Units
		Min	Max	Min	Max	
T_{RC}	Read Cycle time	120		150		ns
T_{CE}	Chip Enable Access Time		120		150	ns
T_{AA}	Address Access Time		120		150	ns
T_{OE}	Output Enable Access Time		50		60	ns
T_{CLZ}[1]	CE# Low to Active Output	0		0		ns
T_{OLZ}[1]	OE# Low to Active Output	0		0		ns
T_{CHZ}[1]	CE# High to High-Z Output		30		30	ns
T_{OHZ}[1]	OE# High to High-Z Output		30		30	ns
T_{OH}[1]	Output Hold from Address Change	0		0		ns

Table 10: Page-Write Cycle Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{WC}	Write Cycle (erase and program)		10	ms
T_{AS}	Address Setup Time	0		ns
T_{AH}	Address Hold Time	50		ns
T_{CS}	WE# and CE# Setup Time	0		ns
T_{CH}	WE# and CE# Hold Time	0		ns
T_{OES}	OE# High Setup Time	0		ns
T_{OEH}	OE# High Hold Time	0		ns
T_{CP}	CE# Pulse Width	70		ns
T_{WP}	WE# Pulse Width	70		ns
T_{DS}	Data Setup Time	35		ns
T_{DH}	Data Hold Time	0		ns
T_{BLC}[1]	Byte Load Cycle Time	0.05	100	µs
T_{BLCO}[1]	Byte Load Cycle Time	200		µs
T_{IDA}	Software ID Access and Exit Time		10	µs
T_{SCE}	Software Chip Erase		20	ms

Note: [1]This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.

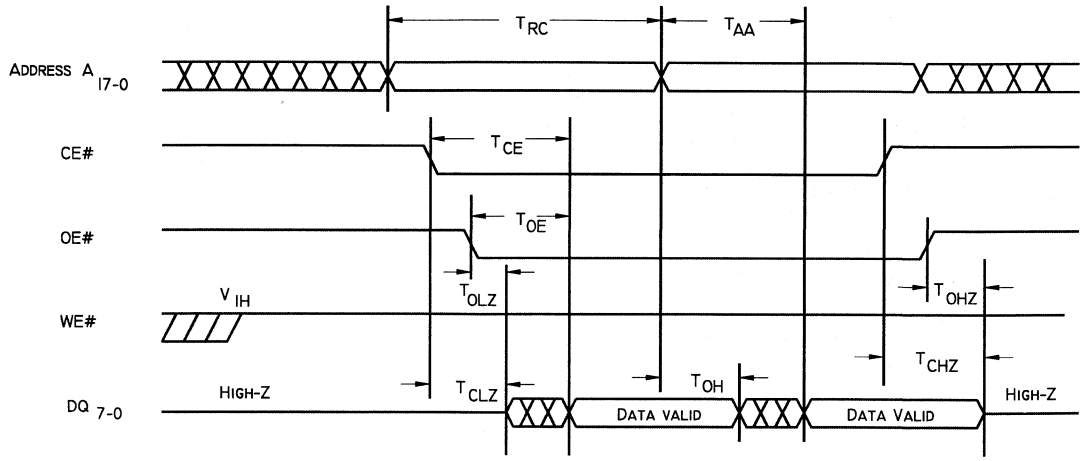


Figure 3: Read Cycle Timing Diagram

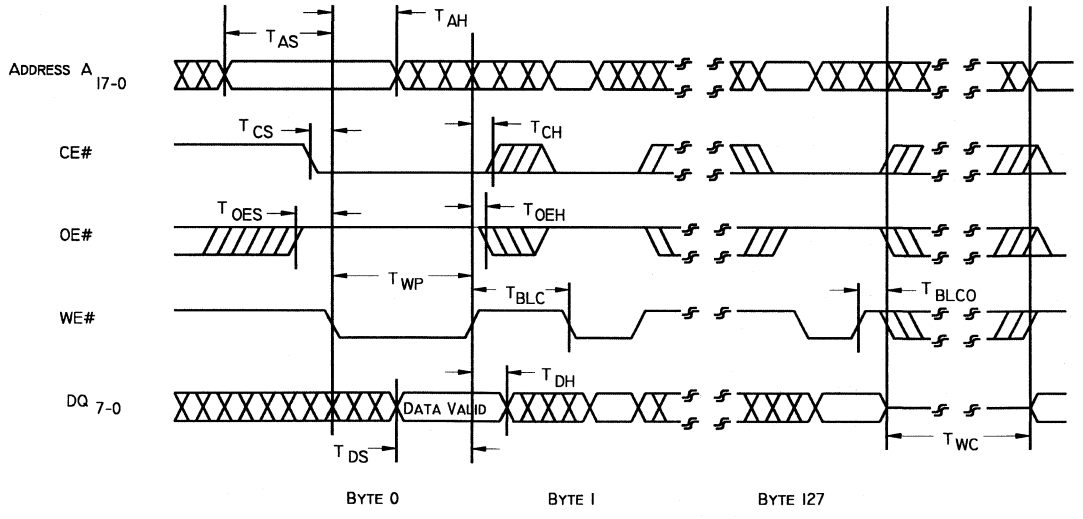


Figure 4: WE# Controlled Page Write Cycle Timing Diagram

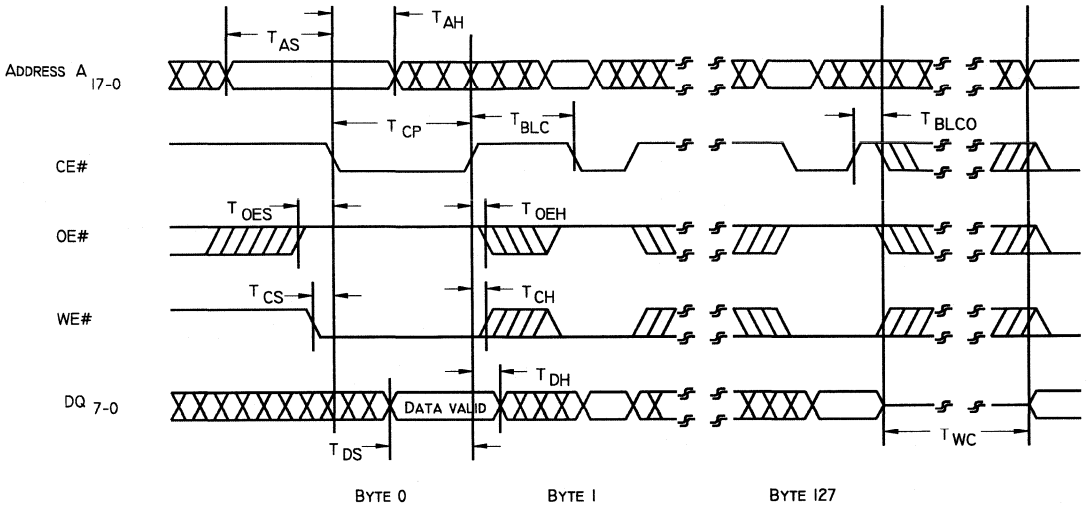


Figure 5: CE# Controlled Page Write Cycle Timing Diagram

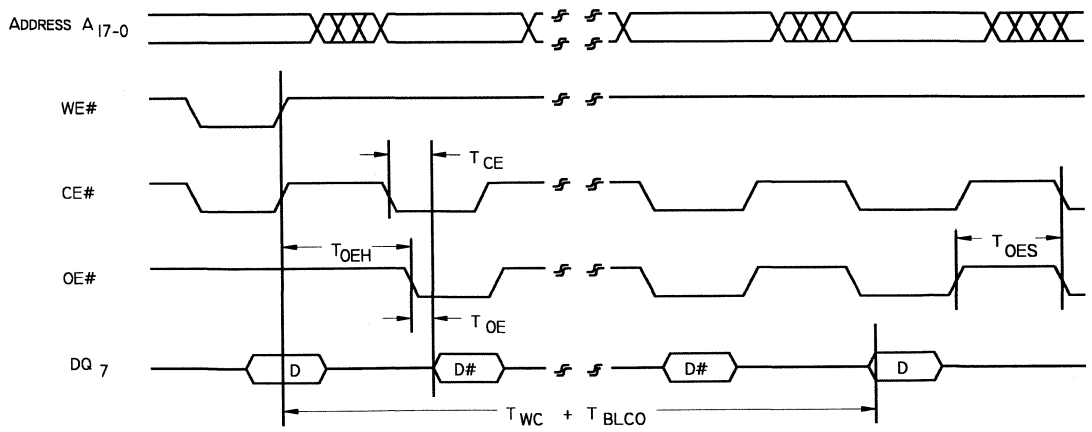
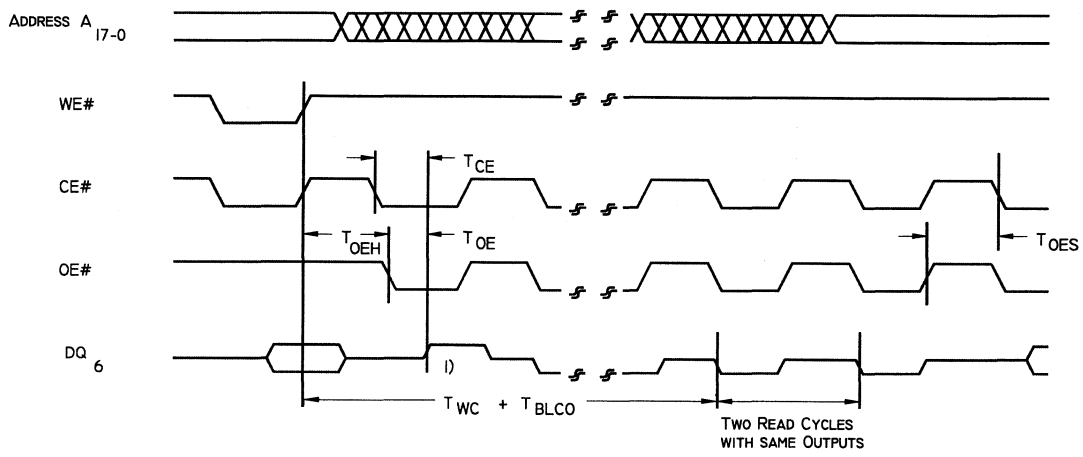
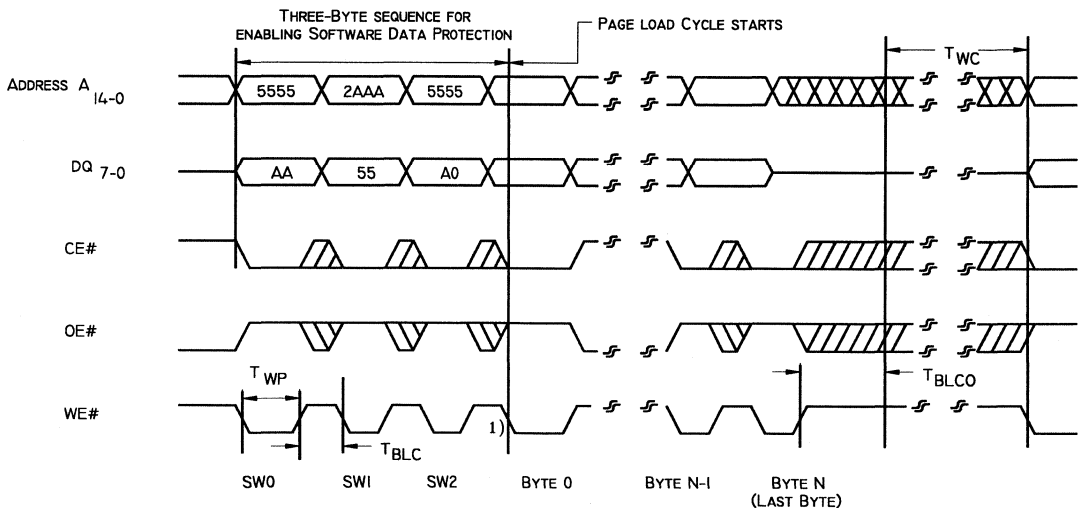


Figure 6: Data# Polling Timing Diagram



NOTE: 1) TOGGLE BIT OUTPUT IS ALWAYS HIGH FIRST.

Figure 7: Toggle Bit Timing Diagram



NOTE 1): THE TIME BETWEEN ENABLING SOFTWARE DATA PROTECT AND THE PAGE LOAD MUST BE LESS THAN T_{BLCO}

Figure 8: Software Data Protection Page Write Timing Diagram

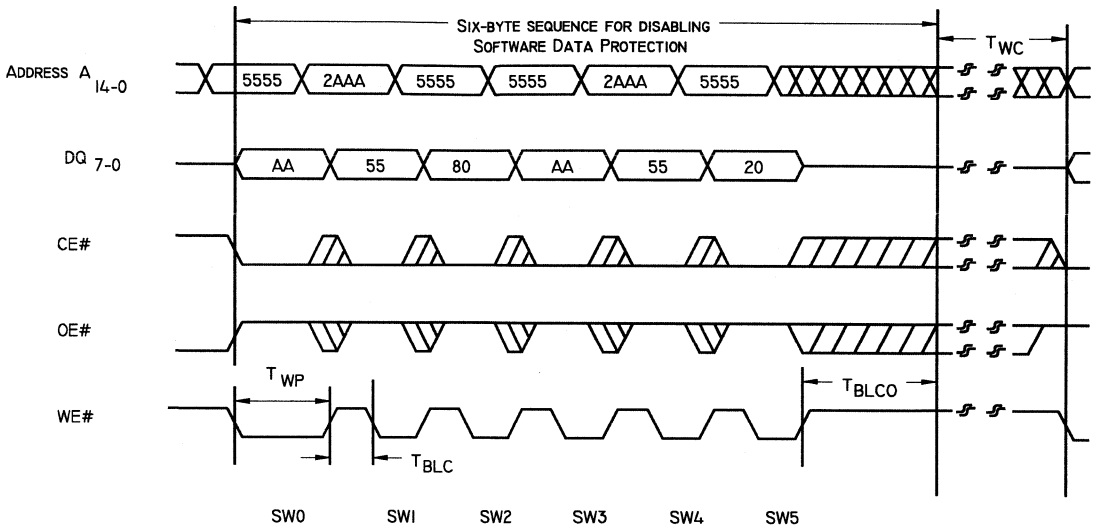


Figure 9: Software Data Protect Disable Timing Diagram

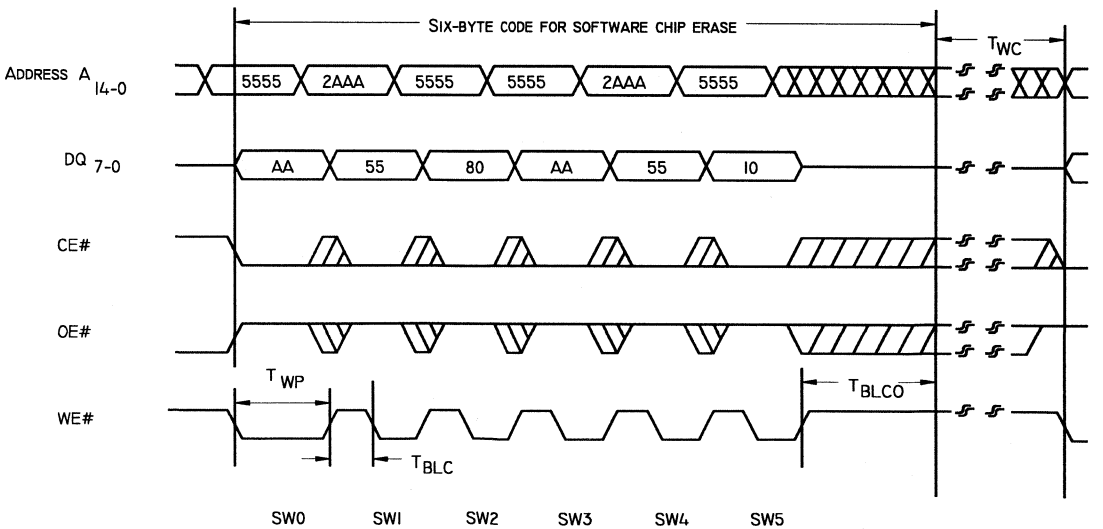


Figure 10: Software Chip Erase Timing Diagram

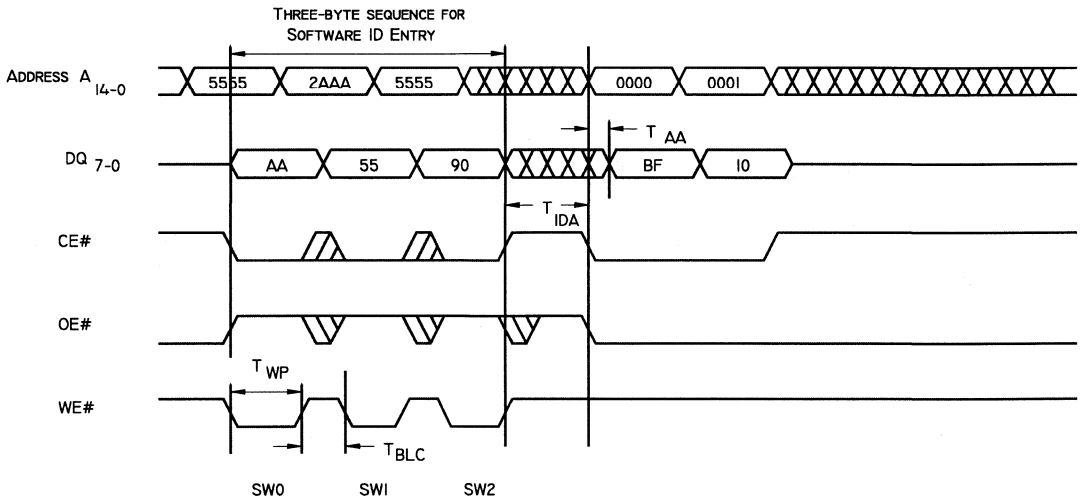


Figure 11: Software ID Entry and Read

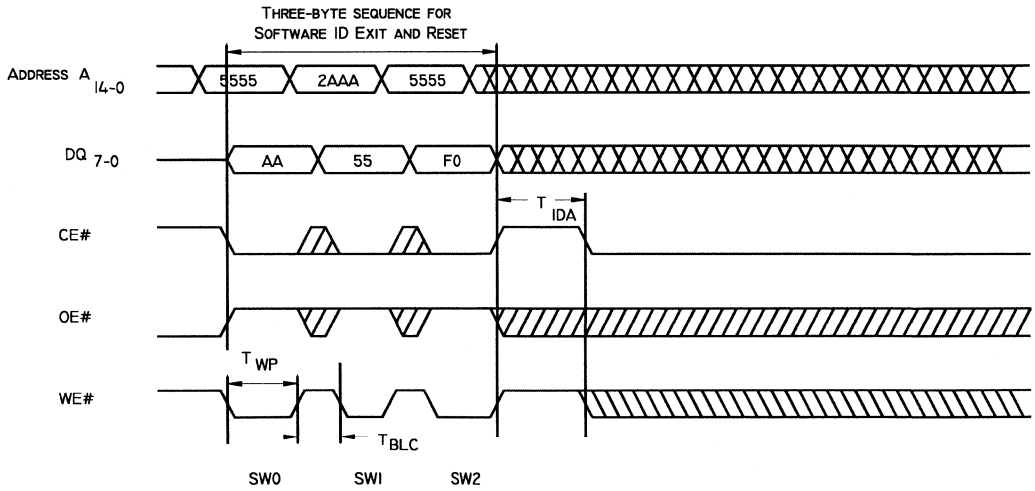
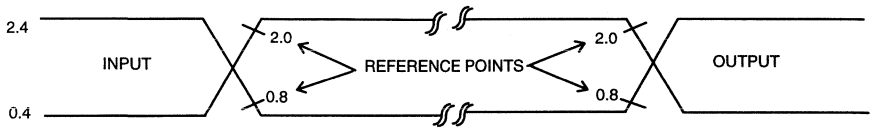


Figure 12: Software ID Exit and Reset



AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a logic "1" and V_{OL} (0.4 V_{TTL}) for a logic "0". Measurement reference points for inputs and outputs are V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Inputs rise and fall times (10% ↔ 90%) are <10 ns.

Figure 13: AC Input/Output Reference Waveforms

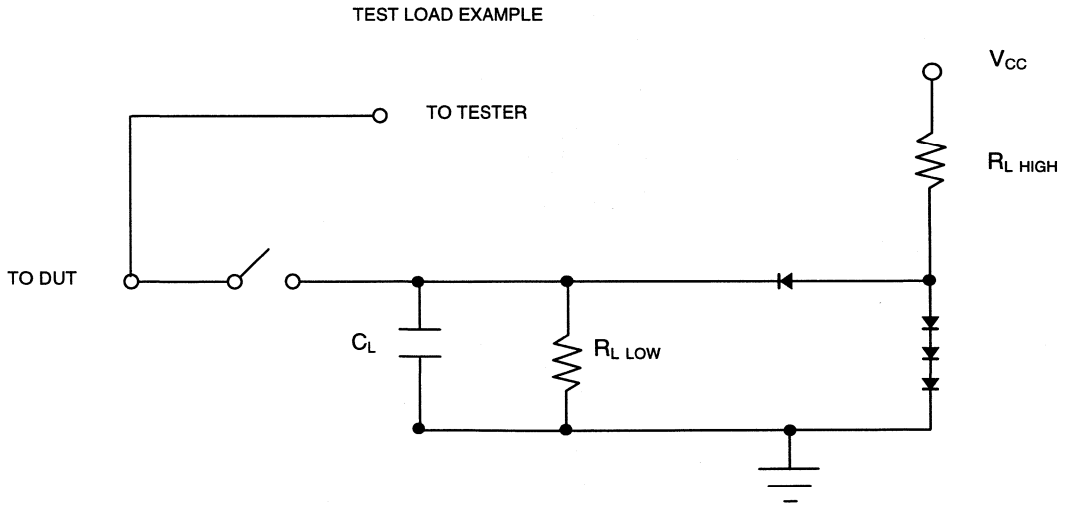


Figure 14: Test Load Example

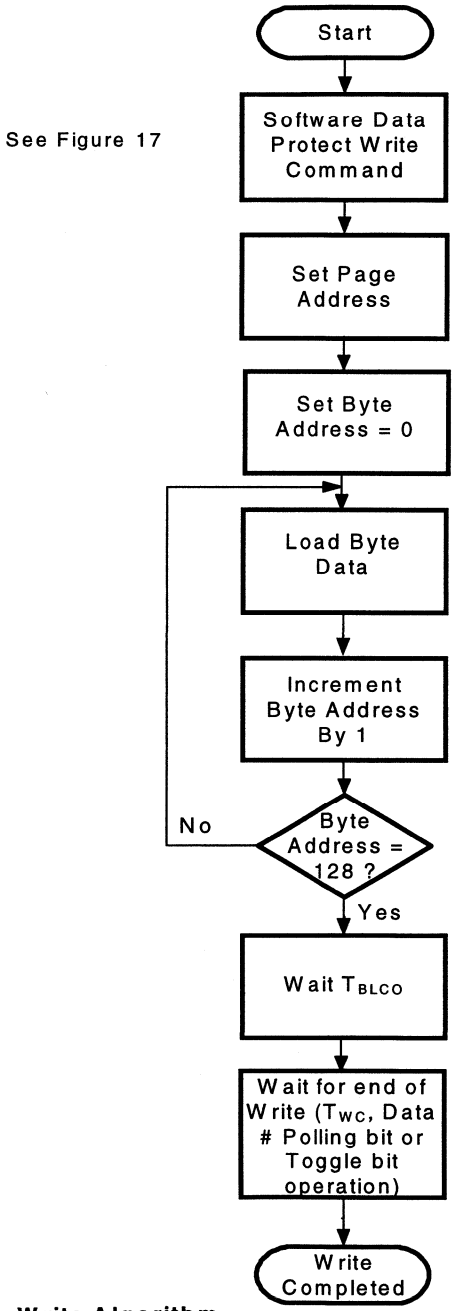


Figure 15: Write Algorithm

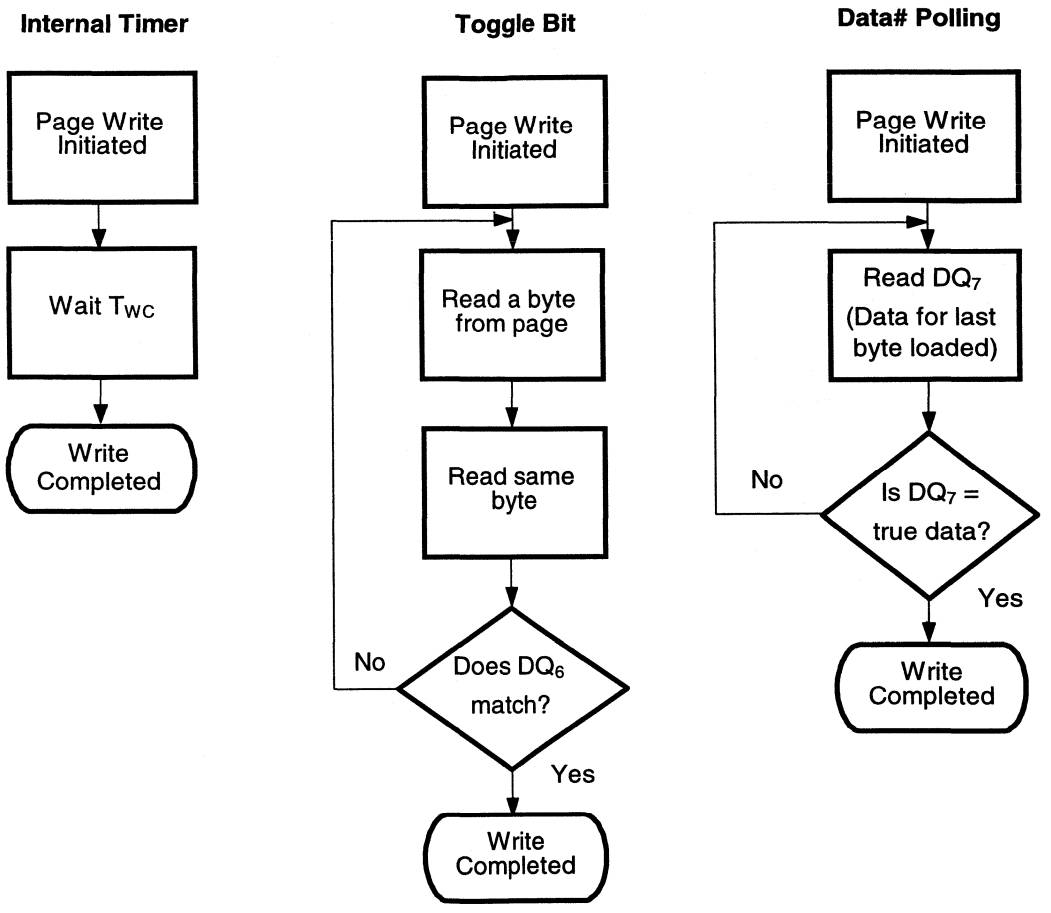


Figure 16: Wait Options

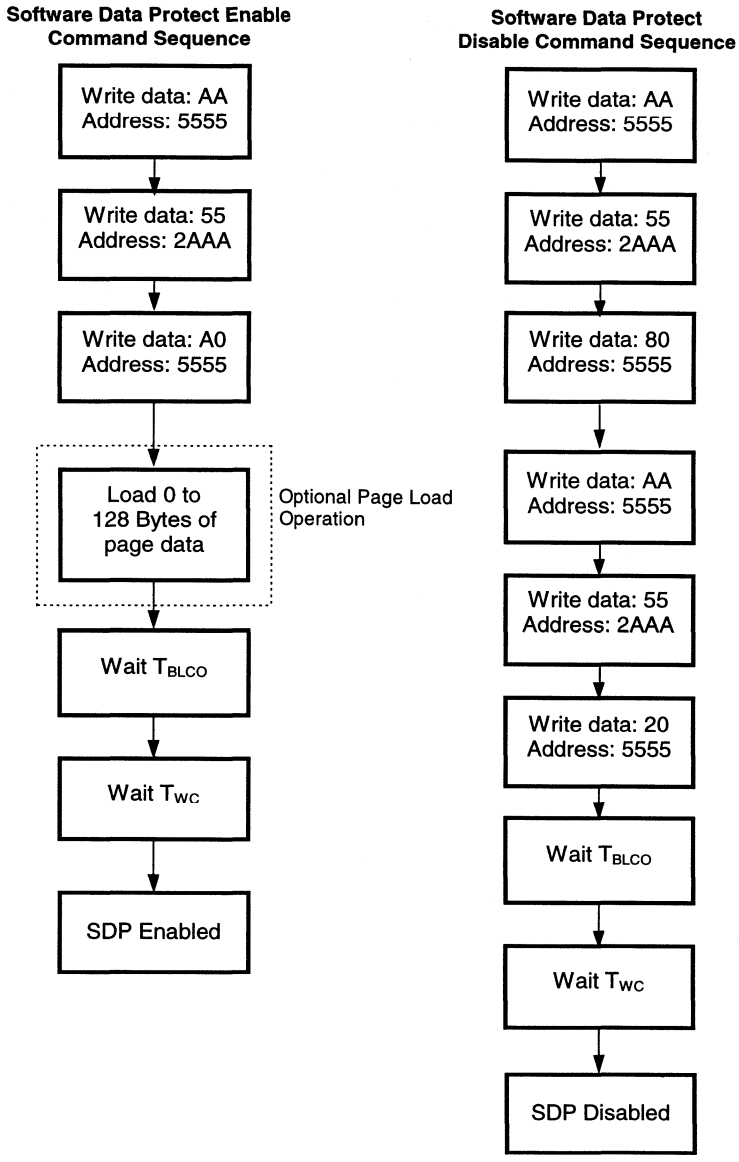


Figure 17: Software Data Protection Flowcharts

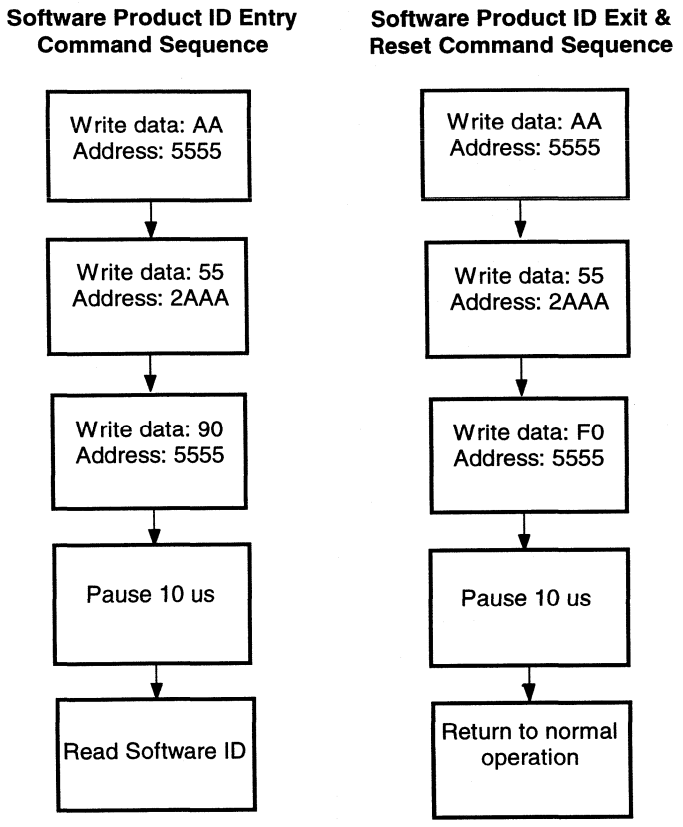


Figure 18: Software Product Command Flowcharts

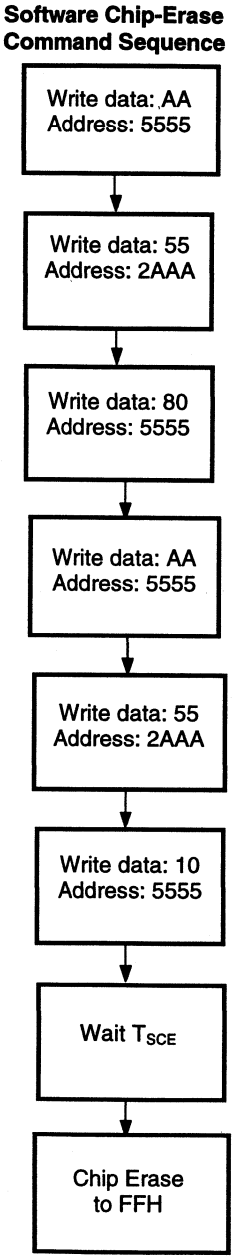


Figure 19: Software Chip Erase Command Codes

Product Ordering Information

Device **Speed** **Suffix1** **Suffix2**

SST29EE020 - XXX - XX - XX

Package Modifier
H = 32 leads
Numeric = Die modifier

Package Type
P = PDIP
N = PLCC
E = TSOP (die up)
U = Unencapsulated die

Operating Temperature
C = Commercial = 0° to 70°C
I = Industrial = -40° to 85°C

Minimum Endurance
3 = 1000 cycles
4 = 10,000 cycles

Read Access Speed
150 = 150 ns
120 = 120 ns

Valid combinations

SST29EE020-120-4C- EH	SST29EE020-120-4C- NH	SST29EE020-120-4C- PH
SST29EE020-150-4C- EH	SST29EE020-150-4C- NH	SST29EE020-150-4C- PH
SST29EE020-120-3C- EH	SST29EE020-120-3C- NH	SST29EE020-120-3C- PH
SST29EE020-150-3C- EH	SST29EE020-150-3C- NH	SST29EE020-150-3C- PH
SST29EE020-120-4I-EH	SST29EE020-120-4I-NH	SST29EE020-150-4C-U1
SST29EE020-150-4I-EH	SST29EE020-150-4I-NH	
SST29EE020-120-3I-EH	SST29EE020-120-3I-NH	SST29EE020-150-3C-U1
SST29EE020-150-3I-EH	SST29EE020-150-3I-NH	

Example: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Preliminary Specifications

SST 29LE020
3.0V-only 2 Megabit Page Mode EEPROM

July 1996

SST 29LE020
3.0V-only 2 Megabit Page Mode EEPROM

Preliminary Specifications

Features:

Single 3.0-Volt Read and Write Operations
CMOS SuperFlash EEPROM Technology
Endurance: 100,000 Cycles (typical)
Greater than 100 years Data Retention
Low Power Consumption:
Active Current: 10 mA (typical)
Standby Current: 10 µA (typical)
Fast Page-Write Operation
128 Bytes per Page, 2048 Pages
Page-Write Cycle: 5 ms (typical)
Complete Memory Rewrite: 10 sec (typical)
Effective Byte-write Cycle Time: 39 µs (typical)
Fast Access Time: 200 and 250 ns
Latched Address and Data
Automatic Write Timing with Internal V_{pp} Generation
End of Write Detection
Toggle Bit
Data# Polling
Hardware and Software Data Protection
TTL I/O Compatibility
JEDEC Standard Byte-wide EEPROM Pinouts
Packages Available
32-Pin TSOP
32-Lead PLCC
32 Pin Plastic DIP

Product Description

The 29LE020 is a 256K x 8 CMOS page mode EEPROM manufactured with SST's proprietary, high performance CMOS SuperFlash technology. The split gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The 29LE020 writes with a 3.0-volt-only power supply. (V_{CC}: 3.0V to 3.6V) Internal erase/program is transparent to the user. The 29LE020 conforms to JEDEC standard pinouts for byte-wide memories.

Featuring high performance page write, the 29LE020 provides a typical byte-write time of 39 µsec. The entire memory, i.e., 256K bytes, can be written page by page in as little as 10 seconds, when using interface features such as Toggle Bit or Data# Polling to indicate the completion of a write cycle. To protect against inadvertent write, the 29LE020 has on-chip hardware and software data protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, the 29LE020 is offered with a guaranteed page-write endurance of 10^4 or 10^3 cycles. Data retention is rated at greater than 100 years.

The 29LE020 is suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, the 29LE020 significantly improves performance and reliability, while lowering power consumption, when compared with 5 volt EEPROM or EPROM approaches. The 29LE020 improves flexibility while lowering the cost for program, data, and configuration storage applications.

To meet high density, surface mount requirements, the 29LE020 is offered in 32-pin TSOP and 32-lead PLCC packages. A 600-mil, 32-pin PDIP package is also available. See Figures 2A and 2B for pinouts.

Device Operation

The SST page mode EEPROM offers in-circuit electrical write capability. The 29LE020 does not require separate erase and program operations. The internally timed write cycle executes both erase and program transparently to the user. The 29LE020 has industry standard optional Software Data Protection, which SST recommends always to be enabled. The 29LE020 is compatible with industry standard EEPROM pinouts and functionality.

Read

The read operation of the 29LE020 is controlled by CE# and OE#, both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the read cycle timing diagram for further details (Figure 3).

Write

The write operation consists of three steps. The first step is the optional three byte load sequence for Software Data Protection. This is an optional first step in the write operation, but highly recommended to ensure proper data integrity. Step 2 is the byte-load cycle to a page buffer of the 29LE020. Step 3 is an internally controlled write cycle for writing the data loaded in the page buffer into the memory array for nonvolatile storage. During the byte-load cycle, the addresses are latched by the falling edge of either CE# or WE#, whichever occurs last. The data is latched by the rising edge of either CE# or WE#, whichever occurs first. The internal write cycle is initiated by a timer after the rising edge of WE# or CE#, whichever occurs first. The write cycle, once initiated, will continue to completion, typically within 5 ms. See Figures 4 and 5 for WE# and CE# controlled page write cycle timing diagrams and Figures 15 and 17 for flowcharts.

The write operation has three functional cycles: the optional Software Data Protection load sequence, the page load cycle and the internal write cycle. The Software Data Protection consists of a specific three byte load sequence that will leave the 29LE020 protected at the end of the page write. The page load cycle consists of loading 1 to 128 bytes of data into the page buffer. The internal write cycle consists of the T_{BLCO} time-out and the write timer operation. During the write operation, the only valid reads are Data# Polling and Toggle Bit.

The page-write operation allows the loading of up to 128 bytes of data into the page buffer of the 29LE020 before the initiation of the internal write cycle. During the internal write cycle, all the data in the page buffer is written simultaneously into the memory array. Hence, the page-write feature of 29LE020 allows the entire memory to be written in as little as 10 seconds. During the internal write cycle, the host is free to perform additional tasks, such as to fetch data from other locations in the system to set up the write to the next page. In each page-write operation, all the bytes that are loaded into the page buffer must have the same page address, i.e., A_7 through A_{17}. Any byte not loaded with user data will be written to FF.

See Figures 4, 5, and 8 for the page-write cycle timing diagrams. If after the initial byte-load cycle, the host loads a second byte into the page buffer within a byte-load cycle time (T_{BLC}) of 100 µs, the 29LE020 will stay in the page load cycle. Additional bytes are then loaded consecutively. The page load cycle will be terminated if no additional byte is loaded into the page buffer within 200 µs (T_{BLCO}) from the last byte-load cycle, i.e., no subsequent WE# or CE# high-to-low transition after the last rising edge of WE# or CE#. Data in the page buffer can be changed by a subsequent byte-load cycle. The page load period can continue indefinitely, as long as the host continues to load the device within the byte-load cycle time of 100 µs. The page to be loaded is determined by the page address of the last byte loaded.

Software Chip-Erase

The 29LE020 provides a chip-erase operation, which allows the user to simultaneously clear the entire memory array to the "1" state. This is useful when the entire device must be quickly erased.

The Software Chip-Erase operation is initiated by using a specific six byte-load sequence. After the load sequence, the device enters into an internally timed cycle similar to the write cycle. During the erase operation, the only valid read is Toggle Bit. See Table 4 for the load sequence, Figure 10 for timing diagram, and Figure 19 for the flowchart.

Write Operation Status Detection

The 29LE020 provides two software means to detect the completion of a write cycle, in order to optimize the system write cycle time. The software detection includes two status bits: Data# Polling (DQ_7) and Toggle Bit (DQ_6). The end of write detection mode is enabled after the rising WE# or CE# whichever occurs first, which initiates the internal write cycle.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both

reads are valid, then the device has completed the write cycle, otherwise the rejection is valid.

Data# Polling (DQ_7)

When the 29LE020 is in the internal write cycle, any attempt to read DQ_7 of the last byte loaded during the byte-load cycle will receive the complement of the true data. Once the write cycle is completed, DQ_7 will show true data. The device is then ready for the next operation. See Figure 6 for Data# Polling timing diagram and Figure 16 for a flowchart.

Toggle Bit (DQ_6)

During the internal write cycle, any consecutive attempts to read DQ_6 will produce alternating 0's and 1's, i.e., toggling between 0 and 1. When the write cycle is completed, the toggling will stop. The device is then ready for the next operation. See Figure 7 for Toggle Bit timing diagram and Figure 16 for a flowchart. The initial read of the Toggle Bit will be a "1".

Data Protection

The 29LE020 provides both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a write cycle.

V_{CC} Power Up/Down Detection: The write operation is inhibited when V_{CC} is less than 2.5V.

Write Inhibit Mode: Forcing OE# low, CE# high, or WE# high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down.

Software Data Protection (SDP)

The 29LE020 provides the JEDEC approved optional software data protection scheme for all data alteration operations, i.e., write and chip erase. With this scheme, any write operation requires the inclusion of a series of three byte-load operations to precede the data loading operation. The three byte-load sequence is used to initiate the write cycle, providing optimal protection from inadvertent write operations, e.g., during the system power-up or power-down. The 29LE020 is shipped with the software data protection disabled.

The software protection scheme can be enabled by applying a three-byte sequence to the device, during a page-load cycle (Figure 8). The device will then be automatically set into the data protect mode. Any subsequent write operation will require the preceding three-byte sequence. See Table 4 for the specific software command codes and Figure 8 for the timing diagram. To set the device into the unprotected mode, a six-byte sequence is required. See Table 4 for the specific codes and Figure 9 for the timing diagram. If a write is attempted while SDP is enabled the device will be in a non-accessible state for ~ 300 µs. SST recommends Software Data Protection always be enabled. See Figure 17 for flowcharts.

The 29LE020 Software Data Protection is a global command, protecting (or unprotecting) all pages in the entire memory array once enabled (or disabled). Therefore using SDP for a single page write will enable SDP for the entire array. Single pages by themselves cannot be SDP enabled or disabled.

Single power supply reprogrammable nonvolatile memories may be unintentionally altered. SST strongly recommends that Software Data Protection (SDP) always be enabled. The 29LE020 should be programmed using the SDP command sequence. SST recommends the SDP Disable Command Sequence not be issued to the device prior to writing.

Product Identification

The product identification mode identifies the device as the 29LE020 and manufacturer as SST. This mode may be accessed by hardware or software operations. The hardware operation is typically used by a programmer to identify the correct algorithm for the 29LE020. Users may wish to use the software product identification operation to identify the part (i.e., using the device code) when using multiple manufacturers in the same socket. For details, see Table 3 for hardware operation or Table 4 for software operation, Figure 11 for the software ID entry and read timing diagram and Figure 18 for the ID entry command sequence flowchart. The manufacturer and device codes are the same for both operations.

Table 1: Product Identification Table

	Byte	Data
Manufacturers Code	0000 H	BF H
Device Code	0001 H	12 H

Product Identification Mode Exit

In order to return to the standard read mode, the Software Product Identification mode must be exited. Exiting is accomplished by issuing the Software ID Exit (reset) operation, which returns the device to the read operation. The reset operation may also be used to reset the device to the read mode after an inadvertent transient condition that apparently causes the device to behave abnormally, e.g., not read correctly. See Table 4 for software command codes, Figure 12 for timing wavefrom and Figure 18 for a flowchart.

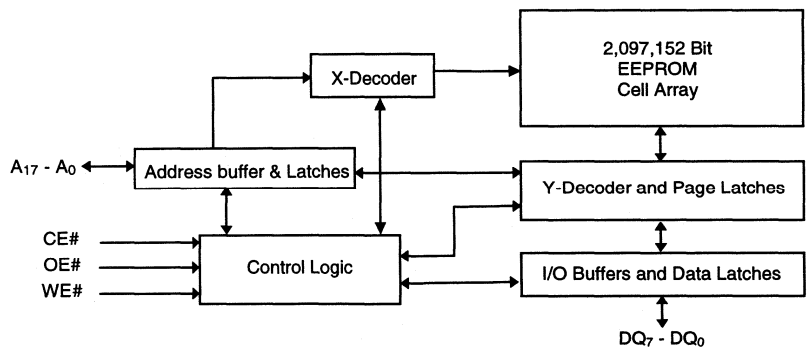


Figure 1: Functional Block Diagram of SST 29LE020

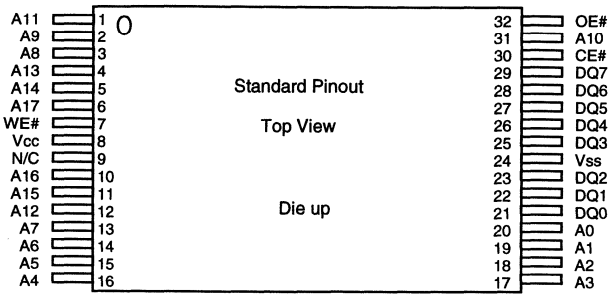


Figure 2A: Pin Assignments for 32-pin TSOP Packages

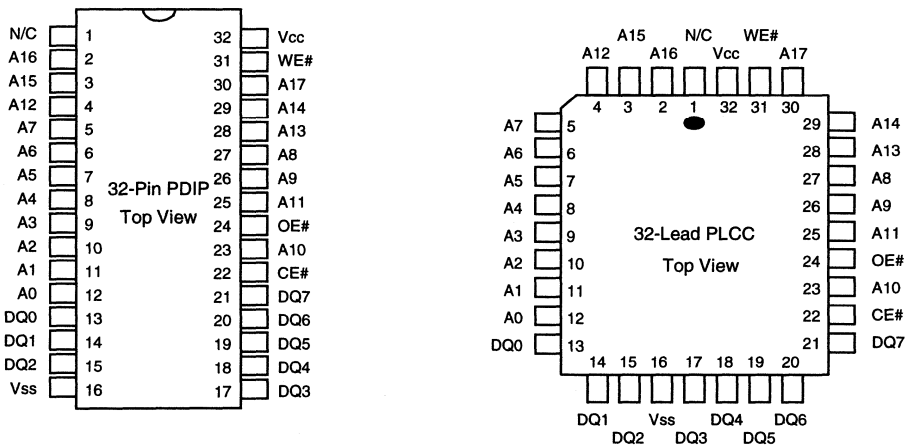


Figure 2B: Pin Assignments for 32-pin Plastic DIPs and 32-lead PLCCs

Table 2: Pin Description

Symbol	Pin Name	Functions
A_{17}-A_7	Row Address Inputs	To provide memory addresses. Row addresses define a page for a write cycle.
A_6-A_0	Column Address Inputs	Column Addresses are toggled to load page data.
DQ_7-DQ_0	Data Input/output	To output data during read cycles and receive input data during write cycles. Data is internally latched during a write cycle. The outputs are in tri-state when OE# or CE# is high.
CE#	Chip Enable	To activate the device when CE# is low.
OE#	Output Enable	To gate the data output buffers.
WE#	Write Enable	To control the write operations
Vcc	Power Supply	To provide 3.3-volt supply (± 0.3V)
Vss	Ground	
NC	No Connection	Unconnected pins.

Table 3: Operation Modes Selection

Mode	CE#	OE#	WE#	DQ	Address
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	A_{IN}
Page Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}
Standby	V_{IH}	X	X	High Z	X
Write Inhibit	X	V_{IL}	X	High Z/ D_{OUT}	X
Write Inhibit	X	X	V_{IH}	High Z/ D_{OUT}	X
Software Chip Erase	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}, See Table 4
Product Identification					
Hardware Mode	V_{IL}	V_{IL}	V_{IH}	Manufacturer Code (BF)	A_{17} - A_1 = V_{IL}, A_9 = V_H, A_0 = V_{IL}
				Device Code (12)	A_{17} - A_1 = V_{IL}, A_9 = V_H, A_0= V_{IH}
Software Mode	V_{IL}	V_{IH}	V_{IL}		See Table 4
SDP Enable Mode	V_{IL}	V_{IH}	V_{IL}		See Table 4
SDP Disable Mode	V_{IL}	V_{IH}	V_{IL}		See Table 4

Table 4: Software Command Codes

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data
Software Data Protect Enable & Page Write	5555H	AAH	2AAAH	55H	5555H	A0H	Addr[2]	Data				
Software Data Protect Disable	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	20H
Software Chip Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry	5555H	AAH	2AAAH	55H	5555H	90H						
Software ID Exit	5555H	AAH	2AAAH	55H	5555H	F0H						
Alternate Software ID Entry[3]	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	60H

Notes: (1) Address format A_{14}-A_0 (Hex), Address A_{15} is a "Don't Care".

(2) Page Write consists of loading up to 128 bytes (A_6 - A_0).

(3) Alternate 6 byte Software Product ID Command Code

Notes for Software Product ID Command Code:

1. With A_{14} -A_1 =0; SST Manufacturer Code = BFH, is read with A_0 = 0,
   29LE020 Device Code = 12H, is read with A_0 = 1.
2. The device does not remain in Software Product ID Mode if powered down.
3. This product supports both the JEDEC standard 3 byte command code sequence and SST's original 6 byte command code sequence. For new designs, SST recommends that the 3 byte command code sequence be used.

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential ..... -0.5V to V_{CC}+ 0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential ..... -1.0V to V_{CC}+ 1.0V
Voltage on A_9 Pin to Ground Potential ..... -0.5V to 14.0V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Through Hole Lead Soldering Temperature (10 Seconds) ..... 300°C
Surface Mount Lead Soldering Temperature (3 Seconds) ..... 240°C
Output Short Circuit Current[1] ..... 100 mA

Note: [1] Outputs shorted for no more than one second. No more than one output shorted at a time.

Operating Range

Range	Ambient Temp	V_{CC}
Commercial	0 °C to +70 °C	3.0V to 3.6V
Industrial	-40 °C to +85 °C	3.0V to 3.6V

AC Conditions of Test

Input Rise/Fall Time.....10 ns
Output Load.....1 TTL Gate and C_L = 100 pF
See Figures 13 and 14

Table 5: DC Operating Characteristics

Symbol	Parameter	Limits Min	Limits Max	Units	Test Conditions
I_{CC}	Power Supply Current				CE#=OE#=V_{IL},WE#=V_{IH}, all I/Os open,
	Read		12	mA	Address input = V_{IL}/V_{IH}, at f=1/T_{RC} Min., V_{CC}=V_{CC} Max
	Write		15	mA	CE#=WE#=V_{IL}, OE#=V_{IH}, V_{CC}=V_{CC} Max.
I_{SB1}	Standby V_{CC} Current (TTL input)		1	mA	CE#=OE#=WE#=V_{IH}, V_{CC}=V_{CC} Max.
I_{SB2}	Standby V_{CC} Current (CMOS input)		15	µA	CE#=OE#=WE#=V_{CC} -0.3V. V_{CC} = V_{CC} Max.
I_{LI}	Input Leakage Current		1	µA	V_{IN} =GND to V_{CC}, V_{CC} = V_{CC} Max.
I_{LO}	Output Leakage Current		10	µA	V_{OUT} =GND to V_{CC}, V_{CC} = V_{CC} Max.
V_{IL}	Input Low Voltage		0.8	V	V_{CC} = V_{CC} Max.
V_{IH}	Input High Voltage	2.0		V	V_{CC} = V_{CC} Max.
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 100 µA, V_{CC} = V_{CC} Min.
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -100 µA, V_{CC} = V_{CC} Min.
V_H	Supervoltage for A_9	11.6	12.4	V	CE# = OE# =V_{IL}, WE# = V_{IH}
I_H	Supervoltage Current for A_9		200	µA	CE# = OE# = V_{IL}, WE# = V_{IH}, A_9 = V_H Max.

Table 6: Power-up Timings

Symbol	Parameter	Maximum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$[1]	Power-up to Write Operation	5	ms

Table 7: Capacitance (Ta = 25 °C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0v	6 pF

Note: [1]This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 8: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}	Endurance	1,000 & 10,000[2]	Cycles	MIL-STD-883, Method 1033
T_{DR}[1]	Data Retention	100	Years	MIL-STD-883, Method 1008
V_{ZAP_HBM}[1]	ESD Susceptibility Human Body Model	1000	Volts	JEDEC Standard A114
V_{ZAP_MM}[1]	ESD Susceptibility Machine Model	200	Volts	JEDEC
I_{LTH}[1]	Latch Up	100	mA	JEDEC Standard 17

Note: [1]This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

[2]See Ordering Information for desired type.

AC Characteristics

Table 9: Read Cycle Timing Parameters

Symbol	Parameter	29LE020-200		29LE020-250		Units
		Min	Max	Min	Max	
T_{RC}	Read Cycle time	200		250		ns
T_{CE}	Chip Enable Access Time		200		250	ns
T_{AA}	Address Access Time		200		250	ns
T_{OE}	Output Enable Access Time		100		120	ns
T_{CLZ}[1]	CE# Low to Active Output	0		0		ns
T_{OLZ}[1]	OE# Low to Active Output	0		0		ns
T_{CHZ}[1]	CE# High to High-Z Output		50		50	ns
T_{OHZ}[1]	OE# High to High-Z Output		50		50	ns
T_{OH}[1]	Output Hold from Address Change	0		0		ns

Table 10: Page-Write Cycle Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{WC}	Write Cycle (erase and program)		10	ms
T_{AS}	Address Setup Time	0		ns
T_{AH}	Address Hold Time	50		ns
T_{CS}	WE# and CE# Setup Time	0		ns
T_{CH}	WE# and CE# Hold Time	0		ns
T_{OES}	OE# High Setup Time	0		ns
T_{OEH}	OE# High Hold Time	0		ns
T_{CP}	CE# Pulse Width	70		ns
T_{WP}	WE# Pulse Width	70		ns
T_{DS}	Data Setup Time	35		ns
T_{DH}	Data Hold Time	0		ns
T_{BLC}[1]	Byte Load Cycle Time	0.05	100	µs
T_{BLCO}[1]	Byte Load Cycle Time	200		µs
T_{IDA}	Software ID Access and Exit Time		10	µs
T_{SCE}	Software Chip Erase		20	ms

Note: [1]This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.

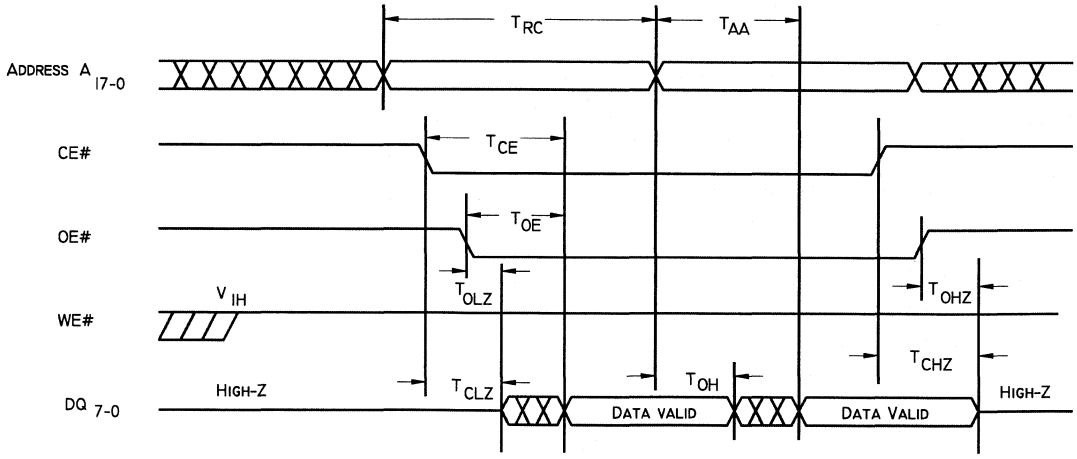


Figure 3: Read Cycle Timing Diagram

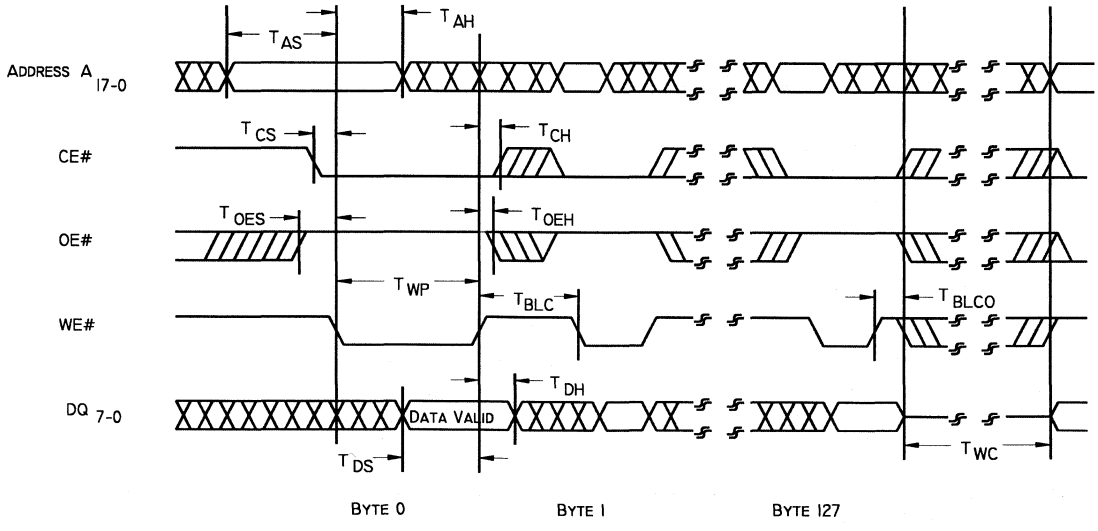


Figure 4: WE# Controlled Page Write Cycle Timing Diagram

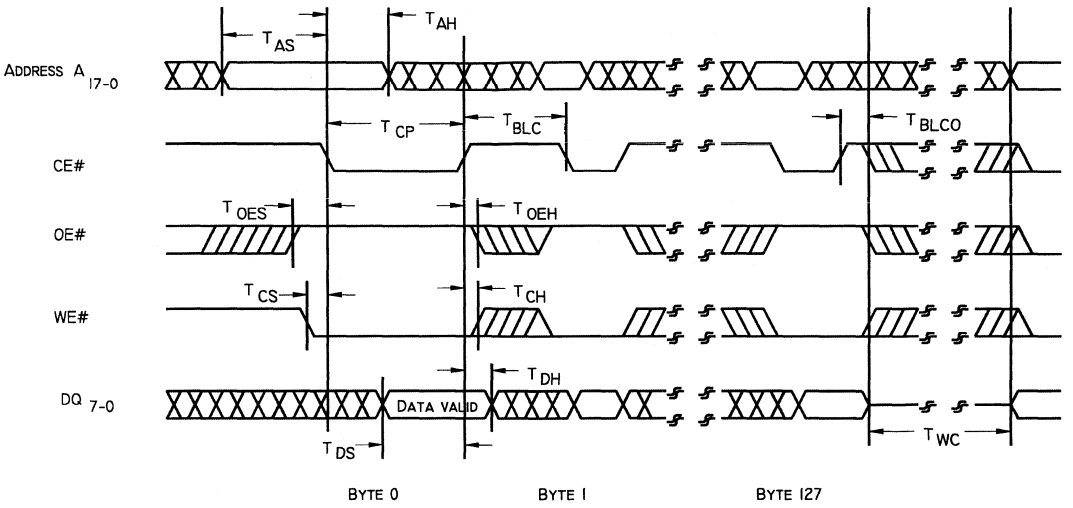


Figure 5: CE# Controlled Page Write Cycle Timing Diagram

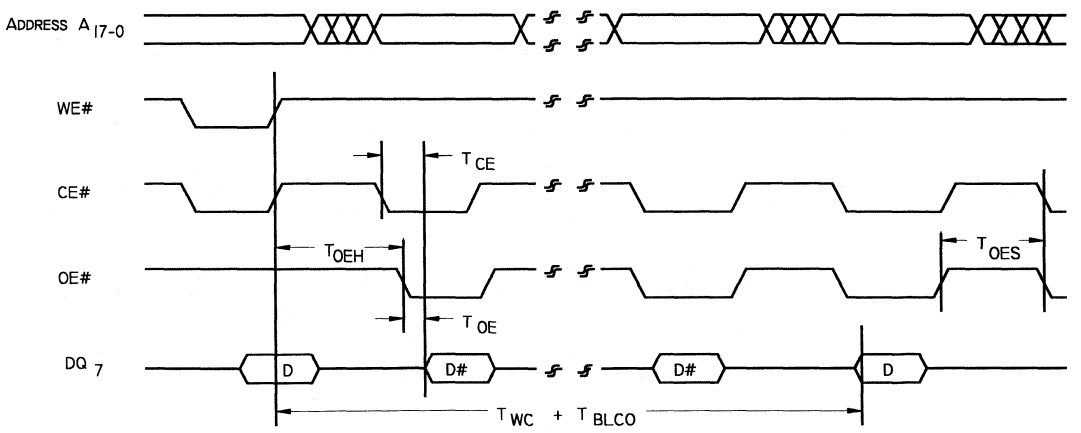
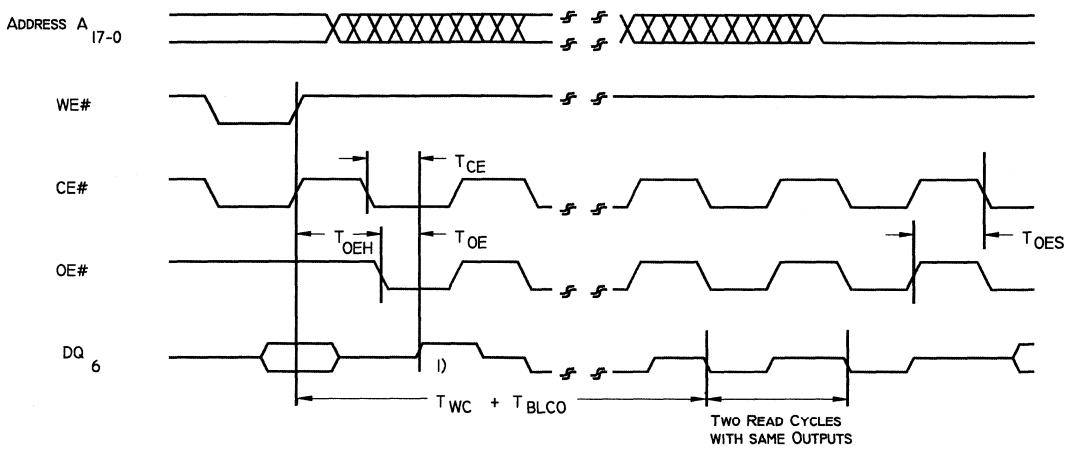
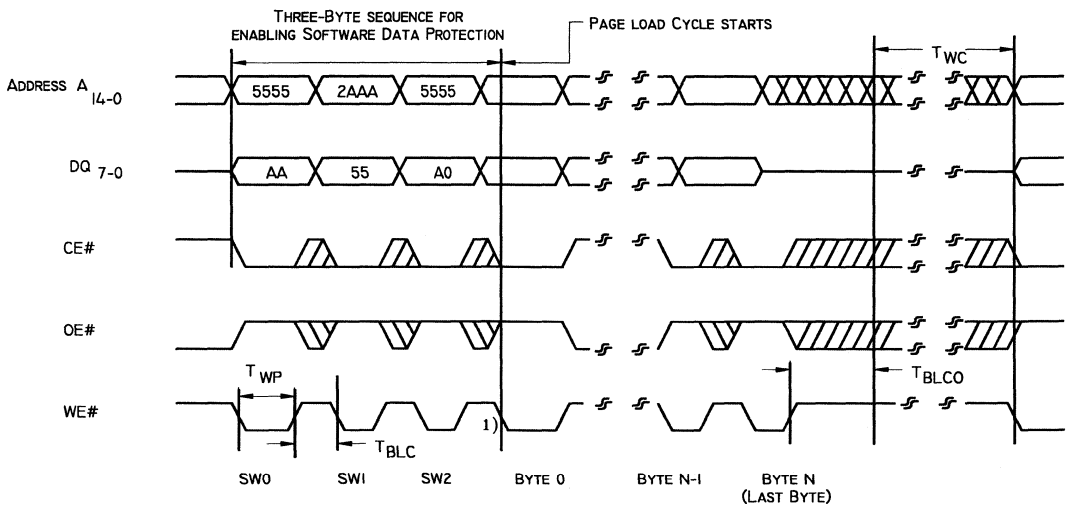


Figure 6: Data# Polling Timing Diagram



NOTE: 1) TOGGLE BIT OUTPUT IS ALWAYS HIGH FIRST.

Figure 7: Toggle Bit Timing Diagram



NOTE 1): THE TIME BETWEEN ENABLING SOFTWARE DATA PROTECT AND THE PAGE LOAD MUST BE LESS THAN T_{BLCO}

Figure 8: Software Data Protection Page Write Timing Diagram

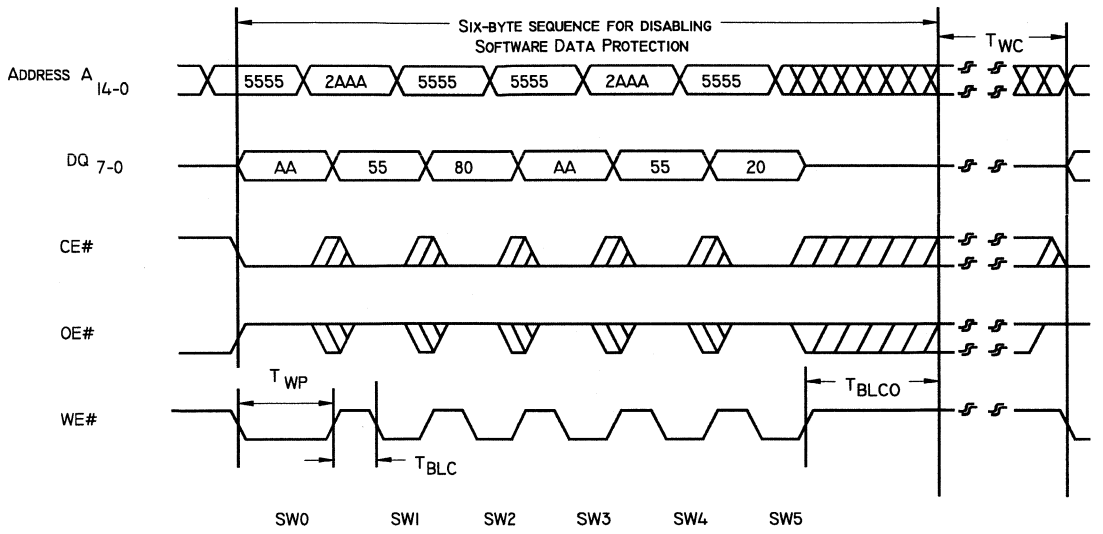


Figure 9: Software Data Protect Disable Timing Diagram

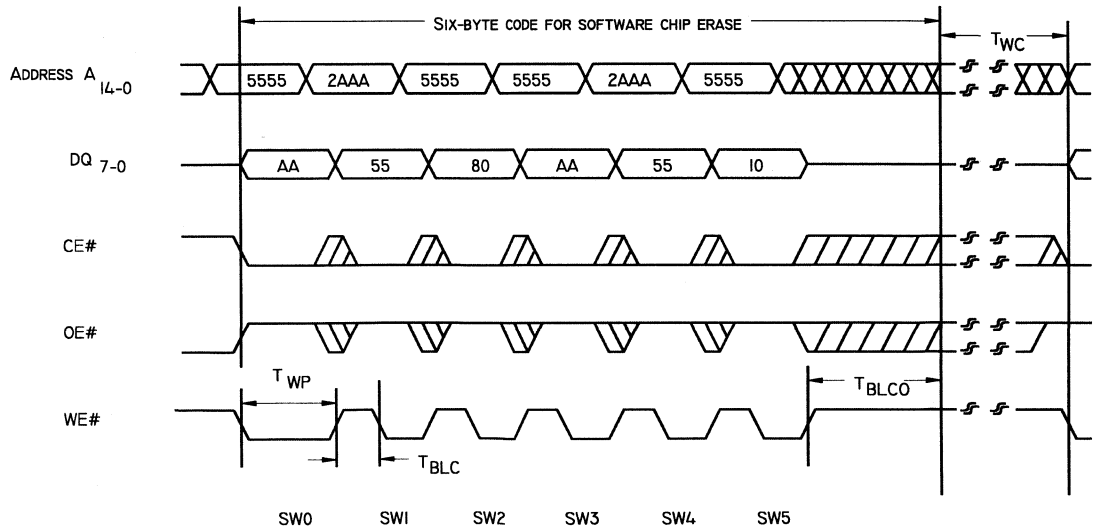


Figure 10: Software Chip Erase Timing Diagram

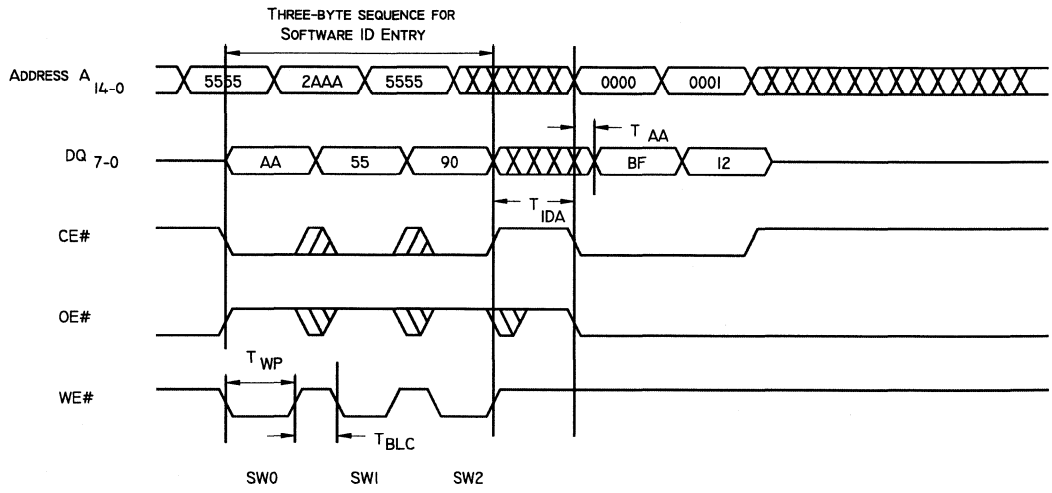


Figure 11: Software ID Entry and Read

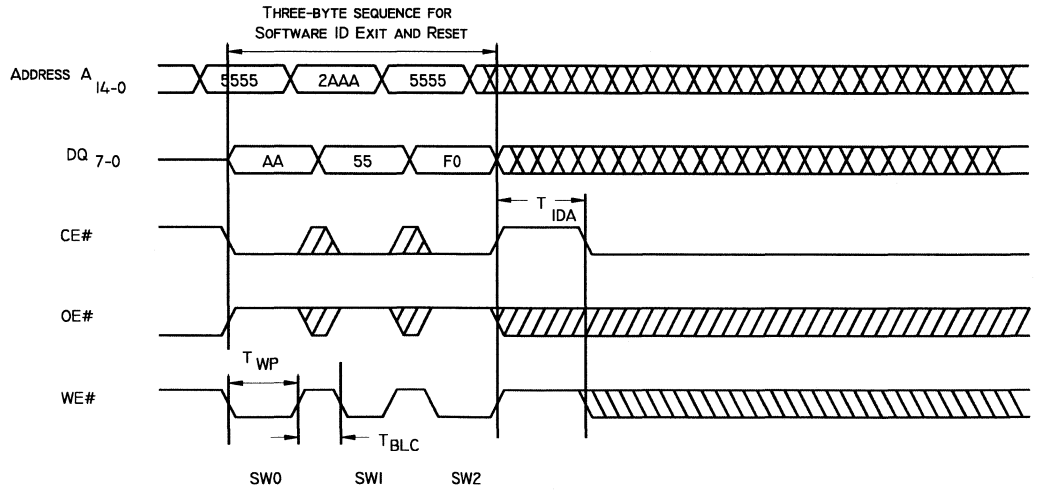
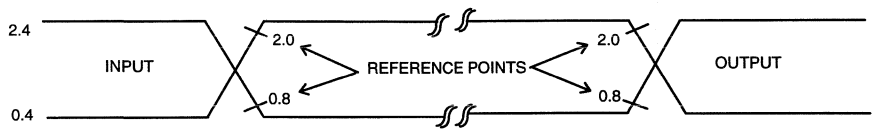


Figure 12: Software ID Exit and Reset



AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a logic "1" and V_{OL} (0.4 V_{TTL}) for a logic "0". Measurement reference points for inputs and outputs are V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Inputs rise and fall times (10% ↔ 90%) are <10 ns.

Figure 13: AC Input/Output Reference Waveforms

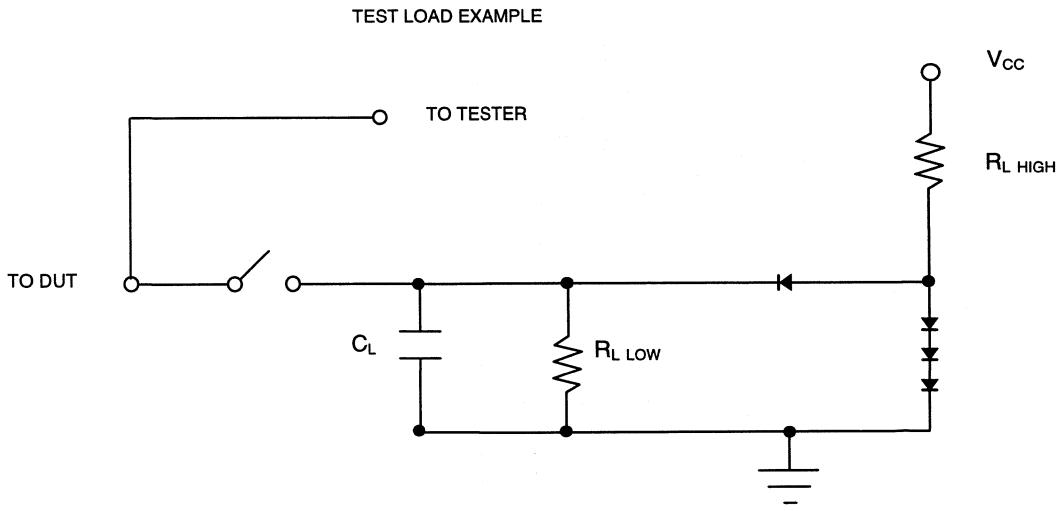


Figure 14: Test Load Example

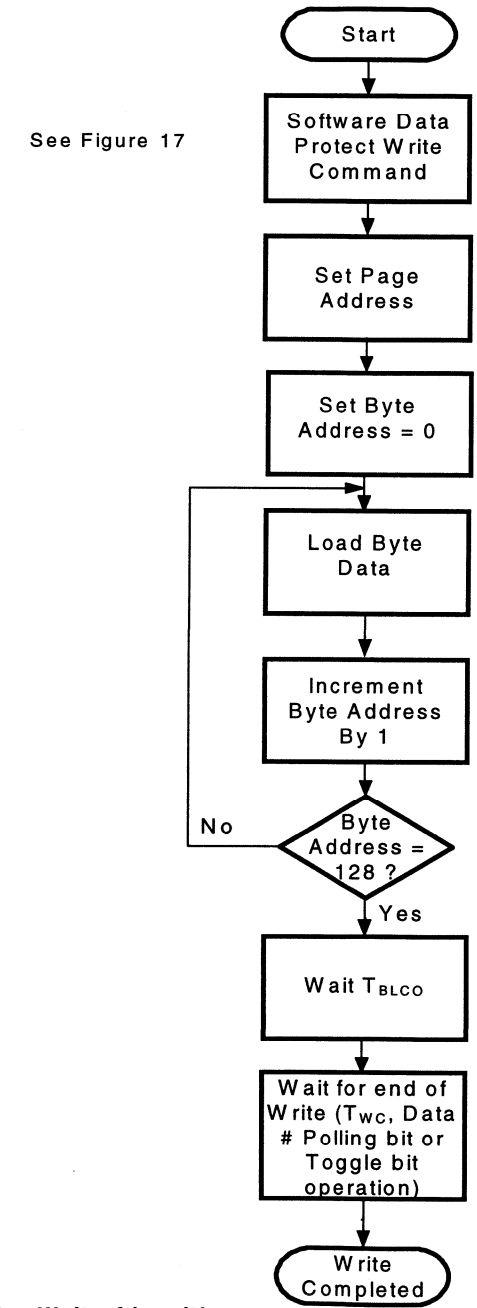


Figure 15: Write Algorithm

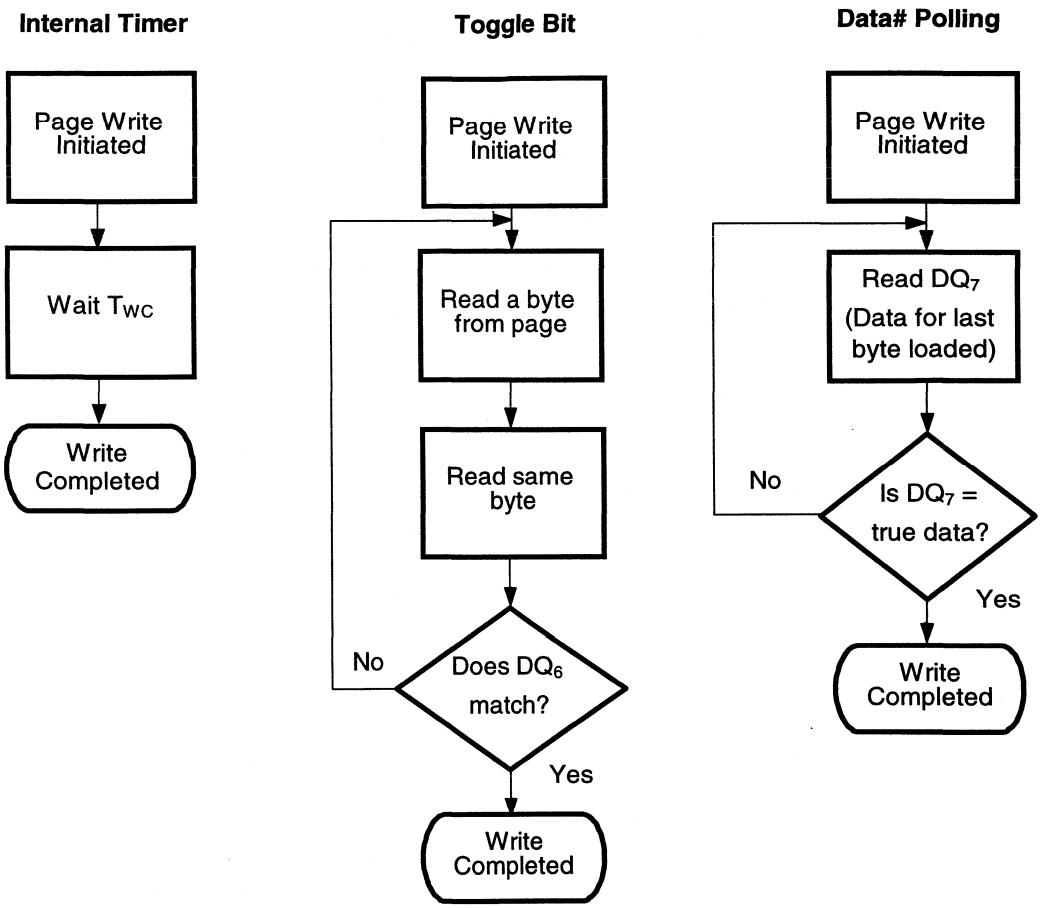


Figure 16: Wait Options

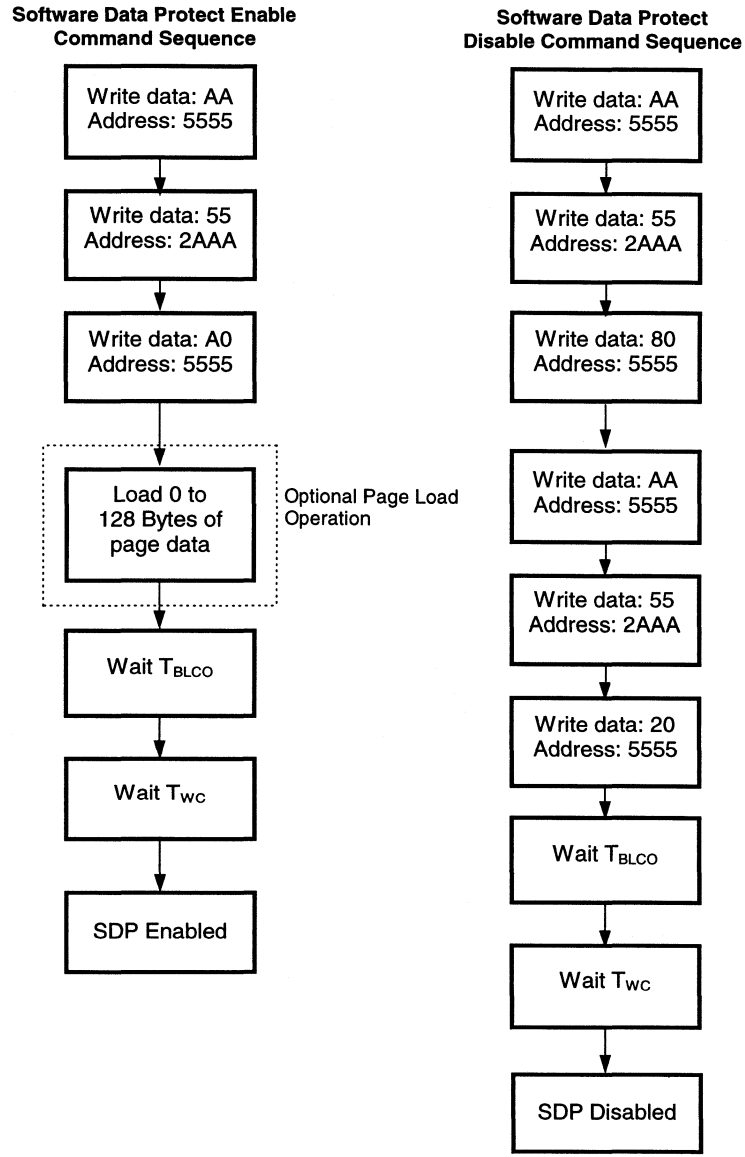


Figure 17: Software Data Protection Flowcharts

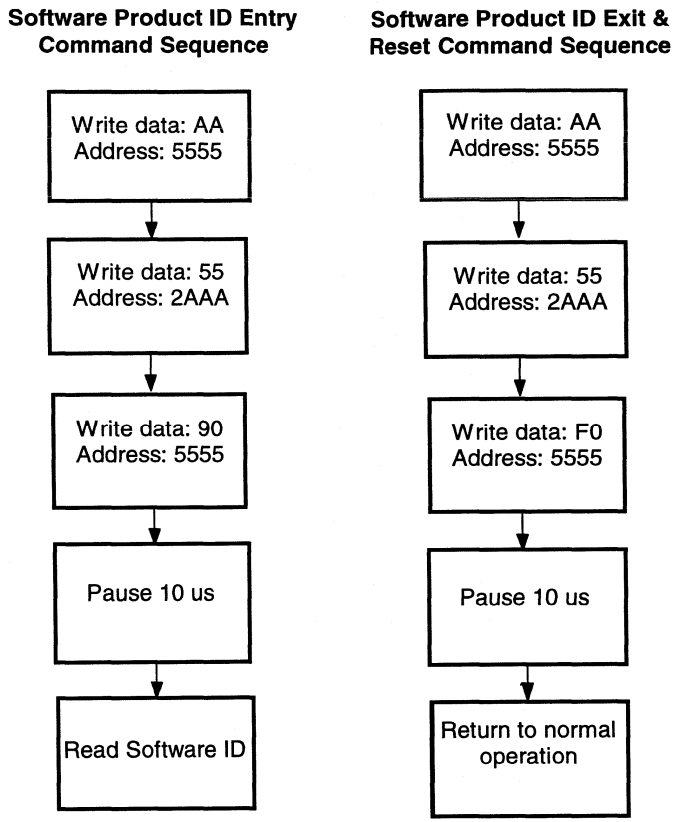


Figure 18: Software Product Command Flowcharts

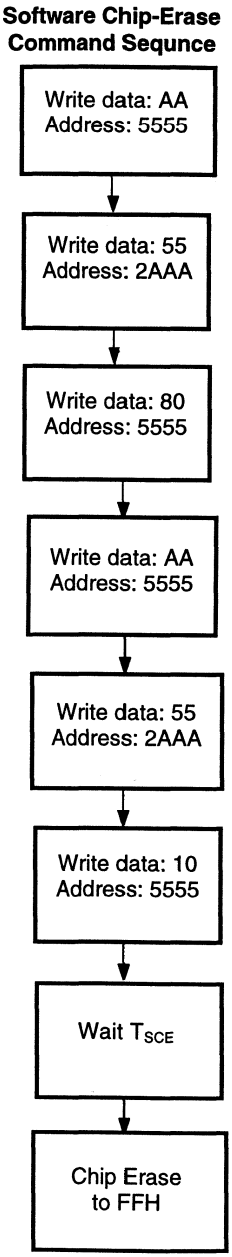


Figure 19: Software Chip Erase Command Codes

Product Ordering Information

Device **Speed** **Suffix1** **Suffix2**

SST29LE020 - XXX - XX - XX

Package Modifier
H = 32 leads
Numeric = Die modifier

Package Type
P = PDIP
N = PLCC
E = TSOP (die up)
U = Unencapsulated die

Operating Temperature
C = Commercial = 0° to 70°C
I = Industrial = -40° to 85°C

Minimum Endurance
3 = 1000 cycles
4 = 10,000 cycles

Read Access Speed
200 = 200 ns
250 = 250 ns

Valid combinations

SST29LE020-200-4C- EH	SST29LE020-200-4C- NH	SST29LE020-200-4C- PH
SST29LE020-250-4C- EH	SST29LE020-250-4C- NH	SST29LE020-250-4C- PH
SST29LE020-200-4I-EH	SST29LE020-200-4I-NH	
SST29LE020-250-4I-EH	SST29LE020-250-4I-NH	SST29LE020-250-4C-U1

Example: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Preliminary Specifications

SST 29VE020
2.7V-only 2 Megabit
Page Mode EEPROM

July 1996

SST 29VE020
2.7V-only 2 Megabit Page Mode EEPROM

Preliminary Specifications

Features:

Single 2.7-Volt Read and Write Operations
CMOS SuperFlash EEPROM Technology
- Endurance: 100,000 Cycles (typical)
- Greater than 100 years Data Retention

Low Power Consumption:
- Active Current: 20 mA (typical)
- Standby Current: 10 µA (typical)

Fast Page-Write Operation
- 128 Bytes per Page, 2048 Pages
- Page-Write Cycle: 5 ms (typical)
- Complete Memory Rewrite: 10 sec (typical)
- Effective Byte-write Cycle Time: 39 µs (typical)

Fast Access Time: 250 and 300 ns
Latched Address and Data
Automatic Write Timing with Internal V_{PP} Generation
End of Write Detection
- Toggle Bit
- Data# Polling

Hardware and Software Data Protection
TTL I/O Compatibility
JEDEC Standard Byte-wide EEPROM Pinouts
Packages Available
- 32-Pin TSOP
- 32-Lead PLCC
- 32 Pin Plastic DIP

Product Description

The 29VE020 is a 256K x 8 CMOS page mode EEPROM manufactured with SST's proprietary, high performance CMOS SuperFlash technology. The split gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The 29VE020 writes with a 2.7-volt-only power supply. (V_{CC}: 2.7V to 3.6V) Internal erase/program is transparent to the user. The 29VE020 conforms to JEDEC standard pinouts for byte-wide memories.

Featuring high performance page write, the 29VE020 provides a typical byte-write time of 39 µsec. The entire memory, i.e., 256K bytes, can be written page by page in as little as 10 seconds, when using interface features such as Toggle Bit or Data# Polling to indicate the completion of a write cycle. To protect against inadvertent write, the 29VE020 has on-chip hardware and software data protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, the 29VE020 is offered with a guaranteed page-write endurance of 10^4 or 10^3 cycles. Data retention is rated at greater than 100 years.

The 29VE020 is suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, the 29VE020 significantly improves performance and reliability, while lowering power consumption, when compared with 5 volt EEPROM or EPROM approaches. The 29VE020 improves flexibility while lowering the cost for program, data, and configuration storage applications.

To meet high density, surface mount requirements, the 29VE020 is offered in 32-pin TSOP and 32-lead PLCC packages. A 600-mil, 32-pin PDIP package is also available. See Figures 2A and 2B for pinouts.

Device Operation

The SST page mode EEPROM offers in-circuit electrical write capability. The 29VE020 does not require separate erase and program operations. The internally timed write cycle executes both erase and program transparently to the user. The 29VE020 has industry standard optional Software Data Protection, which SST recommends always to be enabled. The 29VE020 is compatible with industry standard EEPROM pinouts and functionality.

Read

The read operation of the 29VE020 is controlled by CE# and OE#, both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the read cycle timing diagram for further details (Figure 3).

Write

The write operation consists of three steps. The first step is the optional three byte load sequence for Software Data Protection. This is an optional first step in the write operation, but highly recommended to ensure proper data integrity. Step 2 is the byte-load cycle to a page buffer of the 29VE020. Step 3 is an internally controlled write cycle for writing the data loaded in the page buffer into the memory array for nonvolatile storage. During the byte-load cycle, the addresses are latched by the falling edge of either CE# or WE#, whichever occurs last. The data is latched by the rising edge of either CE# or WE#, whichever occurs first. The internal write cycle is initiated by a timer after the rising edge of WE# or CE#, whichever occurs first. The write cycle, once initiated, will continue to completion, typically within 5 ms. See Figures 4 and 5 for WE# and CE# controlled page write cycle timing diagrams and Figures 15 and 17 for flowcharts.

The write operation has three functional cycles: the optional Software Data Protection load sequence, the page load cycle and the internal write cycle. The Software Data Protection consists of a specific three byte load sequence that will leave the 29VE020 protected at the end of the page write. The page load cycle consists of loading 1 to 128 bytes of data into the page buffer. The internal write cycle consists of the T_{BLCO} time-out and the write timer operation. During the write operation, the only valid reads are Data# Polling and Toggle Bit.

The page-write operation allows the loading of up to 128 bytes of data into the page buffer of the 29VE020 before the initiation of the internal write cycle. During the internal write cycle, all the data in the page buffer is written simultaneously into the memory array. Hence, the page-write feature of 29VE020 allows the entire memory to be written in as little as 10 seconds. During the internal write cycle, the host is free to perform additional tasks, such as to fetch data from other locations in the system to set up the write to the next page. In each page-write operation, all the bytes that are loaded into the page buffer must have the same page address, i.e., A_7 through A_{17}. Any byte not loaded with user data will be written to FF.

See Figures 4, 5, and 8 for the page-write cycle timing diagrams. If after the initial byte-load cycle, the host loads a second byte into the page buffer within a byte-load cycle time (T_{BLC}) of 100 µs, the 29VE020 will stay in the page load cycle. Additional bytes are then loaded consecutively. The page load cycle will be terminated if no additional byte is loaded into the page buffer within 200 µs (T_{BLCO}) from the last byte-load cycle, i.e., no subsequent WE# or CE# high-to-low transition after the last rising edge of WE# or CE#. Data in the page buffer can be changed by a subsequent byte-load cycle. The page load period can continue indefinitely, as long as the host continues to load the device within the byte-load cycle time of 100 µs. The page to be loaded is determined by the page address of the last byte loaded.

Software Chip-Erase

The 29VE020 provides a chip-erase operation, which allows the user to simultaneously clear the entire memory array to the "1" state. This is useful when the entire device must be quickly erased.

The Software Chip-Erase operation is initiated by using a specific six byte-load sequence. After the load sequence, the device enters into an internally timed cycle similar to the write cycle. During the erase operation, the only valid read is Toggle Bit. See Table 4 for the load sequence, Figure 10 for timing diagram, and Figure 19 for the flowchart.

Write Operation Status Detection

The 29VE020 provides two software means to detect the completion of a write cycle, in order to optimize the system write cycle time. The software detection includes two status bits: Data# Polling (DQ_7) and Toggle Bit (DQ_6). The end of write detection mode is enabled after the rising WE# or CE# whichever occurs first, which initiates the internal write cycle.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If

both reads are valid, then the device has completed the write cycle, otherwise the rejection is valid.

Data# Polling (DQ_7)

When the 29VE020 is in the internal write cycle, any attempt to read DQ_7 of the last byte loaded during the byte-load cycle will receive the complement of the true data. Once the write cycle is completed, DQ_7 will show true data. The device is then ready for the next operation. See Figure 6 for Data# Polling timing diagram and Figure 16 for a flowchart.

Toggle Bit (DQ_6)

During the internal write cycle, any consecutive attempts to read DQ_6 will produce alternating 0's and 1's, i.e., toggling between 0 and 1. When the write cycle is completed, the toggling will stop. The device is then ready for the next operation. See Figure 7 for Toggle Bit timing diagram and Figure 16 for a flowchart. The read of the Toggle Bit will be a "1".

Data Protection

The 29VE020 provides both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a write cycle.

V_{CC} Power Up/Down Detection: The write operation is inhibited when V_{CC} is less than 2.5V.

Write Inhibit Mode: Forcing OE# low, CE# high, or WE# high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down.

Software Data Protection (SDP)

The 29VE020 provides the JEDEC approved optional software data protection scheme for all data alteration operations, i.e., write and chip erase. With this scheme, any write operation requires the inclusion of a series of three byte-load operations to precede the data loading operation. The three byte-load sequence is used to initiate the write cycle, providing optimal protection from inadvertent write operations, e.g., during the system power-up or power-down. The 29VE020 is shipped with the software data protection disabled.

The software protection scheme can be enabled by applying a three-byte sequence to the device, during a page-load cycle (Figure 8). The device will then be automatically set into the data protect mode. Any subsequent write operation will require the preceding three-byte sequence. See Table 4 for the specific software command codes and Figure 8 for the timing diagram. To set the device into the unprotected mode, a six-byte sequence is required. See Table 4 for the specific codes and Figure 9 for the timing diagram. If a write is attempted while SDP is enabled the device will be in a non-accessible state for ~ 300 µs. SST recommends Software Data Protection always be enabled. See Figure 17 for flowcharts.

The 29VE020 Software Data Protection is a global command, protecting (or unprotecting) all pages in the entire memory array once enabled (or disabled). Therefore using SDP for a single page write will enable SDP for the entire array. Single pages by themselves cannot be SDP enabled or disabled.

Single power supply reprogrammable nonvolatile memories may be unintentionally altered. SST strongly recommends that Software Data Protect (SDP) always be enabled. The 29VE020 should be programmed using the SDP command sequence. SST recommends the SDP Disable Command Sequence not be issued to the device prior to writing.

Product Identification

The product identification mode identifies the device as the 29VE020 and manufacturer as SST. This mode may be accessed by hardware or software operations. The hardware operation is typically used by a programmer to identify the correct algorithm for the SST 29VE020. Users may wish to use the software product identification operation to identify the part (i.e., using the device code) when using multiple manufacturers in the same socket. For details, see Table 3 for hardware operation or Table 4 for software operation, Figure 11 for the software ID entry and read timing diagram and Figure 18 for the ID entry command sequence flowchart. The manufacturer and device codes are the same for both operations.

Table 1: Product Identification Table

	Byte	Data
Manufacturers Code	0000 H	BF H
Device Code	0001 H	12 H

Product Identification Mode Exit

In order to return to the standard read mode, the Software Product Identification mode must be exited. Exiting is accomplished by issuing the Software ID Exit (reset) operation, which returns the device to the read operation. The reset operation may also be used to reset the device to the read mode after an inadvertent transient condition that apparently causes the device to behave abnormally, e.g., not read correctly. See Table 4 for software command codes, Figure 12 for timing wavefrom and Figure 18 for a flowchart.

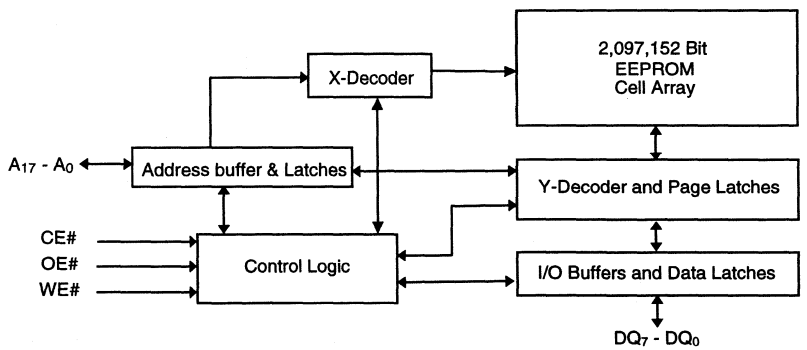


Figure 1: Functional Block Diagram of SST 29VE020

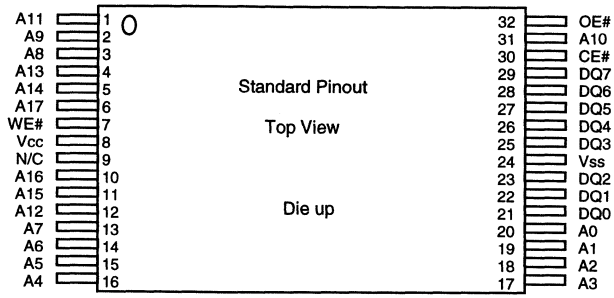


Figure 2A: Pin Assignments for 32-pin TSOP Packages

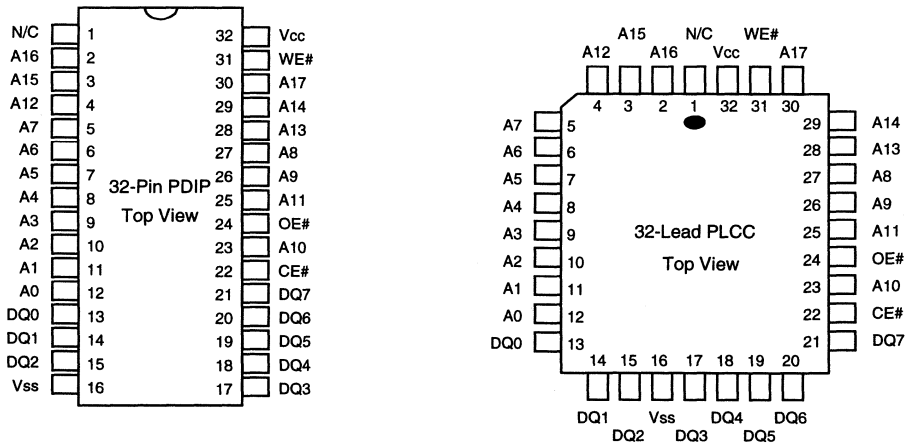


Figure 2B: Pin Assignments for 32-pin Plastic DIPs and 32-lead PLCCs

Table 2: Pin Description

Symbol	Pin Name	Functions
A_{17}-A_7	Row Address Inputs	To provide memory addresses. Row addresses define a page for a write cycle.
A_6-A_0	Column Address Inputs	Column Addresses are toggled to load page data.
DQ_7-DQ_0	Data Input/output	To output data during read cycles and receive input data during write cycles. Data is internally latched during a write cycle. The outputs are in tri-state when OE# or CE# is high.
CE#	Chip Enable	To activate the device when CE# is low.
OE#	Output Enable	To gate the data output buffers.
WE#	Write Enable	To control the write operations
Vcc	Power Supply	To provide 3.0-volt supply (2.7 to 3.6V)
Vss	Ground	
NC	No Connection	Unconnected pins.

Table 3: Operation Modes Selection

Mode	CE#	OE#	WE#	DQ	Address
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	A_{IN}
Page Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}
Standby	V_{IH}	X	X	High Z	X
Write Inhibit	X	V_{IL}	X	High Z/ D_{OUT}	X
Write Inhibit	X	X	V_{IH}	High Z/ D_{OUT}	X
Software Chip Erase	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}, See Table 4
Product Identification					
Hardware Mode	V_{IL}	V_{IL}	V_{IH}	Manufacturer Code (BF) Device Code (12)	A_{17} - A_1 = V_{IL}, A_9 = V_H, A_0 = V_{IL} A_{17} - A_1 = V_{IL}, A_9 = V_H, A_0= V_{IH}
Software Mode	V_{IL}	V_{IH}	V_{IL}		See Table 4
SDP Enable Mode	V_{IL}	V_{IH}	V_{IL}		See Table 4
SDP Disable Mode	V_{IL}	V_{IH}	V_{IL}		See Table 4

Table 4: Software Command Codes

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data
Software Data Protect Enable & Page Write	5555H	AAH	2AAAH	55H	5555H	A0H	Addr[2]	Data				
Software Data Protect Disable	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	20H
Software Chip Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry	5555H	AAH	2AAAH	55H	5555H	90H						
Software ID Exit	5555H	AAH	2AAAH	55H	5555H	F0H						
Alternate Software ID Entry[3]	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	60H

Notes: (1) Address format A_{14}-A_0 (Hex), Address A_{15} is a "Don't Care".

(2) Page Write consists of loading up to 128 bytes (A_6 - A_0).

(3) Alternate 6 byte Software Product ID Command Code

Notes for Software Product ID Command Code:

1. With A_{14} -A_1 =0; SST Manufacturer Code = BFH, is read with A_0 = 0,
   29VE020 Device Code = 12H, is read with A_0 = 1.
2. The device does not remain in Software Product ID Mode if powered down.
3. This product supports both the JEDEC standard 3 byte command code sequence and SST's original 6 byte command code sequence. For new designs, SST recommends that the 3 byte command code sequence be used.

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential ..... -0.5V to V_{CC}+ 0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential ..... -1.0V to V_{CC}+ 1.0V
Voltage on A_9 Pin to Ground Potential ..... -0.5V to 14.0V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Through Hole Lead Soldering Temperature (10 Seconds) ..... 300°C
Surface Mount Lead Soldering Temperature (3 Seconds) ..... 240°C
Output Short Circuit Current[1] ..... 100 mA

Note: [1] Outputs shorted for no more than one second. No more than one output shorted at a time.

Operating Range

Range	Ambient Temp	V_{CC}
Commercial	0 °C to +70 °C	2.7 to 3.6V
Industrial	-40 °C to +85 °C	2.7 to 3.6V

AC Conditions of Test

Input Rise/Fall Time.....10 ns
Output Load.....1 TTL Gate and C_L = 100 pF
See Figures 13 and 14

Table 5: DC Operating Characteristics

Symbol	Parameter	Limits Min	Limits Max	Limits Units	Test Conditions
I_{CC}	Power Supply Current				CE#=OE#=V_{IL},WE#=V_{IH}, all I/Os open,
	Read		12	mA	Address input = V_{IL}/V_{IH}, at f=1/T_{RC} Min., V_{CC}=V_{CC} Max
	Write		15	mA	CE#=WE#=V_{IL}, OE#=V_{IH}, V_{CC}=V_{CC} Max.
I_{SB1}	Standby V_{CC} Current (TTL input)		1	mA	CE#=OE#=WE#=V_{IH}, V_{CC}=V_{CC} Max.
I_{SB2}	Standby V_{CC} Current (CMOS input)		15	µA	CE#=OE#=WE#=V_{CC} -0.3V. V_{CC} = V_{CC} Max.
I_{LI}	Input Leakage Current		1	µA	V_{IN} =GND to V_{CC}, V_{CC} = V_{CC} Max.
I_{LO}	Output Leakage Current		10	µA	V_{OUT} =GND to V_{CC}, V_{CC} = V_{CC} Max.
V_{IL}	Input Low Voltage		0.8	V	V_{CC} = V_{CC} Max.
V_{IH}	Input High Voltage	2.0		V	V_{CC} = V_{CC} Max.
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 100 µA, V_{CC} = V_{CC} Min.
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -100 µA, V_{CC} = V_{CC} Min.
V_H	Supervoltage for A_9	11.6	12.4	V	CE# = OE# =V_{IL}, WE# = V_{IH}
I_H	Supervoltage Current for A_9		200	µA	CE# = OE# = V_{IL}, WE# = V_{IH}, A_9 = V_H Max.

Table 6: Power-up Timings

Symbol	Parameter	Maximum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$[1]	Power-up to Write Operation	5	ms

Table 7: Capacitance (Ta = 25 °C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0v	6 pF

Note: [1]This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 8: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}	Endurance	1,000 & 10,000[2]	Cycles	MIL-STD-883, Method 1033
T_{DR}[1]	Data Retention	100	Years	MIL-STD-883, Method 1008
V_{ZAP_HBM}[1]	ESD Susceptibility Human Body Model	1000	Volts	JEDEC Standard A114
V_{ZAP_MM}[1]	ESD Susceptibility Machine Model	200	Volts	JEDEC
I_{LTH}[1]	Latch Up	100	mA	JEDEC Standard 17

Note: [1]This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

[2]See Ordering Information for desired type.

AC Characteristics

Table 9: Read Cycle Timing Parameters

Symbol	Parameter	29VE020-250		29VE020-300		Units
		Min	Max	Min	Max	
T_{RC}	Read Cycle time	250		300		ns
T_{CE}	Chip Enable Access Time		250		300	ns
T_{AA}	Address Access Time		250		300	ns
T_{OE}	Output Enable Access Time		120		150	ns
T_{CLZ}(1)	CE# Low to Active Output	0		0		ns
T_{OLZ}(1)	OE# Low to Active Output	0		0		ns
T_{CHZ}(1)	CE# High to High-Z Output		50		50	ns
T_{OHZ}(1)	OE# High to High-Z Output		50		50	ns
T_{OH}(1)	Output Hold from Address Change	0		0		ns

Table 10: Page-Write Cycle Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{WC}	Write Cycle (erase and program)		10	ms
T_{AS}	Address Setup Time	0		ns
T_{AH}	Address Hold Time	50		ns
T_{CS}	WE# and CE# Setup Time	0		ns
T_{CH}	WE# and CE# Hold Time	0		ns
T_{OES}	OE# High Setup Time	0		ns
T_{OEH}	OE# High Hold Time	0		ns
T_{CP}	CE# Pulse Width	70		ns
T_{WP}	WE# Pulse Width	70		ns
T_{DS}	Data Setup Time	35		ns
T_{DH}	Data Hold Time	0		ns
T_{BLC}(1)	Byte Load Cycle Time	0.05	100	µs
T_{BLCO}(1)	Byte Load Cycle Time	200		µs
T_{IDA}	Software ID Access and Exit Time		10	µs
T_{SCE}	Software Chip Erase		20	ms

Note: (1)This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.

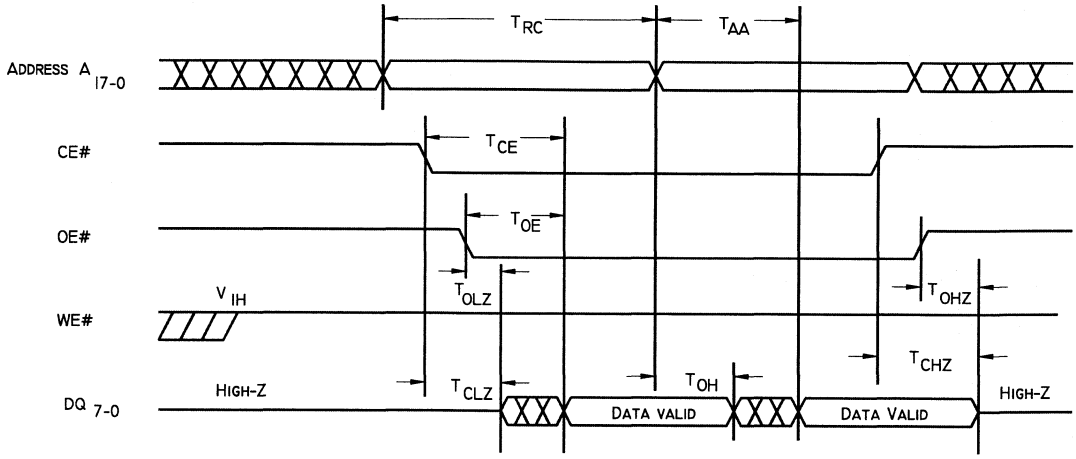


Figure 3: Read Cycle Timing Diagram

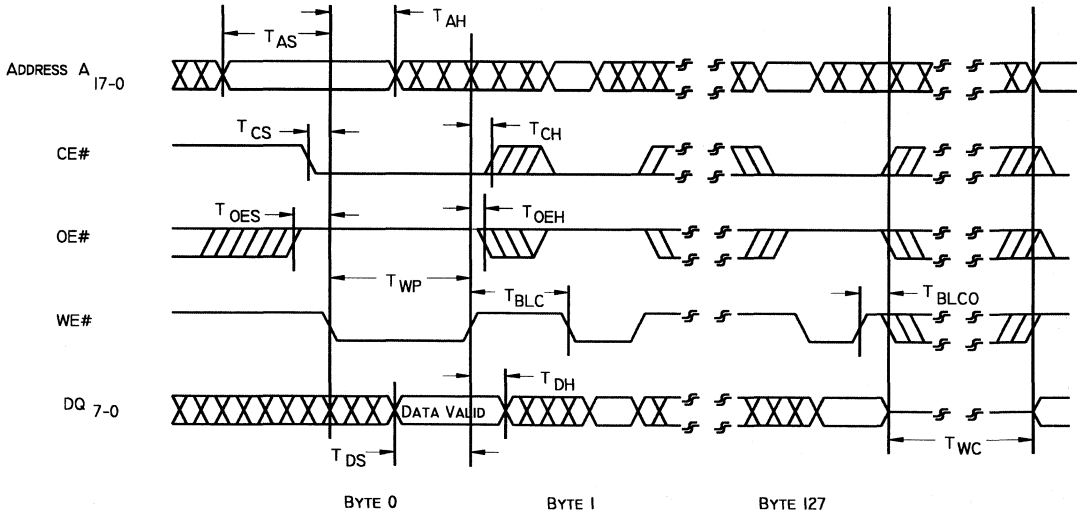


Figure 4: WE# Controlled Page Write Cycle Timing Diagram

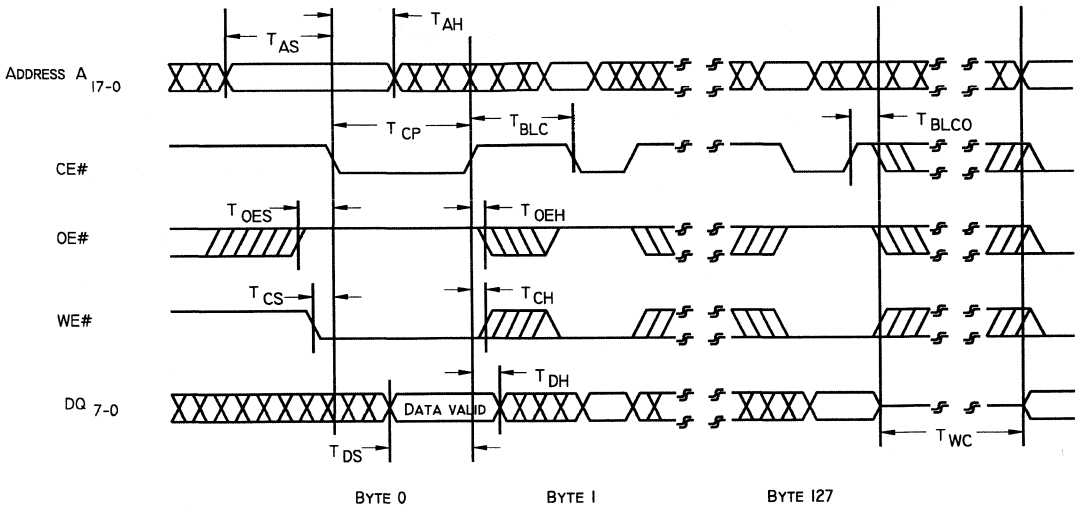


Figure 5: CE# Controlled Page Write Cycle Timing Diagram

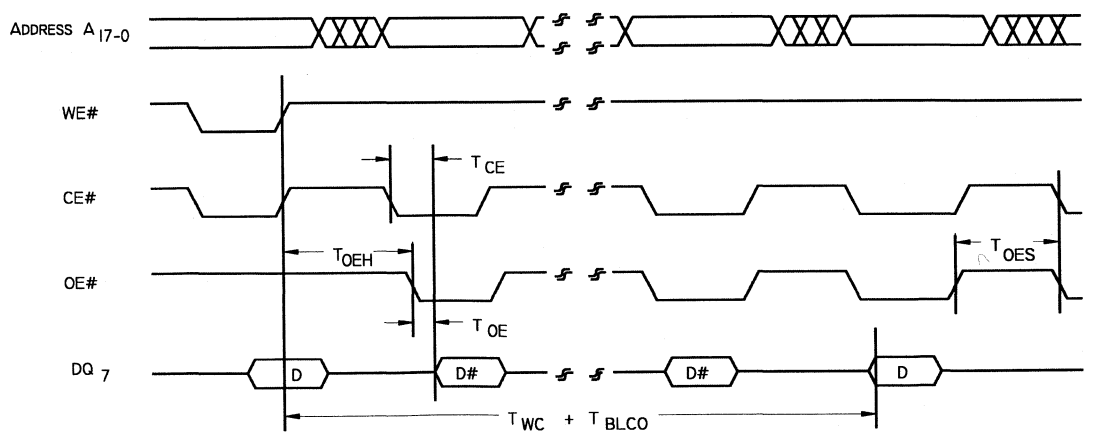
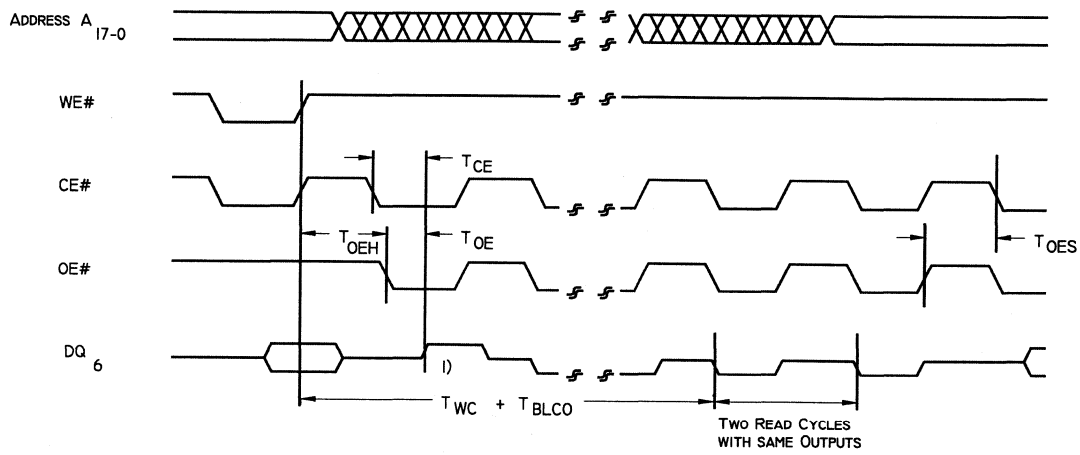
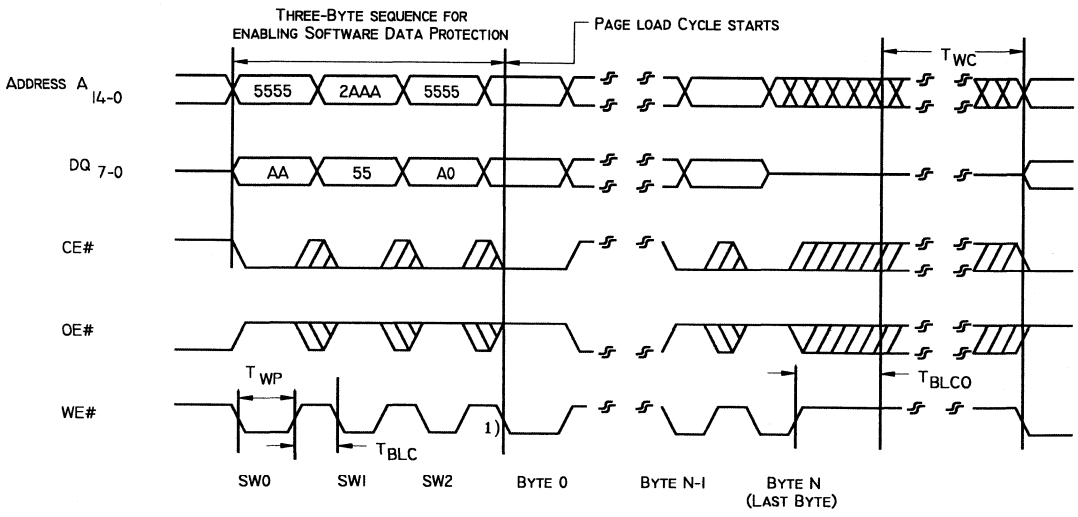


Figure 6: Data# Polling Timing Diagram



NOTE: 1) TOGGLE BIT OUTPUT IS ALWAYS HIGH FIRST.

Figure 7: Toggle Bit Timing Diagram



NOTE 1): THE TIME BETWEEN ENABLING SOFTWARE DATA PROTECT AND THE PAGE LOAD MUST BE LESS THAN T_{BLCO}

Figure 8: Software Data Protection Page Write Timing Diagram

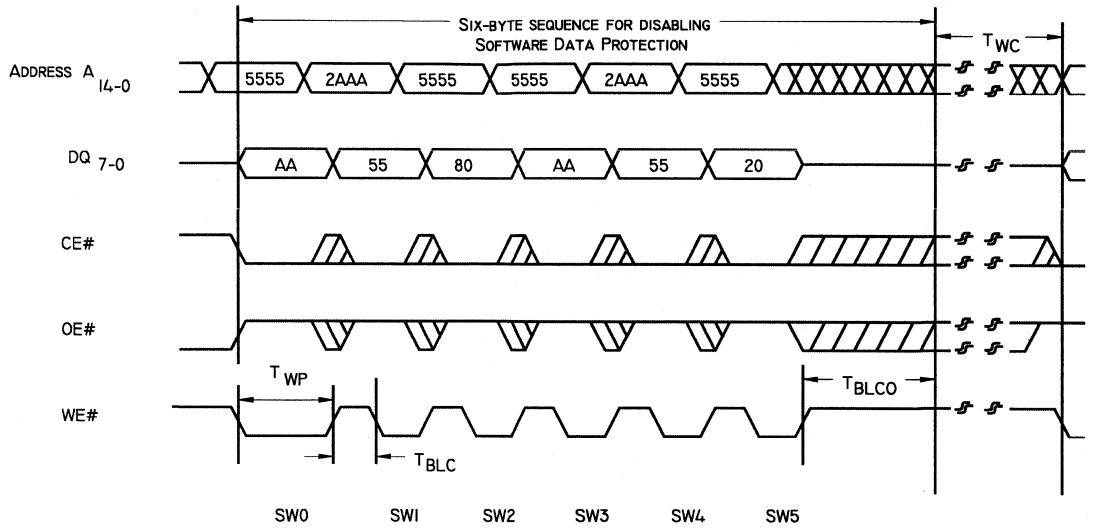


Figure 9: Software Data Protect Disable Timing Diagram

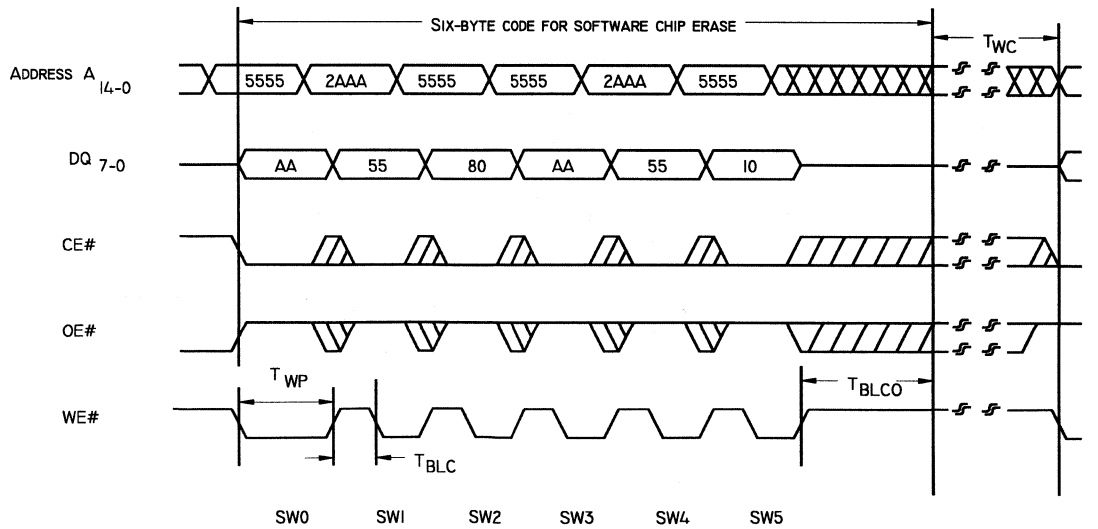


Figure 10: Software Chip Erase Timing Diagram

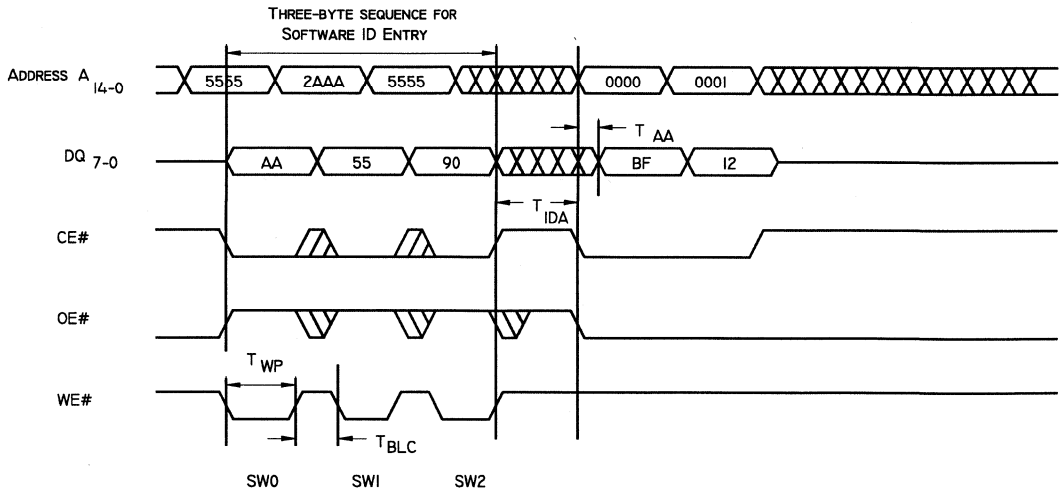


Figure 11: Software ID Entry and Read

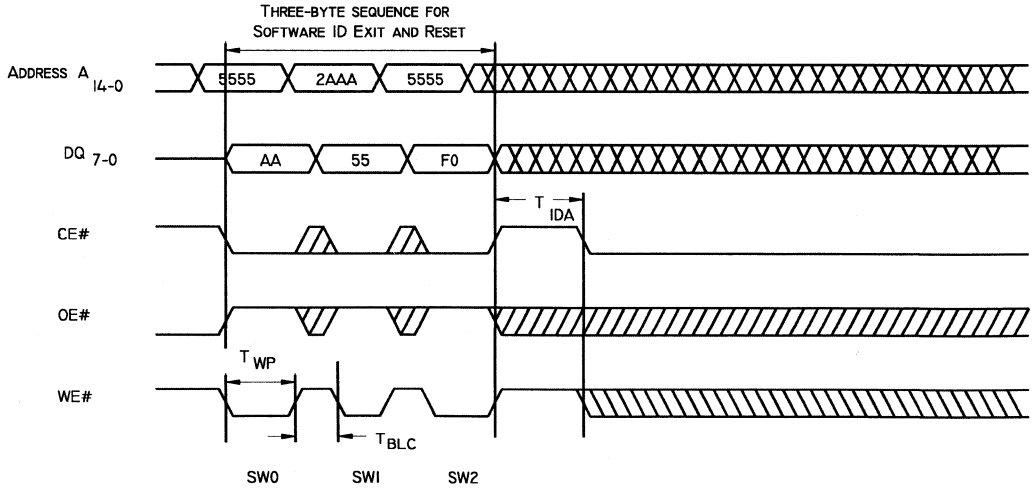
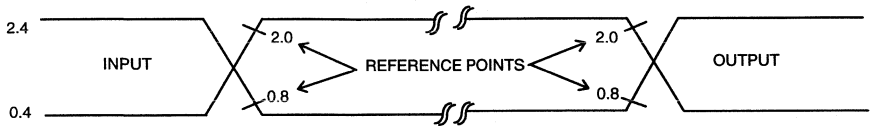


Figure 12: Software ID Exit and Reset



AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a logic "1" and V_{OL} (0.4 V_{TTL}) for a logic "0". Measurement reference points for inputs and outputs are V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Inputs rise and fall times (10% ↔ 90%) are <10 ns.

Figure 13: AC Input/Output Reference Waveforms

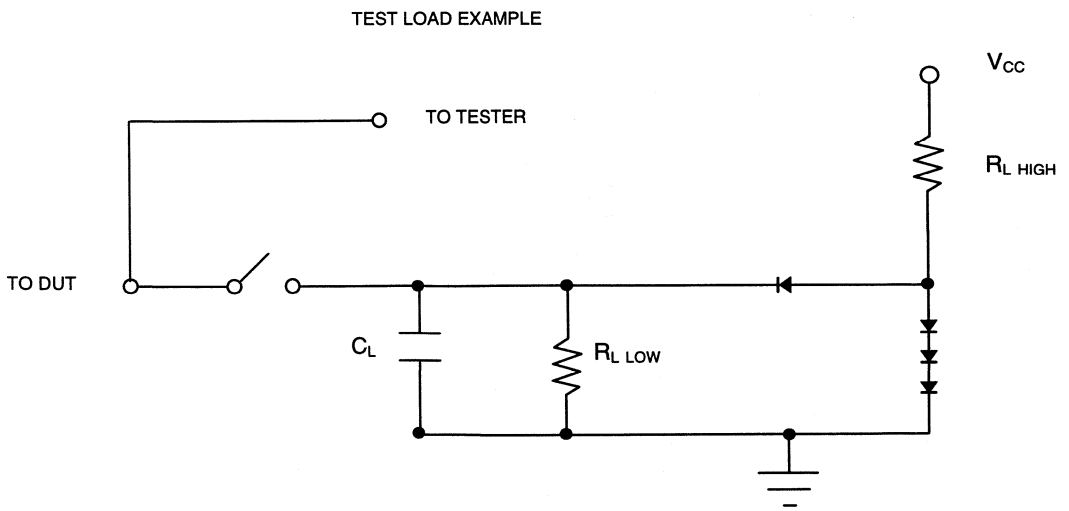


Figure 14: Test Load Example

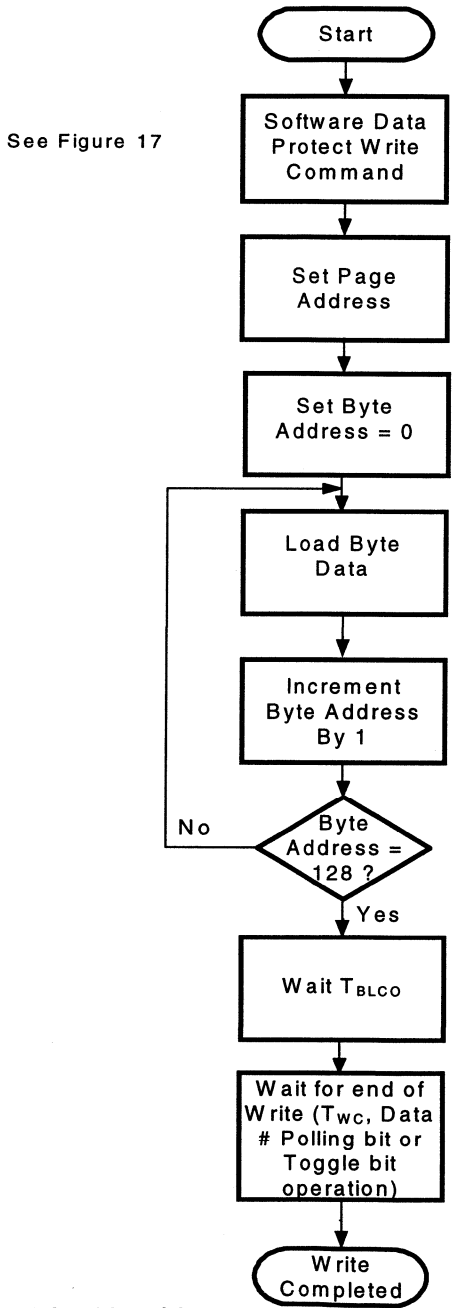


Figure 15: Write Algorithm

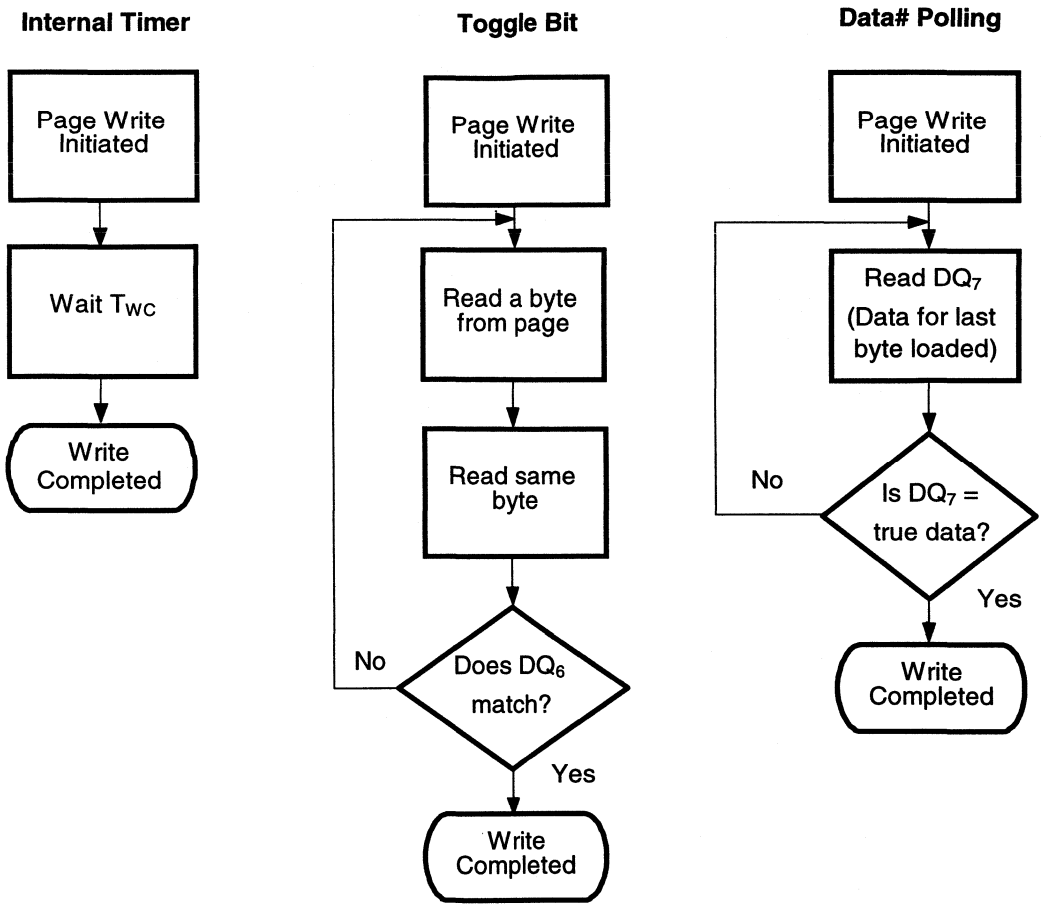


Figure 16: Wait Options

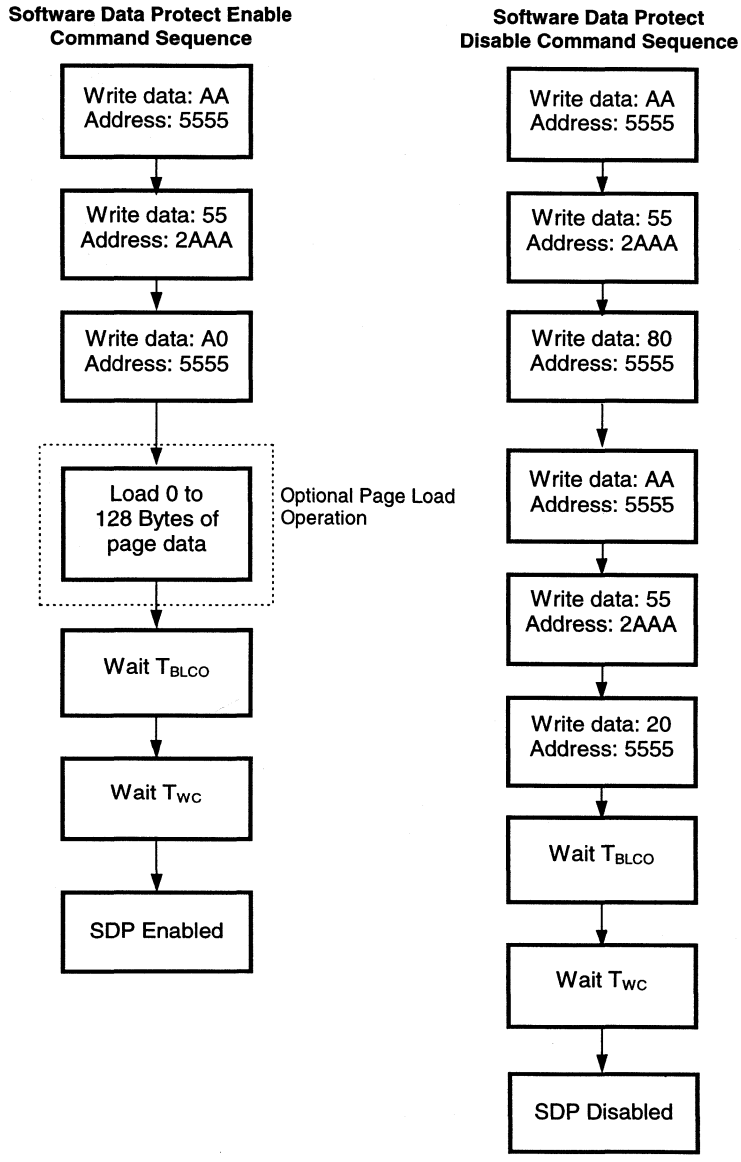


Figure 17: Software Data Protection Flowcharts

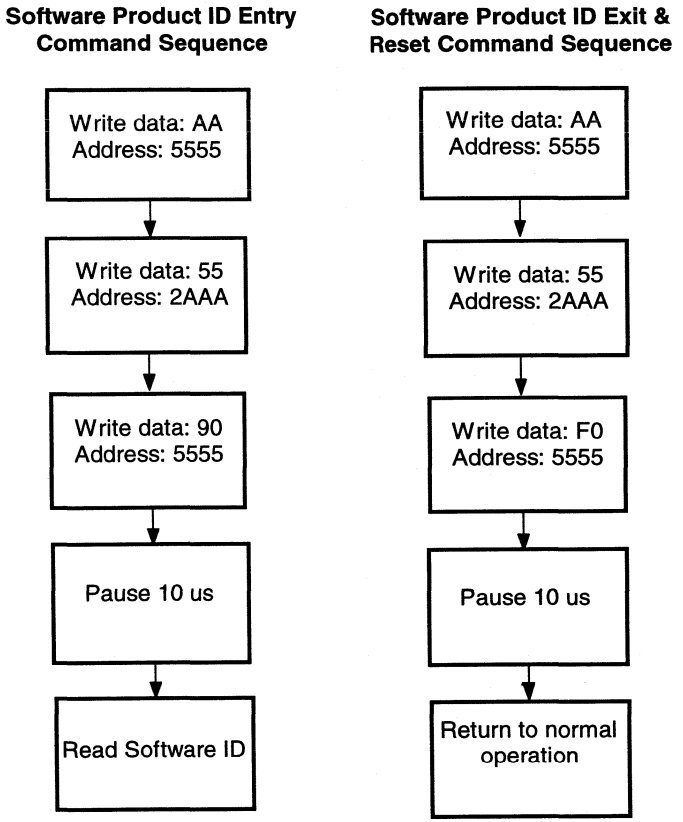


Figure 18: Software Product Command Flowcharts

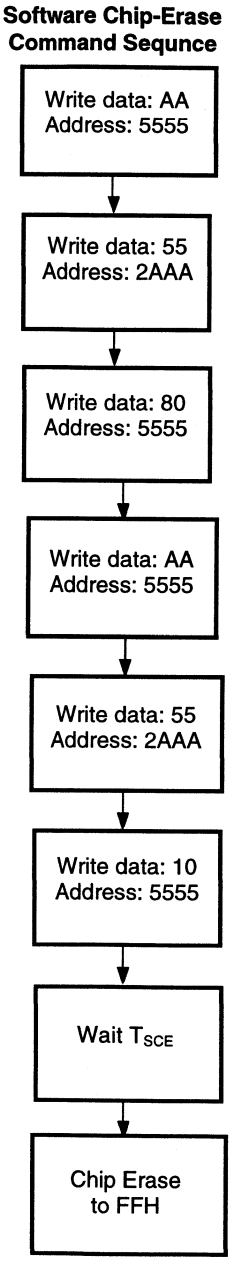


Figure 19: Software Chip Erase Command Codes

Product Ordering Information

Device		Speed		Suffix1		Suffix2
SST29VE020	-	XXX	-	XX	-	XX

Package Modifier
H = 32 leads
Numeric = Die modifier

Package Type
P = PDIP
N = PLCC
E = TSOP (die up)
U = Unencapsulated die

Operating Temperature
C = Commercial = 0° to 70°C
I = Industrial = -40° to 85°C

Minimum Endurance
3 = 1000 cycles
4 = 10,000 cycles

Read Access Speed
300 = 300 ns
250 = 250 ns

Valid combinations

SST29VE020-250-4C-EH	SST29VE020-250-4C-NH	SST29VE020-250-4C-PH
SST29VE020-300-4C-EH	SST29VE020-300-4C-NH	SST29VE020-300-4C-PH
SST29VE020-250-4I-EH	SST29VE020-250-4I-NH	
SST29VE020-300-4I-EH	SST29VE020-300-4I-NH	SST29VE020-300-4C-U1

Example: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Data Sheet

SST 28SF040
5.0V-only 4 Megabit
SuperFlash EEPROM

July 1996

SST 28SF040
5.0V-only 4 Megabit
SuperFlash EEPROM

Features:

Single 5.0-Volt Read and Write Operations
CMOS SuperFlash EEPROM Technology
- Endurance: 100,000 Cycles (typical)
- Greater than 100 years Data Retention

Memory Organization: 512K x 8
Sector Erase Capability: 256 bytes per Sector
Low Power Consumption:
- Active Current: 15 mA (typical)
- Standby Current: 5 µA (typical)

Fast Sector Erase/Byte Program Operation
- Byte Program Time: 30 µs (typical)
- Sector Erase Time: 2 ms (typical)
- Complete Memory Rewrite: 20 sec (typical)

Fast Access Time: 150 and 200 ns
Latched Address and Data
Hardware and Software Data Protection
- 7-Read-Cycle-Sequence Software Data Protection

End of Write Detection
- Toggle Bit
- Data# Polling

TTL I/O Compatibility
Packages Available
- 40-Pin TSOP (10 mm x 20 mm)
- 32-Pin TSOP (8 mm x 20 mm)
- 32-Pin PLCC
- 32-Pin PDIP

Product Description

The 28SF040 is organized as a 512K x 8 bit CMOS sector erase, byte program EEPROM. The 28SF040 is manufactured using SST's proprietary, high performance CMOS SuperFlash EEPROM Technology. The split gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternative approaches. The 28SF040 erases and programs with a 5.0-volt only power supply. The 28SF040 conforms to JEDEC standard pinouts for byte wide memories and is compatible with existing industry standard EPROM, flash EPROM and EEPROM pinouts.

Featuring high performance programming, the 28SF040 typically byte programs in 30 µs. The 28SF040 typically sector erases in 2 ms. Both program and erase times can be optimized using interface features such as Toggle bit or Data# Polling to indicate the completion of the write cycle. To protect against an inadvertent write, the 28SF040 has on chip hardware and software data protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, the 28SF040 is offered with a guaranteed sector endurance of 10^4 and 10^3 cycles. Data retention is rated greater than 100 years.

The 28SF040 is best suited for applications that require reprogrammable nonvolatile mass storage of program, configuration, or data memory. For all system applications, the 28SF040 significantly improves performance and reliability, while lowering power consumption when compared with floppy diskettes or EPROM approaches. EEPROM technology makes possible convenient and economical updating of codes and control programs on-line. The 28SF040 improves flexibility, while lowering the cost of program and configuration storage application.

Figure 1 shows the functional blocks of the 28SF040. Figures 2A, 2B, and 3 show the pin assignments for the 40 pin TSOP, 32 pin TSOP, 32 pin PDIP, and 32 pin PLCC packages. Pin description and operation modes are described in Tables 1 through 4.

Device Operation

Commands are used to initiate the memory operation functions of the device. Commands are written to the device using standard microprocessor write sequences. A command is written by asserting WE# low while keeping CE# low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first. Note, during the software data protection sequence the address are latched on the rising edge of OE# or CE#, whichever occurs first.

Command Definitions

Table 3 contains a command list and a brief summary of the commands. The following is a detailed description of the operations initiated by each command.

Sector_Erase Operation

The Sector_Erase operation erases all bytes within a sector and is initiated by a setup command and an execute command. A sector contains 256 bytes. This sector erasability enhances the flexibility and usefulness of the 28SF040, since most applications only need to change a small number of bytes or sectors, not the entire chip.

The setup command is performed by writing 20H to the device. The execute command is performed by writing D0H to the device. The erase operation begins with the rising edge of the WE# or CE#, whichever occurs first and terminates automatically by using an internal timer. The end of Erase can be determined using either Data# Polling, Toggle Bit, or Successive Reads detection methods. See Figure 9 for timing waveforms.

The two-step sequence of setup command followed by an execute command ensures that only memory contents within the addressed sector are erased and other sectors are not inadvertently erased.

Sector_Erase Flowchart Description

Fast and reliable erasing of the memory contents within a sector is accomplished by following the sector erase flowchart as shown in Figure 18. The entire procedure consists of the execution of two commands. The Sector_Erase operation will terminate after a maximum of 4 ms. A Reset command can be executed to terminate the erase operation; however, if the erase operation is terminated prior to the 4 ms time-out, the sector may not be fully erased. An erase command can be reissued as many times as necessary to complete the erase operation. The 28SF040 cannot be "overerased".

Chip_Erase Operation

The Chip_Erase operation is initiated by a setup command (30H) and an execute command (30H). The Chip_Erase operation allows the entire array of the 28SF040 to erase in one operation, as opposed to 2048 sector erase operations. Using the Chip_Erase operation will minimize the time to rewrite the entire memory array. The Chip_Erase operation will terminate after a maximum of 20 ms. A Reset command can be executed to terminate the erase operation; however, if the erase operation is terminated prior to the 20 ms time-out, the Chip may not be completely erased. If an erase error occurs an erase command can be reissued as many times as necessary to complete the erase operation. The 28SF040 cannot be "overerased". (See Figure 8)

Byte_Program Operation

The Byte_Program operation is initiated by writing the setup command (10H). Once the program setup is performed, programming is executed by the next WE# pulse. See Figures 5 and 6 for timing waveforms. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first, and begins the program operation. The program operation is terminated automatically by an internal timer. See Figure 16 for the programming flowchart.

The two-step sequence of a setup command followed by an execute command ensures that only the addressed byte is programmed and other bytes are not inadvertently programmed.

The Byte_Program Flowchart Description

Programming data into the 28SF040 is accomplished by following the Byte_Program flowchart shown in Figure 16. The Byte_Program command sets up the byte for programming. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first and begins the program operation. The end of program can be detected using either the Data# Polling, Toggle bit, or Successive reads.

Reset Operation

The Reset command is provided as a means to safely abort the erase or program command sequences. Following either setup commands (erase or program) with a write of FFH will safely abort the operation. Memory contents will not be altered. After the Reset command, the device returns to the read mode. The Reset command does not enable software data protection. See Figure 7 for timing waveforms.

Read

The Read operation is initiated by setting CE#, and OE# to logic low and setting WE# to logic high (See Table 2). See Figure 4 for read memory timing waveform. The read operation from the host retrieves data from the array. The device remains enabled for read until another operation mode is accessed. During initial power-up, the device is in the read mode and is software data protected. The device must be unprotected to execute a write command.

The read operation of the 28SF040 is controlled by OE# and CE# at logic low. When CE # is high, the chip is deselected and only standby power will be consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when CE# and OE# are high.

Read_ID operation

The Read_ID operation is initiated by writing a single command (90H). A read of address 0000H will output the manufacturer's code (BFH). A read of address 0001H will output the device code (04H). Any other valid command will terminate this operation.

Data Protection

In order to protect the integrity of nonvolatile data storage, the 28SF040 provides both hardware and software features to prevent inadvertent writes to the device, for example, during system power-up or power-down. Such provisions are described below.

Hardware Data Protection

The 28SF040 is designed with hardware features to prevent inadvertent writes. This is done in the following ways:

1. Write Inhibit Mode: OE# low, CE#, or WE# high will inhibit the write operation.
2. Noise/Glitch Protection: A WE# pulse width of less than 15 ns will not initiate a write cycle.
3. V_{CC} Power Up/Down Detection: The write operation is inhibited when V_{CC} is less than 2.5V.
4. After power-up the device is in the read mode and the device is in the software data protect state.

Software Data Protection (SDP)

The 28SF040 has software methods to further prevent inadvertent writes. In order to perform an erase or program operation, a two-step command sequence consisting of a set-up command followed by an execute command avoids inadvertent erasing and programming of the device.

The 28SF040 will default to software data protection after power up. A sequence of seven consecutive reads at specific addresses will unprotect the device The address sequence is 1823H, 1820H, 1822H, 0418H, 041BH, 0419H, 041AH. The address bus is latched on the rising edge of OE# or CE#, whichever occurs first. A similar seven read sequence of 1823H, 1820H, 1822H, 0418H, 041BH, 0419H, 040AH will protect the device. Also refer to Figures 10 and 11 for the 7 read cycle sequence Software Data Protection. The I/O pins can be in any state (i.e., high, low, or tristate).

Write Operation Status Detection

The 28SF040 provides three means to detect the completion of a write cycle, in order to optimize the system write cycle time. The end of a write cycle (erase or program) can be detected by three means: 1) monitoring the Data# Polling bit; 2) monitoring the Toggle bit; or 3) by two successive read of the same data. These three detection mechanisms are described below.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with the DQ used. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the write cycle, otherwise the rejection is valid.

Data# Polling (DQ_7)

The 28SF040 features Data# Polling to indicate the write operation status. During a write operation, any attempt to read the last byte loaded during the byte-load cycle will receive the complement of the true data on DQ_7. Once the write cycle is completed, DQ_7 will show true data. The

device is then ready for the next operation. See Figure 12 for Data Polling timing waveforms. In order for Data# Polling to function correctly , the byte being polled must be erased prior to programming.

Toggle Bit (DQ_6)

An alternative means for determining the write operation status is by monitoring the Toggle Bit, DQ_6. During a write operation, consecutive attempts to read data from the device will result in DQ_6 toggling between logic 0 (low) and logic 1 (high). When the write cycle is completed, the toggling will stop. The device is then ready for the next operation. See Figure 13 for Toggle Bit timing waveforms.

Successive Reads

An Alternative means for determining an end of a write cycle is by reading the same address for two consecutive data matches.

Product Identification

The Product Identification mode identifies the device as 28SF040 and the manufacturer as SST. This mode may be accessed by hardware and software operations. The hardware operation is typically used by an external programmer to identify the correct algorithm for the 28SF040. Users may wish to use the software operation to identify the device (i.e., using the device code). For details see Table 2 for the hardware operation and Figure 19 for the software operation. The manufacturer and device codes are the same for both operations.

Product Identification Table

	Byte	Data
Manufacturer Code	0000 H	BF H
Device Code	0001 H	04 H

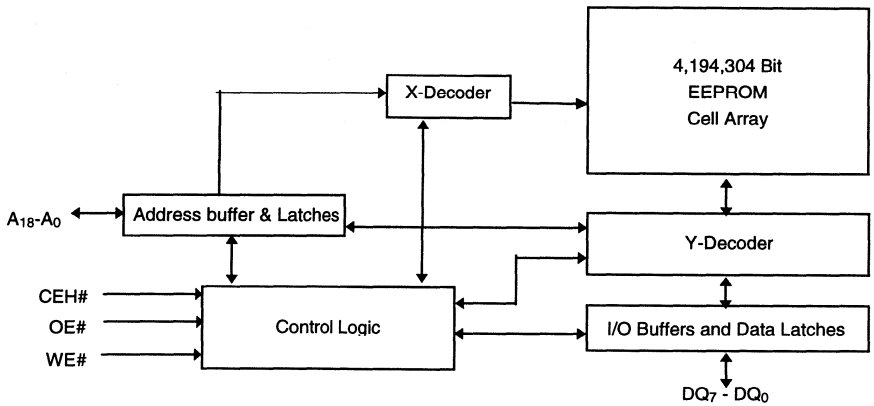


Figure 1: Functional Block Diagram of SST 28SF040

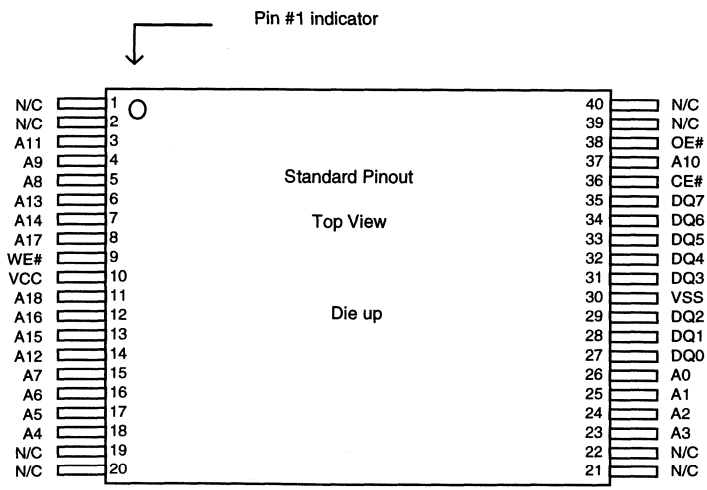


Figure 2A: Standard Pin Assignments for 40-pin TSOP Packages

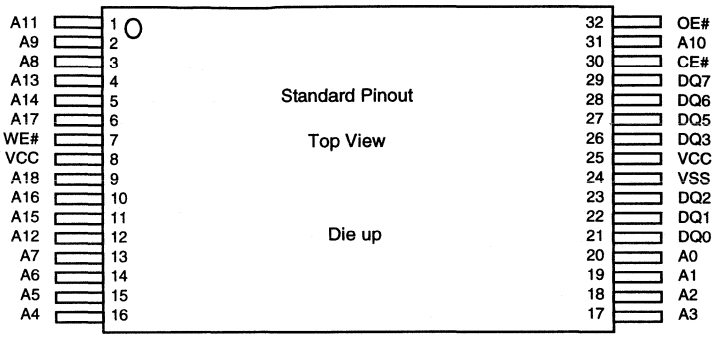


Figure 2B: Standard Pin Assignments for 32-pin TSOP Packages

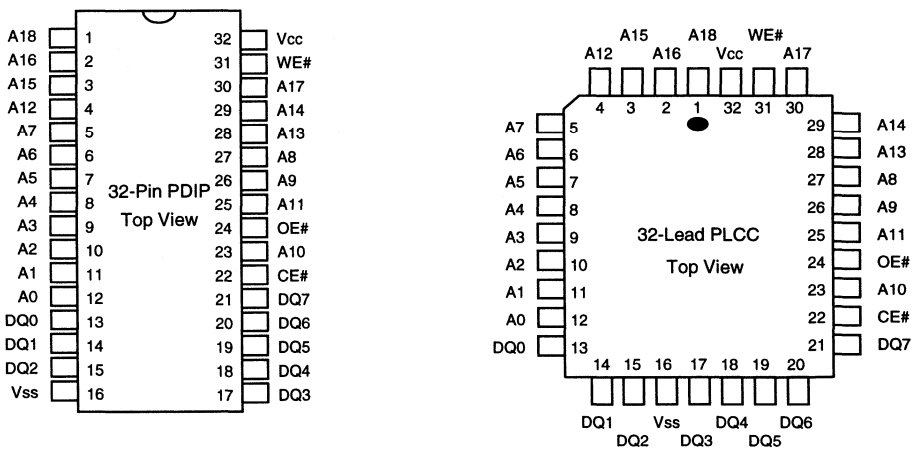


Figure 3: Pin Assignments for 32-pin Plastic DIPs and 32-pin PLCCs

Table 1: Pin Description

Symbol	Pin Name	Functions
A_{18}-A_8	Row Address Inputs	To provide memory addresses. Row addresses define a sector.
A_7-A_0	Column Address Inputs	Selects the byte within the sector.
DQ_7-DQ_0	Data Input/Output	To output data during read cycles and receive input data during write cycles. Data is internally latched during a write cycle. The outputs are in tri-state when OE#, CE # is high.
CE#	Chip Enable	To activate the device when CE # is low. (1)
OE#	Output Enable	To gate the data output buffers. (1)
WE#	Write Enable	To control the write operations. (1)
Vcc	Power Supply	To provide 5-volt supply (± 10%)
Vss	Ground	

Note: (1) This pin is considered an input for the purposes of the DC Operation Characteristics Table.

Table 2: Operation Modes Selection

Mode	CE#	OE#	WE#	DQ	Address
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	A_{IN}
Byte Program	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}, See Table 3
Sector Erase	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}, See Table 3
Standby	V_{IH}	X	X	High Z	X
Write Inhibit	X	V_{IL}	X	High Z/ D_{OUT}	X
Write Inhibit	X	X	V_{IH}	High Z/ D_{OUT}	X
Software Chip Erase	V_{IL}	V_{IH}	V_{IL}	D_{IN}	See Table 3
Product Identification					
Hardware Mode	V_{IL}	V_{IL}	V_{IH}	Manufacturer Code (BF)	A_{18}-A_1=V_{IL}, A_9=V_H, A_0=V_{IL}
				Device Code (04)	A_{18}-A_1=V_{IL}, A_9=V_H, A_0=V_{IH}
Software Mode	V_{IL}	V_{IH}	V_{IL}		See Table 3
SDP Enable & Disable Mode	V_{IL}	V_{IH}	V_{IL}		See Table 3
Reset	V_{IL}	V_{IH}	V_{IL}		See Table 3

Table 3: Software Command Summary

Command Summary	Required Cycle(s)	Setup Command Cycle			Execute Command Cycle			SDP[5]
		Type[1]	Addr[2,3]	Data[4]	Type[1]	Addr[2,3]	Data[4]	
Sector_Erase	2	W	X	20H	W	SA	D0H	N
Byte_Program	2	W	X	10H	W	PA	PD	N
Chip_Erase	2	W	X	30H	W	X	30H	N
Reset	1	W	X	FFH				Y
Read_ID	3	W	X	90H	R	(8)	(8)	Y
Software_Data_Protect	7	R	(6)					
Software_Data_Unprotect	7	R	(7)					

Notes:

1. Type definition: W = Write, R = Read, X= don't care
2. Addr (Address) definition: SA = Sector Address = A_{18} - A_8, sector size = 256 bytes; A_7- A_0 = X for this command.
3. Addr (Address) definition: PA = Program Address = A_{18} - A_0.
4. Data definition: PD = Program Data, H = number in hex.
5. SDP = Software Data Protect mode using 7 Read Cycle Sequence.
   a) Y = the operation can be executed with protection enabled
   b) N = the operation cannot be executed with protection enabled
6. Refer to Figure 11 for the 7 Read Cycle sequence for Software_Data_Protect.
7. Refer to Figure 10 for the 7 Read Cycle sequence for Software_Data_Unprotect.
8. Address 0000H retrieves the manufacturer' code of BFH and address 0001H retrieves the device code of 04H.

Table 4: Memory Array Detail

Sector Select	Byte Select
A_{18} - A_8	A_7 - A_0

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential ..... -0.5V to V_{CC}+ 0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential ..... -1.0V to V_{CC}+ 1.0V
Voltage on A_9 Pin to Ground Potential ..... -0.5V to 14.0V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Through Soldering Temperature (10 Seconds)..... 300°C
Surface Mount Lead Soldering Temperature (3 Seconds) ..... 240°C
Output Short Circuit Current[1] ..... 100 mA

Note: [1] Outputs shorted for no more than one second. No more than one output shorted at a time.

Table 5: Operating Range

Range	Ambient Temp	V_{CC}
Commercial	0 °C to +70 °C	5V±10%
Industrial	-40 °C to +85 °C	5V±10%

Table 6: AC Conditions of Test

Input Rise/Fall Time.....10 ns
Output Load.....1 TTL Gate and C_L = 100 pF
See Figures 14 and 15

Table 7: DC Operating Characteristics

Symbol	Parameter	Limits		Units	Test Conditions
		Min	Max		
I_{CC}	Power Supply Current				CE# = OE# =V_{IL}, WE# =V_{IH}, all I/Os open
	Read		25	mA	Address input = V_{IL}/V_{IH}, at f=1/T_{RC} Min. V_{CC} = V_{CC} Max
	Program and Erase		40	mA	CE# =WE# =V_{IL}, OE# =V_{IH} V_{CC} =V_{CC} Max.
I_{SB1}	Standby V_{CC} Current (TTL input)		3	mA	CE# =OE# =WE# = V_{IH}, V_{CC}=V_{CC} Max
I_{SB2}	Standby V_{CC} Current (CMOS input)		20	µA	CE# = OE# = WE# = V_{CC} -0.3V, V_{CC}=V_{CC} Max
I_{LI}	Input Leakage Current		1	µA	V_{IN} = GND to V_{CC}, V_{CC} = V_{CC} Max.
I_{LO}	Output Leakage Current		10	µA	V_{OUT} =GND to V_{CC}, V_{CC} = V_{CC} Max.
V_{IL}	Input Low Voltage		0.8	V	V_{CC} = V_{CC} Max.
V_{IH}	Input High Voltage	2.0		V	V_{CC} = V_{CC} Max.
V_{OL}	Output Low Voltage		0.4	V	I_{OL}= 2.1 mA, V_{CC} = V_{CC} Min.
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400 µA, V_{CC} = V_{CC} Min.
V_H	Supervoltage for A_9	11.6	12.4	V	CE#=OE#=V_{IL},WE#=V_{IH}
I_H	Supervoltage Current for A_9		200	µA	CE#=OE#=V_{IL},WE#=V_{IH}, A_9 = V_H Max.

Table 8: Power-up Timings

Symbol	Parameter	Maximum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	10	ms
$T_{PU-WRITE}$[1]	Power-up to Write Operation	10	ms

Table 9: Capacitance (Ta = 25 °C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0v	6 pF

Note: [1]This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 10: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}	Endurance	1,000 & 10,000[2]	Cycles	MIL-STD-883, Method 1033
T_{DR}[1]	Data Retention	100	Years	MIL-STD-883, Method 1008
V_{ZAP_HBM}[1]	ESD Susceptibility Human Body Model	1000	Volts	MIL-STD-883, Method 3015
V_{ZAP_MM}[1]	ESD Susceptibility Machine Model	200	Volts	JEDEC
I_{LTH}[1]	Latch Up	100	mA	JEDEC Standard 17

Note: [1]This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

[2]See Ordering Information for desired type.

AC Characteristics

Table 11: Read Cycle Timing Parameters

IEEE Symbol	Industry Symbol	Parameter	28SF040-150		28SF040-200		Units
			Min	Max	Min	Max	
tAVAV	T_{RC}	Read Cycle Time	150		200		ns
tAVQV	T_{AA}	Address Access Time		150		200	ns
tELQV	T_{CE}	Chip Enable Access Time		150		200	ns
tGLQV	T_{OE}	Output Enable Access Time		70		75	ns
tEHQZ	T_{CLZ}[1]	CE# Low to Active Output	0		0		ns
tGHQZ	T_{OLZ}[1]	OE# Low to Active Output	0		0		ns
tELQX	T_{CHZ}[1]	CE# High to High-Z Output		40		40	ns
tGLQX	T_{OHZ}[1]	OE# High to High-Z Output		40		40	ns
tAXQX	T_{OH}[1]	Output Hold from Address Change	0		0		ns

Table 12: Erase/Program Cycle Timing Parameters

IEEE Symbol	Industry Symbol	Parameter	28SF040-150		28SF040-200		Units
			Min	Max	Min	Max	
tAVA	T_{BP}	Byte Program Cycle Time		35		35	µs
tWLWH	T_{WP}	Write Pulse Width (WE#)	80		100		ns
tAVWL	T_{AS}	Address Setup Time	10		10		ns
tWLAX	T_{AH}	Address Hold Time	50		50		ns
tELWL	T_{CS}	CE# Setup Time	0		0		ns
tWHEX	T_{CH}	CE# Hold Time	0		0		ns
tGHWL	T_{OES}	OE# High Setup Time	10		10		ns
tWGL	T_{OEH}	OE# High Hold Time	10		10		ns
tWLEH	T_{CP}	Write Pulse Width (CE#)	80		100		ns
tDVWH	T_{DS}	Data Setup Time	50		50		ns
tWHDX	T_{DH}	Data Hold Time	10		10		ns
tWHWL2	T_{SE}	Sector Erase Cycle Time		4		4	ms
	T_{RST}[1]	Reset Command Recovery Time		4		4	µs
tWHWL3	T_{SCE}	Software Chip_Erase Cycle Time		20		20	ms
tEHEL	T_{CPH}	CE# High Pulse Width	50		50		ns
tWHWL1	T_{WPH}	WE# High Pulse Width	50		50		ns
	T_{PCP}[1]	Protect Chip Enable Pulse Width	10		10		ns
	T_{PCH}[1]	Protect Chip Enable High Time	10		10		ns
	T_{PAS}[1]	Protect Address Setup Time	0		0		ns
	T_{PAH}[1]	Protect Address Hold Time	50		50		ns

Note: [1]This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.

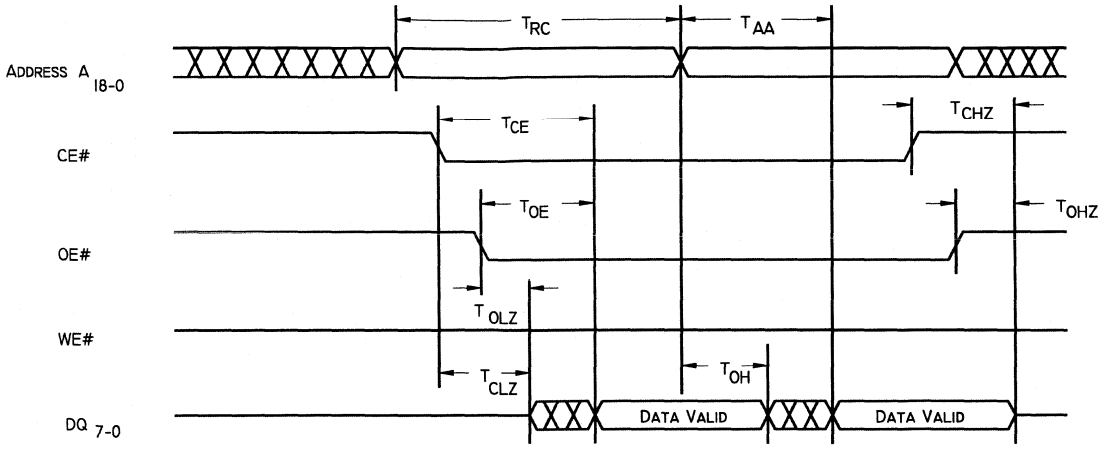


Figure 4: Read Cycle Timing Diagram

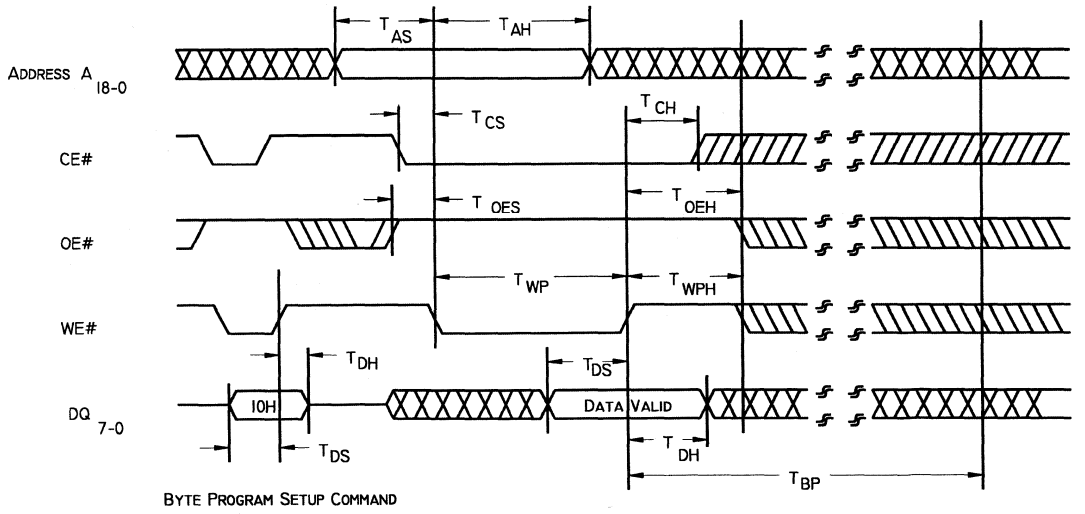


Figure 5: WE# Controlled Byte Program Timing Diagram

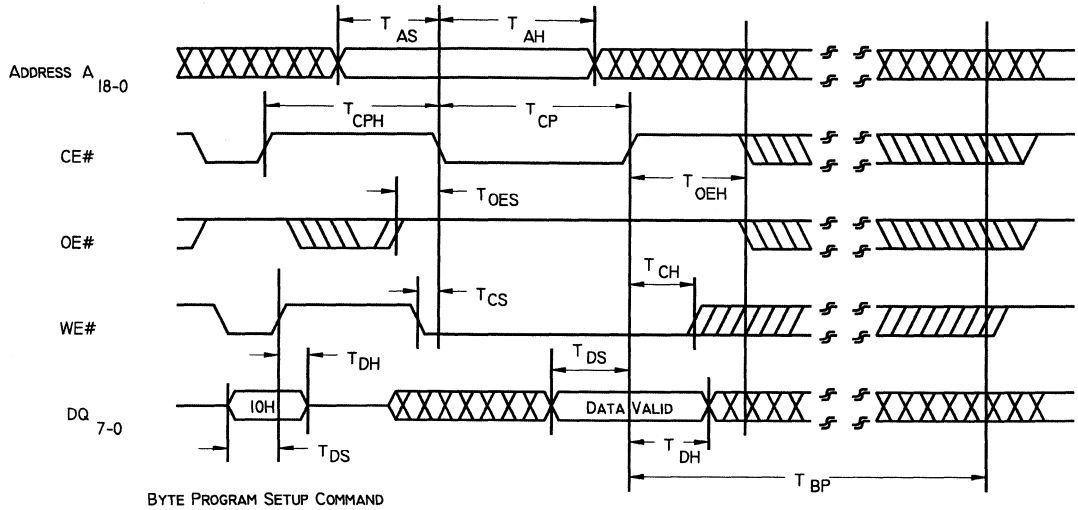


Figure 6: CE# Controlled Byte Program Timing Diagram

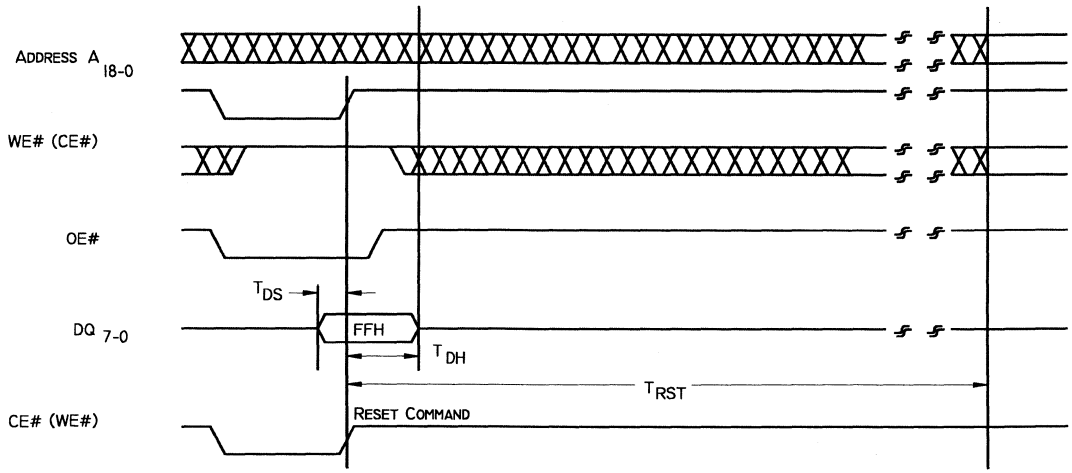


Figure 7: Reset Command Timing Diagram

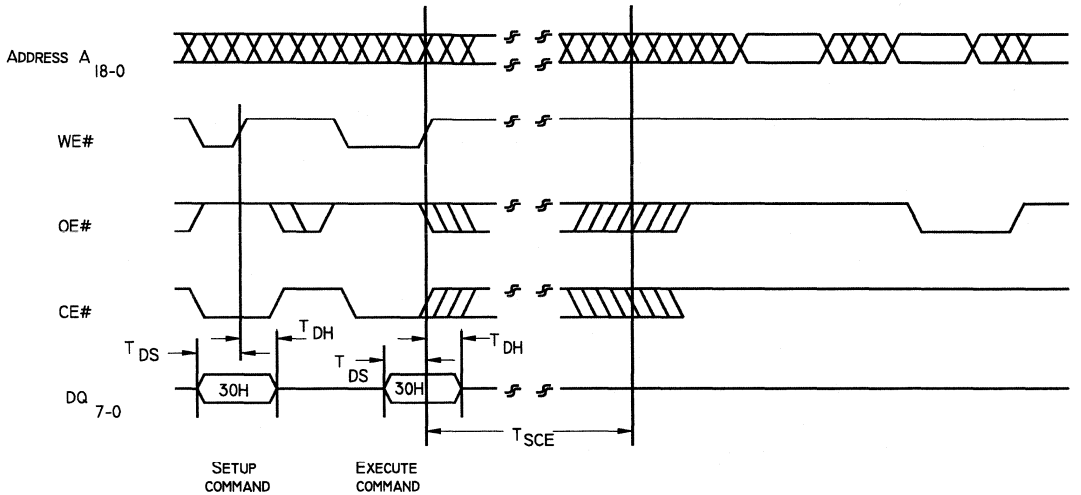


Figure 8: Chip_Erase Timing Diagram

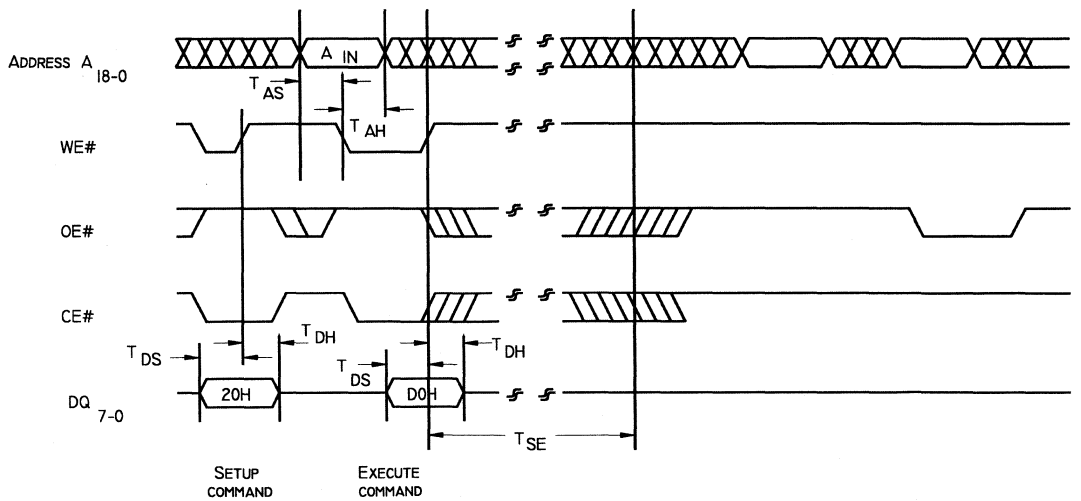
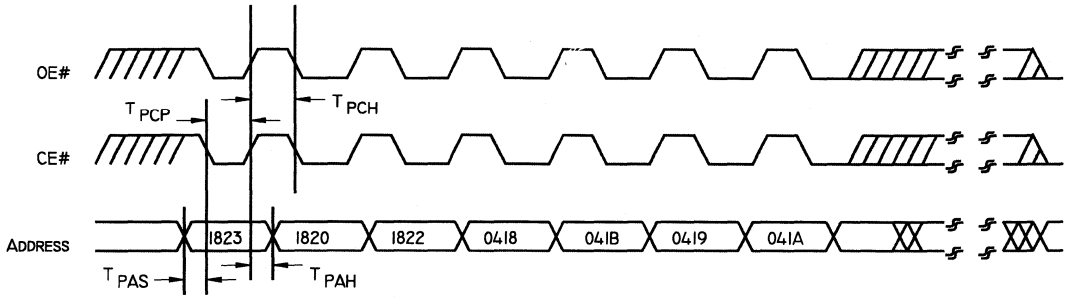


Figure 9: Sector Erase Timing Diagram



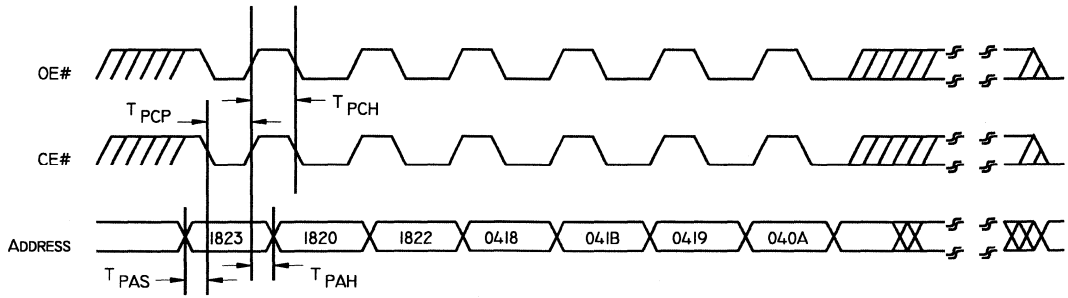
NOTE : A. ADDRESSES ARE LATCHED INTERNALLY ON THE RISING EDGE OF:

1. OE# IF CE# IS KEPT AT LOW ALL TIME.
2. CE# IF OE# IS KEPT AT LOW ALL TIME.
3. THE FIRST PIN TO GO HIGH IF BOTH ARE TOGGLED.

B. ABOVE ADDRESS VALUES ARE IN HEX.

C. ADDRESSES > A_{12} ARE "DON'T CARE"

Figure 10: Software Data Unprotect Timing Diagram



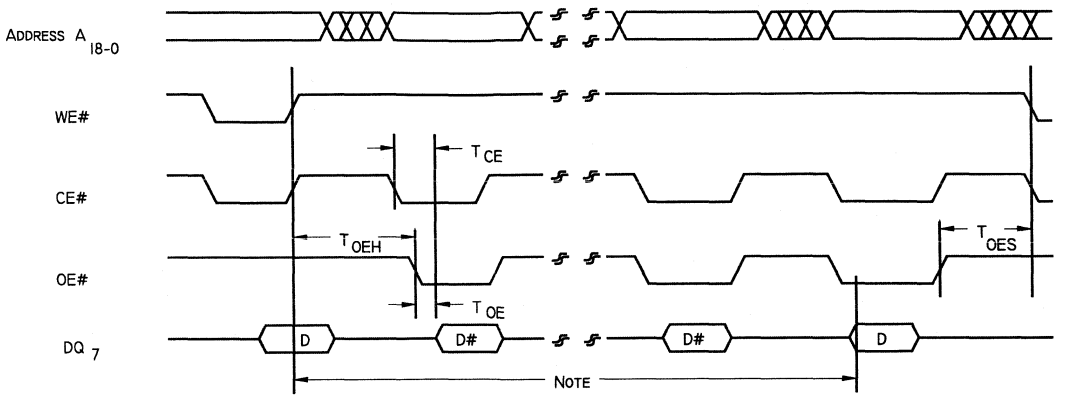
NOTE : A. ADDRESSES ARE LATCHED INTERNALLY ON THE RISING EDGE OF:

1. OE# IF CE# IS KEPT AT LOW ALL TIME.
2. CE# IF OE# IS KEPT AT LOW ALL TIME.
3. THE FIRST PIN TO GO HIGH IF BOTH ARE TOGGLED.

B. ABOVE ADDRESS VALUES ARE IN HEX.

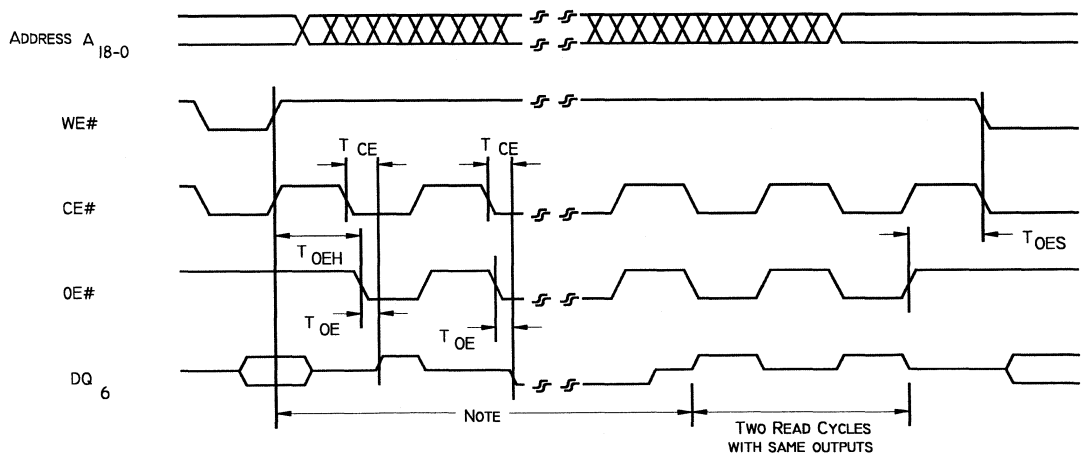
C. ADDRESSES > A_{12} ARE "DON'T CARE"

Figure 11: Software Data Protect Timing Diagram



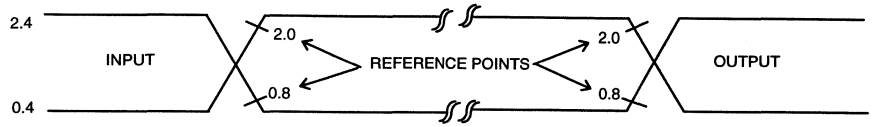
NOTE: THIS TIME INTERVAL SIGNAL CAN BE T_{SE} OR T_{BP} DEPENDING UPON THE SELECTED OPERATION MODE.

Figure 12: Data# Polling Timing Diagram



NOTE: THIS TIME INTERVAL SIGNAL CAN BE T_{SE} OR T_{BP} , DEPENDING UPON THE SELECTED OPERATION MODE.

Figure 13: Toggle Bit Timing Diagram



AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a logic "1" and V_{OL} (0.4 V_{TTL}) for a logic "0". Measurement reference points for inputs and outputs are V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Inputs rise and fall times (10% ↔ 90%) are <10 ns.

Figure 14: AC Input/Output Reference Waveform

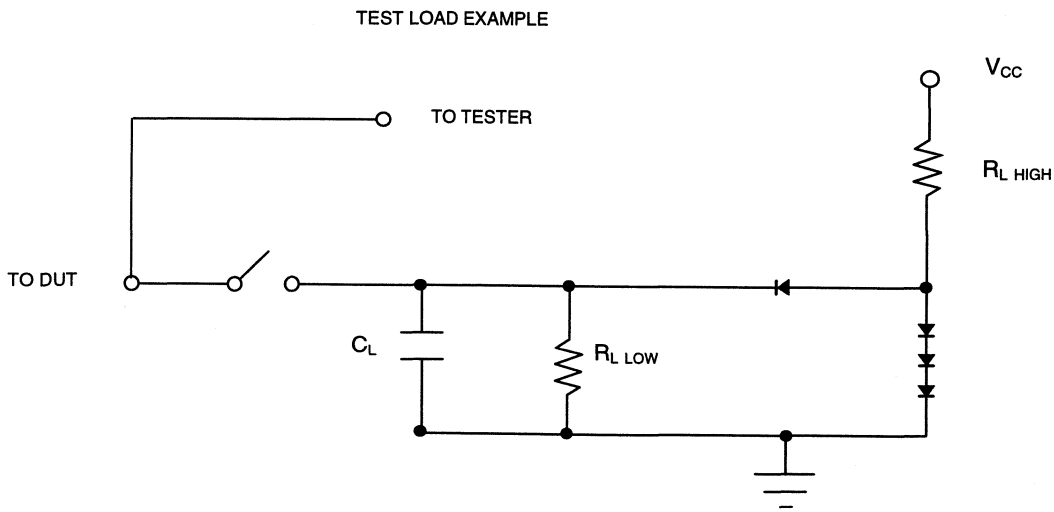


Figure 15: Test Load Example

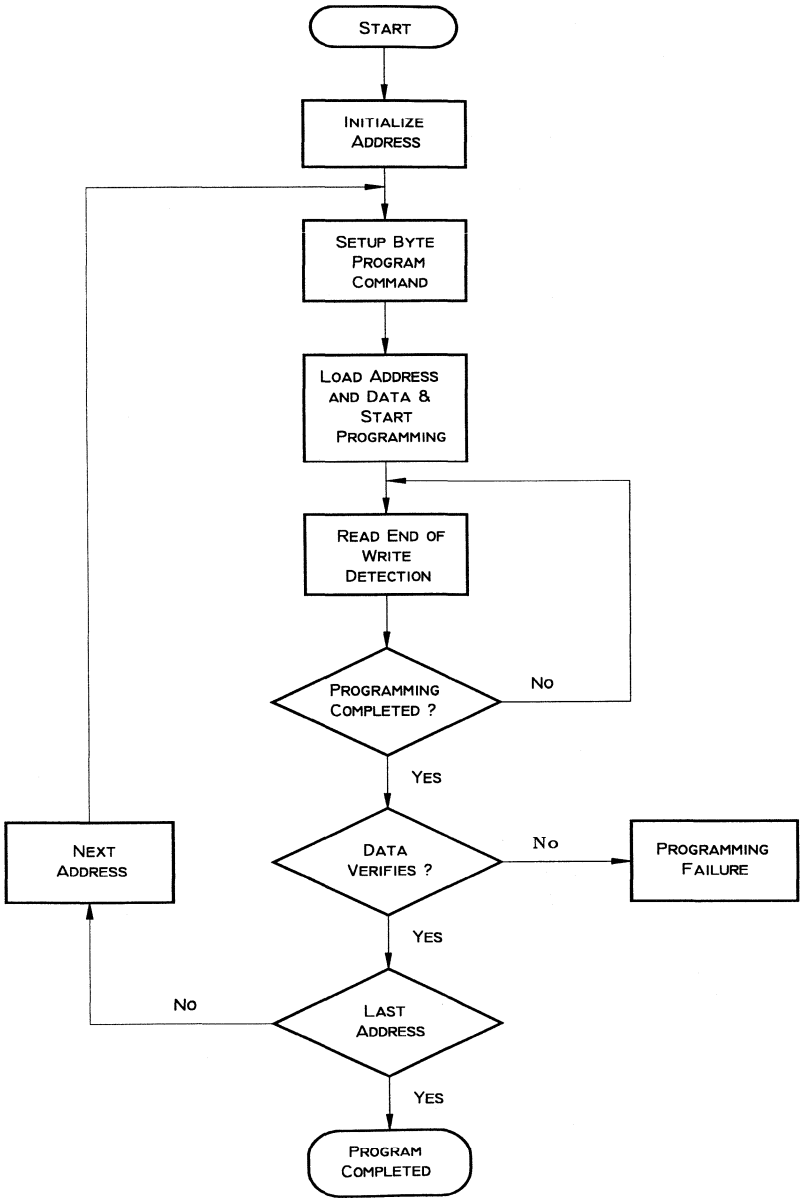


Figure 16: Byte Program Flowchart

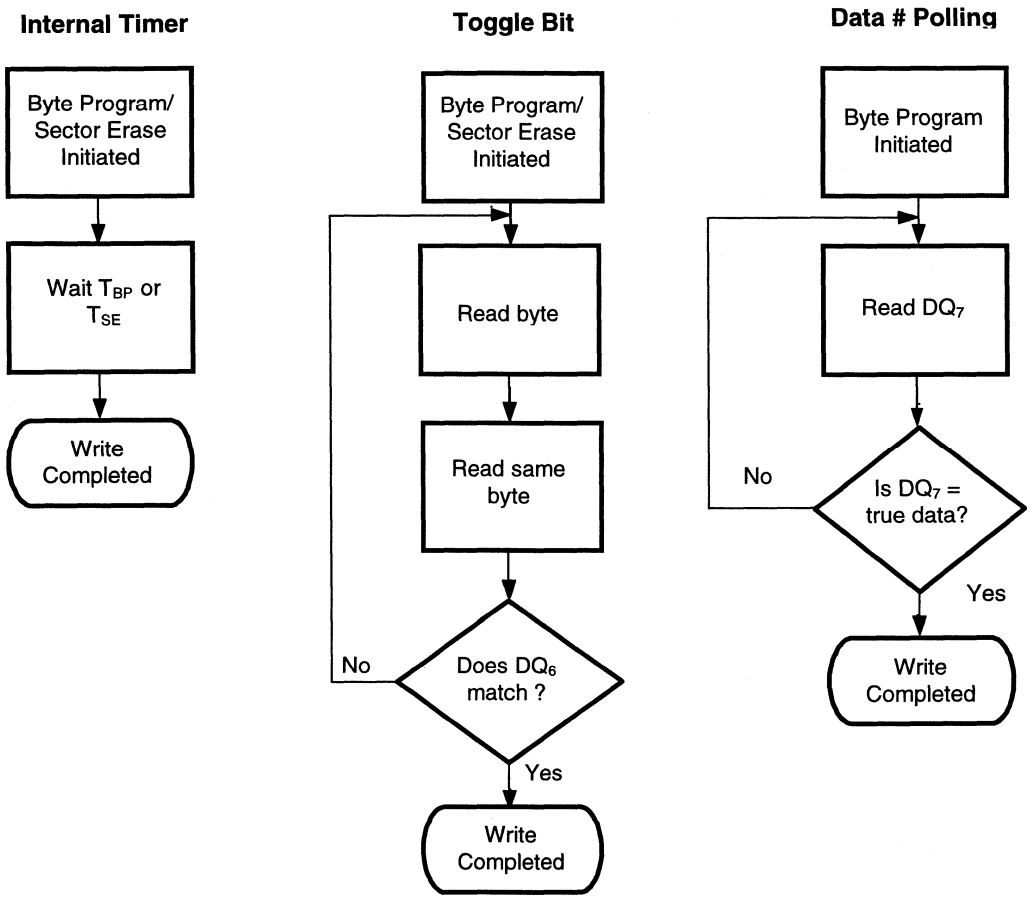


Figure 17: Write Wait Options

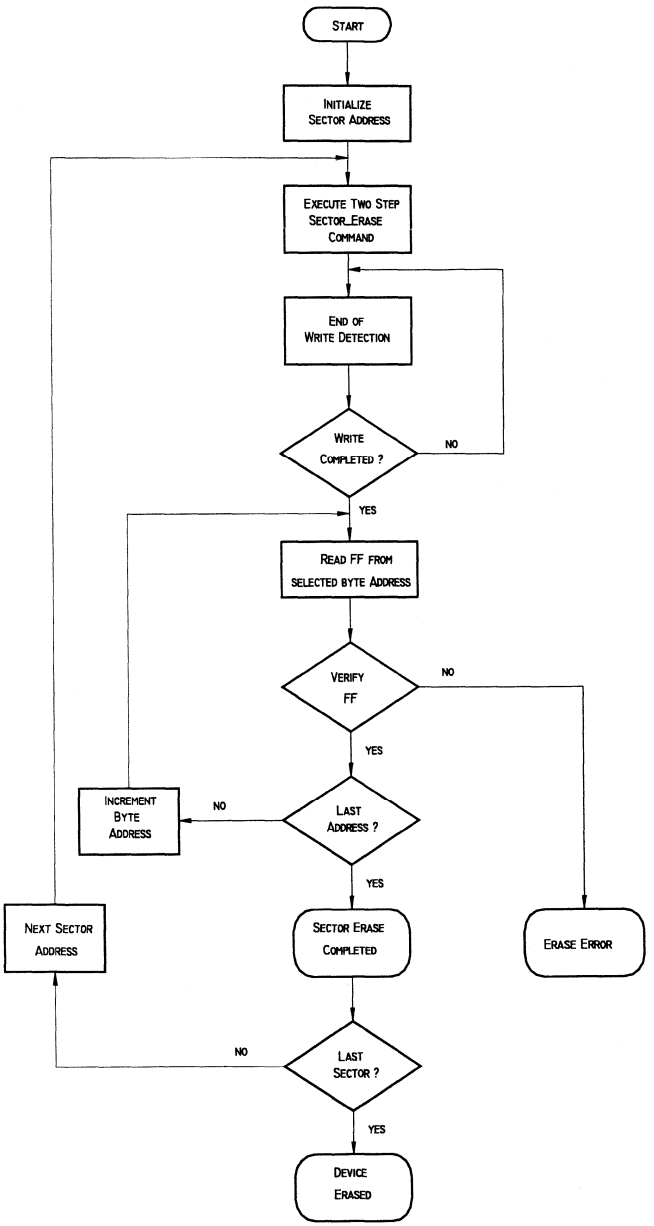


Figure 18: Sector_Erase Flowchart

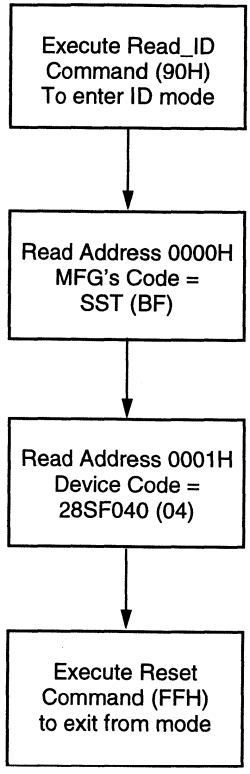


Figure 19: Software Product ID Flow

Product Ordering Information

Device		Speed		Suffix1		Suffix2
SST28SF040	-	XXX	-	XX	-	XX

Package Modifier
I =40 leads
H = 32 leads
Numeric = Die modifier

Package Type
P = PDIP
N = PLCC
E = TSOP (die up)
U = Unencapsulated die

Operating Temperature
C = Commercial = 0° to 70°C

Minimum Endurance
3 = 1000 cycles
4 = 10,000 cycles

Read Access Speed
200 = 200 ns
150 = 150 ns

Valid combinations

SST28SF040-150-4C- EH	SST28SF040-150-4C- EI	SST28SF040-150-4C- NH
SST28SF040-150-4C- PH		
SST28SF040-200-4C- EH	SST28SF040-200-4C- EI	SST28SF040-200-4C- NH
SST28SF040-200-4C- PH	SST28SF040-200-4C- U1	
SST28SF040-150-3C- EH	SST28SF040-150-3C- EI	SST28SF040-150-3C- NH
SST28SF040-150-3C- PH		
SST28SF040-200-3C- EH	SST28SF040-200-3C- EI	SST28SF040-200-3C- NH
SST28SF040-200-3C- PH	SST28SF040-200-3C- U1	
SST28SF040-150-4I- EH	SST28SF040-150-4I- EI	SST28SF040-150-4I- NH
SST28SF040-200-4I- EH	SST28SF040-200-4I- EI	SST28SF040-200-4I- NH
SST28SF040-150-3I- EH	SST28SF040-150-3I- EI	SST28SF040-150-3I- NH
SST28SF040-200-3I- EH	SST28SF040-200-3I- EI	SST28SF040-200-3I- NH

Example: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Data Sheet

SST 28LF040
3.0V-only 4 Megabit
SuperFlash EEPROM

July 1996

SST 28LF040
3.0V-only 4 Megabit SuperFlash EEPROM

Features:

Single 3.0-Volt Read and Write Operations
CMOS SuperFlash EEPROM Technology
Endurance: 100,000 Cycles (typical)
Greater than 100 years Data Retention
Memory Organization: 512K x 8
Sector Erase Capability: 256 bytes per Sector
Low Power Consumption:
Active Current: 10 mA (typical)
Standby Current: 5 µA (typical)
Fast Sector Erase/Byte Program Operation
Byte Program Time: 30 µs (typical)
Sector Erase Time: 2 ms (typical)
Complete Memory Rewrite: 20 sec (typical)
Fast Access Time: 200 and 250 ns
Latched Address and Data
Hardware and Software Data Protection
7-Read-Cycle-Sequence Software Data Protection
End of Write Detection
Toggle Bit
Data# Polling
TTL I/O Compatibility
Packages Available
40-Pin TSOP (10 mm x 20 mm)
32-Pin TSOP (8 mm x 20 mm)
32-Pin PLCC
32-Pin PDIP

Product Description

The 28LF040 is organized as a 512K x 8 (bits) CMOS sector erase, byte program EEPROM. The 28LF040 is manufactured using SST's proprietary, high performance CMOS SuperFlash EEPROM Technology. The split gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternative approaches. The 28LF040 erases and programs with a 3.0 volt only power supply. (V_{CC}: 3.0V to 3.6V) The 28LF040 conforms to JEDEC standard pinouts for byte wide memories and is compatible with existing industry standard EPROM, flash EPROM and EEPROM pinouts.

Featuring high performance programming, the 28LF040 typically byte programs in 30 µs. The 28LF040 typically sector erases in 2 ms. Both program and erase times can be optimized using interface features such as Toggle bit or Data# Polling to indicate the completion of the write cycle. To protect against an inadvertent write, the 28LF040 has on chip hardware and software data protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, the 28LF040 is offered with a guaranteed sector endurance of 10^4 and 10^3 cycles. Data retention is rated greater than 100 years.

The 28LF040 is best suited for applications that require reprogrammable nonvolatile mass storage of program, configuration, or data memory. For all system applications, the 28LF040 significantly improves performance and reliability, while lowering power consumption when compared with floppy diskettes or EPROM approaches. EEPROM technology makes possible convenient and economical updating of codes and control programs on-line. The 28LF040 improves flexibility, while lowering the cost of program and configuration storage application.

Figure 1 shows the functional blocks of the 28LF040. Figures 2A, 2B, and 3 show the pin assignments for the 40 pin TSOP, 32 pin TSOP, 32 pin PDIP, and 32 pin PLCC packages. Pin description and operation modes are described in Tables 1 through 4.

Device Operation

Commands are used to initiate the memory operation functions of the device. Commands are written to the device using standard microprocessor write sequences. A command is written by asserting WE# low while keeping CE# low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first. Note, during the software data protection sequence the address are latched on the rising edge of OE# or CE#, whichever occurs first.

Command Definitions

Table 3 contains a command list and a brief summary of the commands. The following is a detailed description of the operations initiated by each command.

Sector_Erase Operation

The Sector_Erase operation erases all bytes within a sector and is initiated by a setup command and an execute command. A sector contains 256 bytes. This sector erasability enhances the flexibility and usefulness of the 28LF040, since most applications only need to change a small number of bytes or sectors, not the entire chip.

The setup command is performed by writing 20H to the device. The execute command is performed by writing D0H to the device. The erase operation begins with the rising edge of the WE# or CE#, whichever occurs first and terminates automatically by using an internal timer. The end of Erase can be determined using either Data# Polling, Toggle Bit, or Successive Reads detection methods. See Figure 9 for timing waveforms.

The two-step sequence of setup command followed by an execute command ensures that only memory contents within the addressed sector are erased and other sectors are not inadvertently erased.

Sector_Erase Flowchart Description

Fast and reliable erasing of the memory contents within a sector is accomplished by following the sector erase flowchart as shown in Figure 18. The entire procedure consists of the execution of two commands. The Sector_Erase operation will terminate after a maximum of 4 ms. A Reset command can be executed to terminate the erase operation; however, if the erase operation is terminated prior to the 4 ms time-out, the sector may not be fully erased. An erase command can be reissued as many times as necessary to complete the erase operation. The 28LF040 cannot be "overerased".

Chip_Erase Operation

The Chip_Erase operation is initiated by a setup command (30H) and an execute command (30H). The Chip_Erase operation allows the entire array of the 28LF040 to erase in one operation, as opposed to 2048 sector erase operations. Using the Chip_Erase operation will minimize the time to rewrite the entire memory array. The Chip_Erase operation will terminate after a maximum of 20 ms. A Reset command can be executed to terminate the erase operation; however, if the erase operation is terminated prior to the 20 ms time-out, the Chip may not be completely erased. If an erase error occurs an erase command can be reissued as many times as necessary to complete the erase operation. The 28LF040 cannot be "overerased". (See Figure 8)

Byte_Program Operation

The Byte_Program operation is initiated by writing the setup command (10H). Once the program setup is performed, programming is executed by the next WE# pulse. See Figures 5 and 6 for timing waveforms. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first, and begins the program operation. The program operation is terminated automatically by an internal timer. See Figure 16 for the programming flowchart.

The two-step sequence of a setup command followed by an execute command ensures that only the addressed byte is programmed and other bytes are not inadvertently programmed.

The Byte_Program Flowchart Description

Programming data into the 28LF040 is accomplished by following the Byte_Program flowchart shown in Figure 16. The Byte_Program command sets up the byte for programming. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first and begins the program operation. The end of program can be detected using either the Data# Polling, Toggle bit, or Successive reads.

Reset Operation

The Reset command is provided as a means to safely abort the erase or program command sequences. Following either setup commands (erase or program) with a write of FFH will safely abort the operation. Memory contents will not be altered. After the Reset command, the device returns to the read mode. The Reset command does not enable software data protection. See Figure 7 for timing waveforms.

Read

The Read operation is initiated by setting CE#, and OE# to logic low and setting WE# to logic high (See Table 2). See Figure 4 for read memory timing waveform. The read operation from the host retrieves data from the array. The device remains enabled for read until another operation mode is accessed. During initial power-up, the device is in the read mode and is software data protected. The device must be unprotected to execute a write command.

The read operation of the 28LF040 is controlled by OE# and CE# at logic low. When CE # is high, the chip is deselected and only standby power will be consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when CE# and OE# are high.

Read_ID operation

The Read_ID operation is initiated by writing a single command (90H). A read of address 0000H will output the manufacturer's code (BFH). A read of address 0001H will output the device code (04H). Any other valid command will terminate this operation.

Data Protection

In order to protect the integrity of nonvolatile data storage, the 28LF040 provides both hardware and software features to prevent inadvertent writes to the device, for example, during system power-up or power-down. Such provisions are described below.

Hardware Data Protection

The 28LF040 is designed with hardware features to prevent inadvertent writes. This is done in the following ways:

1. Write Inhibit Mode: OE# low, CE#, or WE# high will inhibit the write operation.
2. Noise/Glitch Protection: A WE# pulse width of less than 15 ns will not initiate a write cycle.
3. V_{CC} Power Up/Down Detection: The write operation is inhibited when V_{CC} is less than 2.5V.
4. After power-up the device is in the read mode and the device is in the software data protect state.

Software Data Protection (SDP)

The 28LF040 has software methods to further prevent inadvertent writes. In order to perform an erase or program operation, a two-step command sequence consisting of a set-up command followed by an execute command avoids inadvertent erasing and programming of the device.

The 28LF040 will default to software data protection after power up. A sequence of seven consecutive reads at specific addresses will unprotect the device The address sequence is 1823H, 1820H, 1822H, 0418H, 041BH, 0419H, 041AH. The address bus is latched on the rising edge of OE# or CE#, whichever occurs first. A similar seven read sequence of 1823H, 1820H, 1822H, 0418H, 041BH, 0419H, 040AH will protect the device. Also refer to Figures 10 and 11 for the 7 read cycle sequence Software Data Protection. The I/O pins can be in any state (i.e., high, low, or tristate).

Write Operation Status Detection

The 28LF040 provides three means to detect the completion of a write cycle, in order to optimize the system write cycle time. The end of a write cycle (erase or program) can be detected by three means: 1) monitoring the Data# Polling bit; 2) monitoring the Toggle bit; or 3) by two successive read of the same data. These three detection mechanisms are described below.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with the DQ used. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the write cycle, otherwise the rejection is valid.

Data# Polling (DQ_7)

The 28LF040 features Data# Polling to indicate the write operation status. During a write operation, any attempt to read the last byte loaded during the byte-load cycle will receive the complement of the true data on DQ_7. Once the write cycle is completed, DQ_7 will show true data. The

device is then ready for the next operation. See Figure 12 for Data Polling timing waveforms. In order for Data# Polling to function correctly , the byte being polled must be erased prior to programming.

Toggle Bit (DQ_6)

An alternative means for determining the write operation status is by monitoring the Toggle Bit, DQ_6. During a write operation, consecutive attempts to read data from the device will result in DQ_6 toggling between logic 0 (low) and logic 1 (high). When the write cycle is completed, the toggling will stop. The device is then ready for the next operation. See Figure 13 for Toggle Bit timing waveforms.

Successive Reads

An Alternative means for determining an end of a write cycle is by reading the same address for two consecutive data matches.

Product Identification

The Product Identification mode identifies the device as 28LF040 and the manufacturer as SST. This mode may be accessed by hardware and software operations. The hardware operation is typically used by an external programmer to identify the correct algorithm for the 28LF040. Users may wish to use the software operation to identify the device (i.e., using the device code). For details see Table 2 for the hardware operation and Figure 19 for the software operation. The manufacturer and device codes are the same for both operations.

Product Identification Table

	Byte	Data
Manufacturer Code	0000 H	BF H
Device Code	0001 H	04 H

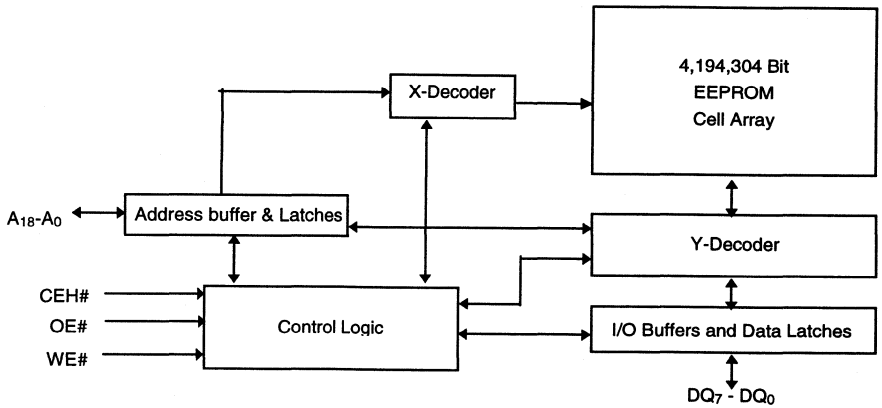


Figure 1: Functional Block Diagram of SST 28LF040

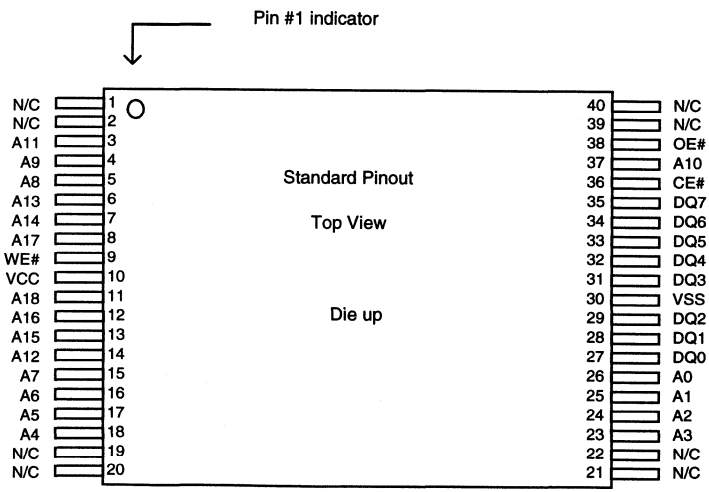


Figure 2A: Standard Pin Assignments for 40-pin TSOP Packages

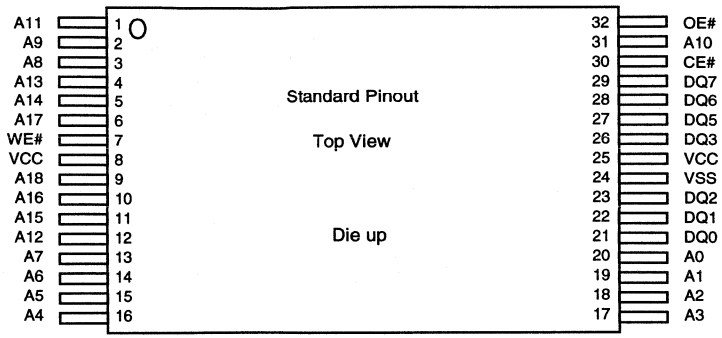


Figure 2B: Standard Pin Assignments for 32-pin TSOP Packages

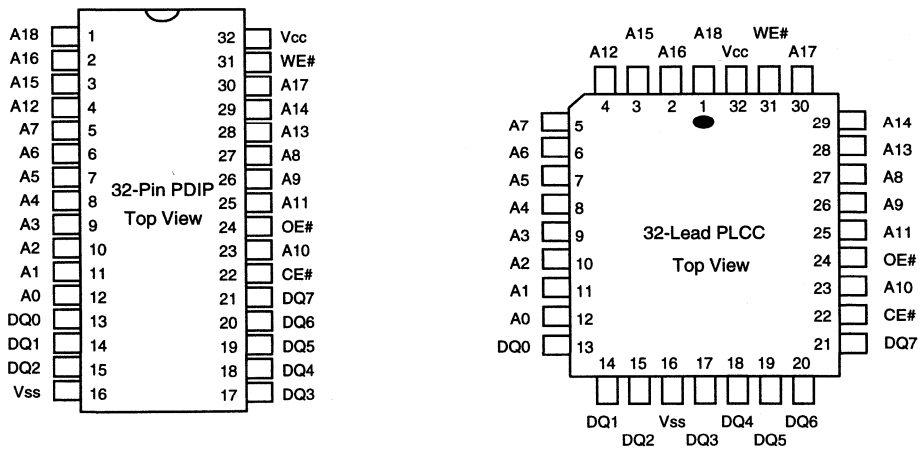


Figure 3: Pin Assignments for 32-pin Plastic DIPs and 32-pin PLCCs

Table 1: Pin Description

Symbol	Pin Name	Functions
A_{18}-A_8	Row Address Inputs	To provide memory addresses. Row addresses define a sector.
A_7-A_0	Column Address Inputs	Selects the byte within the sector.
DQ_7-DQ_0	Data Input/Output	To output data during read cycles and receive input data during write cycles. Data is internally latched during a write cycle. The outputs are in tri-state when OE#, CE # is high.
CE#	Chip Enable	To activate the device when CE # is low. (1)
OE#	Output Enable	To gate the data output buffers. (1)
WE#	Write Enable	To control the write operations. (1)
Vcc	Power Supply	To provide 3.3-volt supply (± 0.3 V)
Vss	Ground	

Note: (1)This pin is considered an input for the purposes of the DC Operation Characteristics Table.

Table 2: Operation Modes Selection

Mode	CE#	OE#	WE#	DQ	Address
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	A_{IN}
Byte Program	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}, See Table 3
Sector Erase	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}, See Table 3
Standby	V_{IH}	X	X	High Z	X
Write Inhibit	X	V_{IL}	X	High Z/ D_{OUT}	X
Write Inhibit	X	X	V_{IH}	High Z/ D_{OUT}	X
Software Chip Erase	V_{IL}	V_{IH}	V_{IL}	D_{IN}	See Table 3
Product Identification					
Hardware Mode	V_{IL}	V_{IL}	V_{IH}	Manufacturer Code (BF)	A_{18}-A_1=V_{IL}, A_9=V_H, A_0=V_{IL}
				Device Code (04)	A_{18}-A_1=V_{IL}, A_9=V_H, A_0=V_{IH}
Software Mode	V_{IL}	V_{IH}	V_{IL}		See Table 3
SDP Enable & Disable Mode	V_{IL}	V_{IH}	V_{IL}		See Table 3
Reset	V_{IL}	V_{IH}	V_{IL}		See Table 3

Table 3: Software Command Summary

Command Summary	Required Cycle(s)	Setup Command Cycle			Execute Command Cycle			SDP[5]
		Type[1]	Addr[2,3]	Data[4]	Type[1]	Addr[2,3]	Data[4]	
Sector_Erase	2	W	X	20H	W	SA	D0H	N
Byte_Program	2	W	X	10H	W	PA	PD	N
Chip_Erase	2	W	X	30H	W	X	30H	N
Reset	1	W	X	FFH				Y
Read_ID	3	W	X	90H	R	(8)	(8)	Y
Software_Data_Protect	7	R	(6)					
Software_Data_Unprotect	7	R	(7)					

Notes:

1. Type definition: W = Write, R = Read, X= don't care
2. Addr (Address) definition: SA = Sector Address = A_{18} - A_8, sector size = 256 bytes; A_7- A_0 = X for this command.
3. Addr (Address) definition: PA = Program Address = A_{18} - A_0.
4. Data definition: PD = Program Data, H = number in hex.
5. SDP = Software Data Protect mode using 7 Read Cycle Sequence.
   a) Y = the operation can be executed with protection enabled
   b) N = the operation cannot be executed with protection enabled
6. Refer to Figure 11 for the 7 Read Cycle sequence for Software_Data_Protect.
7. Refer to Figure 10 for the 7 Read Cycle sequence for Software_Data_Unprotect.
8. Address 0000H retrieves the manufacturer' code of BFH and address 0001H retrieves the device code of 04H.

Table 4: Memory Array Detail

Sector Select	Byte Select
A_{18} - A_8	A_7 - A_0

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential ..... -0.5V to V_{CC}+ 0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential ..... -1.0V to V_{CC}+ 1.0V
Voltage on A_9 Pin to Ground Potential ..... -0.5V to 14.0V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Through Soldering Temperature (10 Seconds)..... 300°C
Surface Mount Lead Soldering Temperature (3 Seconds) ..... 240°C
Output Short Circuit Current[1] ..... 100 mA

Note: [1] Outputs shorted for no more than one second. No more than one output shorted at a time.

Table 5: Operating Range

Range	Ambient Temp	V_{CC}
Commercial	0 °C to +70 °C	3.0V to 3.6V
Industrial	-40 °C to +85 °C	3.0V to 3.6V

Table 6: AC Conditions of Test

Input Rise/Fall Time.....10 ns
Output Load.....1 TTL Gate and C_L = 100 pF
See Figures 14 and 15

Table 7: DC Operating Characteristics

Symbol	Parameter	Limits		Units	Test Conditions
		Min	Max		
I_{CC}	Power Supply Current				CE# = OE# =V_{IL}, WE# =V_{IH}, all I/Os open
	Read		10	mA	Address input = V_{IL}/V_{IH}, at f=1/T_{RC} Min. V_{CC} = V_{CC} Max
	Program and Erase		25	mA	CE# =WE# =V_{IL}, OE# =V_{IH} V_{CC} =V_{CC} Max.
I_{SB1}	Standby V_{CC} Current (TTL input)		1	mA	CE# =OE# =WE# = V_{IH}, V_{CC}=V_{CC} Max
I_{SB2}	Standby V_{CC} Current (CMOS input)		20	µA	CE# = OE# = WE# = V_{CC} -0.3V, V_{CC}=V_{CC} Max
I_{LI}	Input Leakage Current		1	µA	V_{IN} = GND to V_{CC}, V_{CC} = V_{CC} Max.
I_{LO}	Output Leakage Current		10	µA	V_{OUT} =GND to V_{CC}, V_{CC} = V_{CC} Max.
V_{IL}	Input Low Voltage		0.8	V	V_{CC} = V_{CC} Max.
V_{IH}	Input High Voltage	2.0		V	V_{CC} = V_{CC} Max.
V_{OL}	Output Low Voltage		0.4	V	I_{OL}= 100 µA, V_{CC} = V_{CC} Min.
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -100 µA, V_{CC} = V_{CC} Min.
V_H	Supervoltage for A_9	11.6	12.4	V	CE#=OE#=V_{IL},WE#=V_{IH}
I_H	Supervoltage Current for A_9		200	µA	CE#=OE#=V_{IL},WE#=V_{IH}, A_9 = V_H Max.

Table 8: Power-up Timings

Symbol	Parameter	Maximum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	10	ms
$T_{PU-WRITE}$[1]	Power-up to Write Operation	10	ms

Table 9: Capacitance (Ta = 25 °C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0v	6 pF

Note: [1]This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 10: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}	Endurance	1,000 & 10,000[2]	Cycles	MIL-STD-883, Method 1033
T_{DR}[1]	Data Retention	100	Years	MIL-STD-883, Method 1008
V_{ZAP_HBM}[1]	ESD Susceptibility Human Body Model	1000	Volts	MIL-STD-883, Method 3015
V_{ZAP_MM}[1]	ESD Susceptibility Machine Model	200	Volts	JEDEC
I_{LTH}[1]	Latch Up	100	mA	JEDEC Standard 17

Note: [1]This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

[2]See Ordering Information for desired type.

AC Characteristics

Table 11: Read Cycle Timing Parameters

IEEE Symbol	Industry Symbol	Parameter	28LF040-200		28LF040-250		Units
			Min	Max	Min	Max	
tAVAV	T_{RC}	Read Cycle time	200		250		ns
tAVQV	T_{AA}	Address Access Time		200		250	ns
tELQV	T_{CE}	Chip Enable Access Time		200		250	ns
tGLQV	T_{OE}	Output Enable Access Time		120		120	ns
tEHQZ	T_{CLZ}[1]	CE# Low to Active Output	0		0		ns
tGHQZ	T_{OLZ}[1]	OE# Low to Active Output	0		0		ns
tELQX	T_{CHZ}[1]	CE# High to High-Z Output		60		60	ns
tGLQX	T_{OHZ}[1]	OE# High to High-Z Output		60		60	ns
tAXQX	T_{OH}[1]	Output Hold from Address Change	0		0		ns

Table 12: Erase/Program Cycle Timing Parameters

IEEE Symbol	Industry Symbol	Parameter	28LF040-200		28LF040-250		Units
			Min	Max	Min	Max	
tAVA	T_{BP}	Byte Program Cycle Time		35		35	µs
tWLWH	T_{WP}	Write Pulse Width (WE#)	160		200		ns
tAVWL	T_{AS}	Address Setup Time	10		10		ns
tWLAX	T_{AH}	Address Hold Time	100		100		ns
tELWL	T_{CS}	CE# Setup Time	0		0		ns
tWHEX	T_{CH}	CE# Hold Time	0		0		ns
tGHWL	T_{OES}	OE# High Setup Time	20		20		ns
tWGL	T_{OEH}	OE# High Hold Time	20		20		ns
tWLEH	T_{CP}	Write Pulse Width (CE#)	160		200		ns
tDVWH	T_{DS}	Data Setup Time	100		100		ns
tWHDX	T_{DH}	Data Hold Time	20		20		ns
tWHWL2	T_{SE}	Sector Erase Cycle Time		4		4	ms
	T_{RST}[1]	Reset Command Recovery Time		4		4	µs
tWHWL3	T_{SCE}	Software Chip_Erase Cycle Time		20		20	ms
tEHEL	T_{CPH}	CE# High Pulse Width	50		50		ns
tWHWL1	T_{WPH}	WE# High Pulse Width	50		50		ns
	T_{PCP}[1]	Protect Chip Enable Pulse Width	20		20		ns
	T_{PCH}[1]	Protect Chip Enable High Time	20		20		ns
	T_{PAS}[1]	Protect Address Setup Time	0		0		ns
	T_{PAH}[1]	Protect Address Hold Time	100		100		ns

Note: [1]This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.

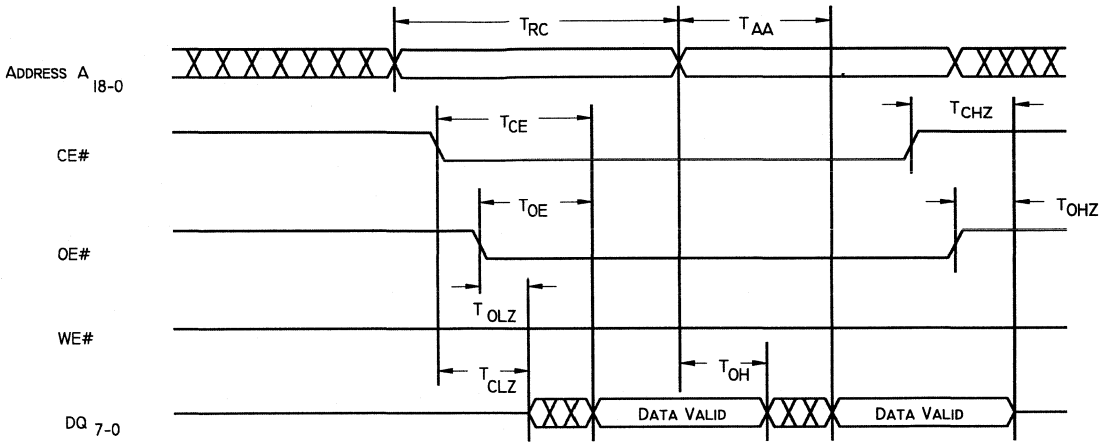


Figure 4: Read Cycle Timing Diagram

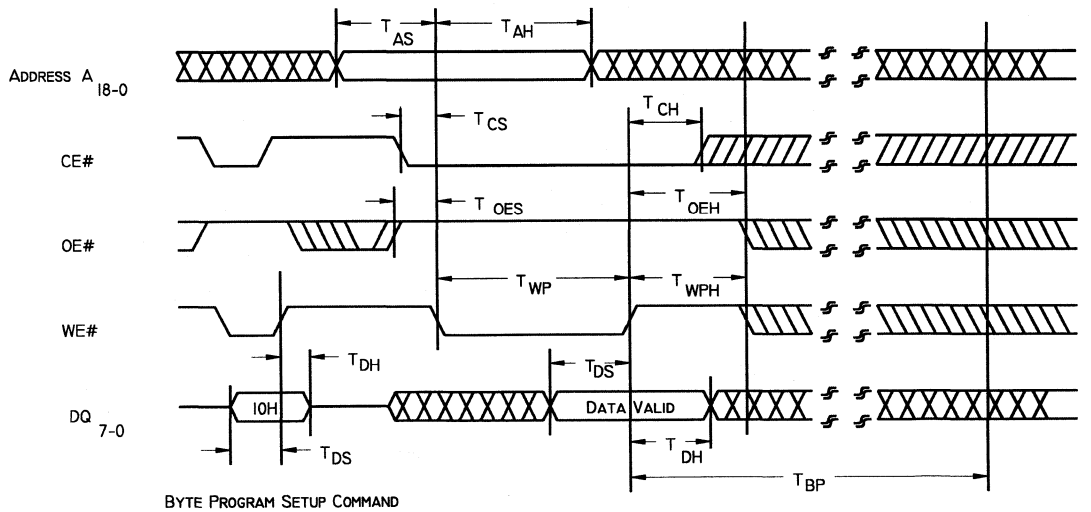


Figure 5: WE# Controlled Byte Program Timing Diagram

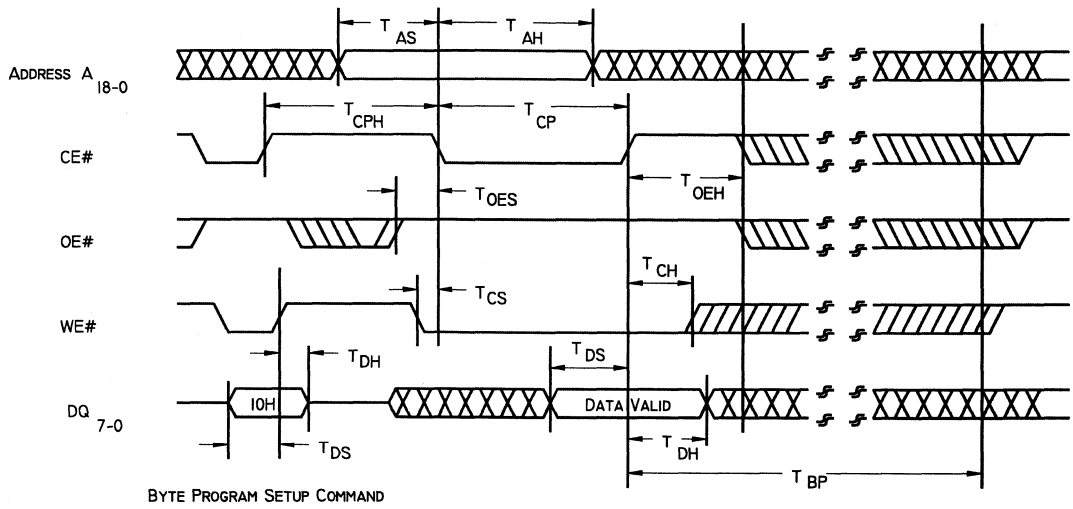


Figure 6: CE# Controlled Byte Program Timing Diagram

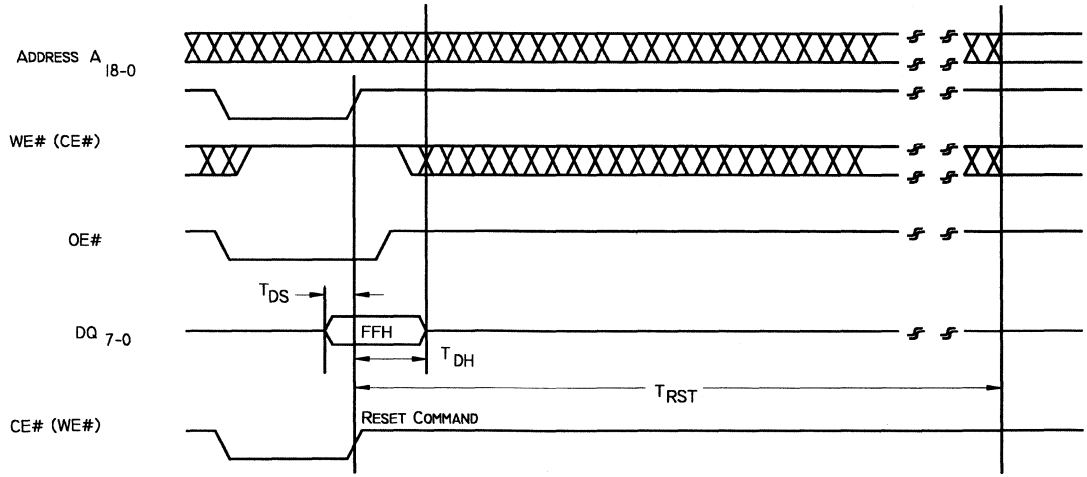


Figure 7: Reset Command Timing Diagram

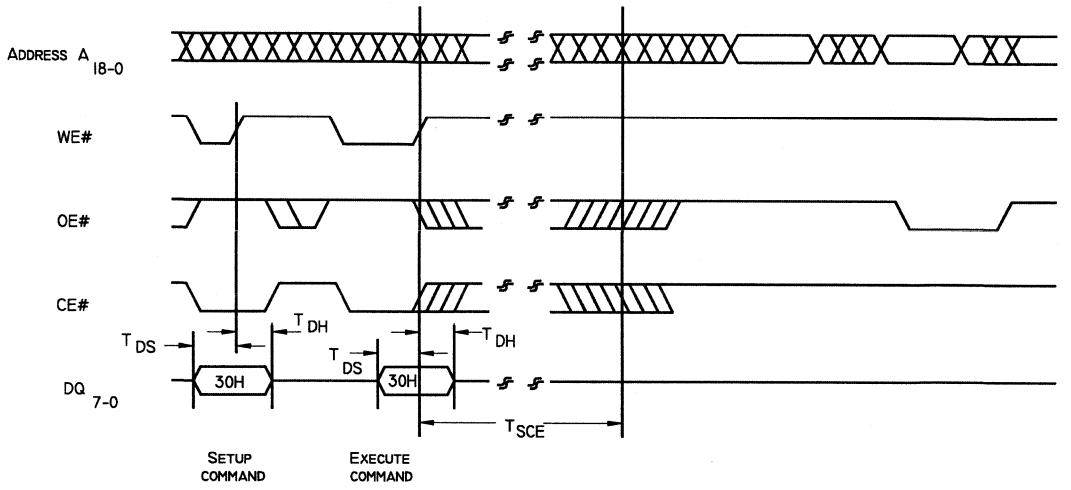


Figure 8: Chip_Erase Timing Diagram

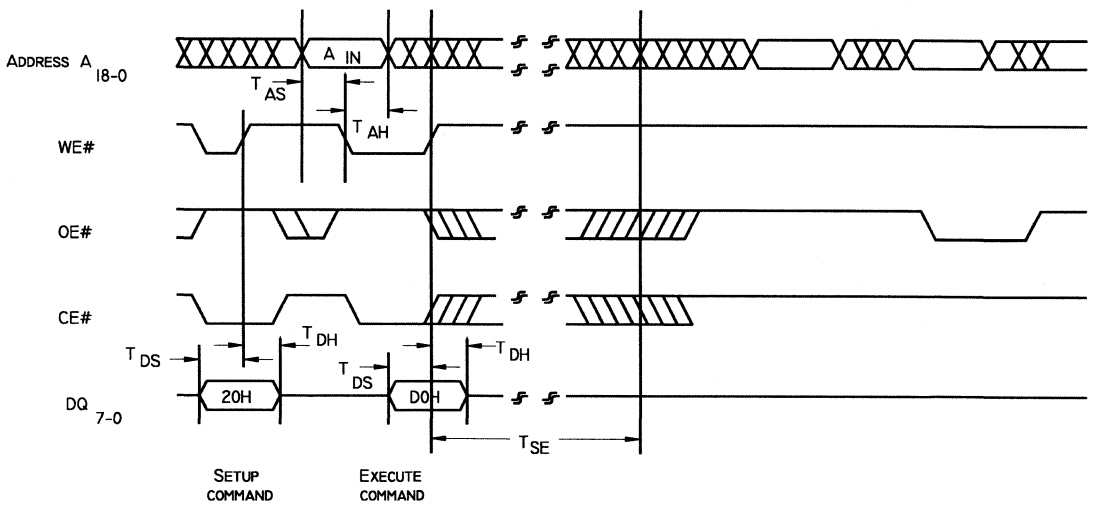
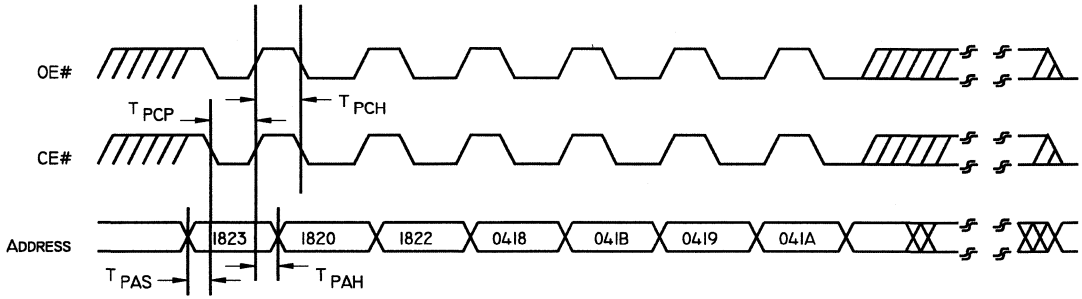


Figure 9: Sector Erase Timing Diagram



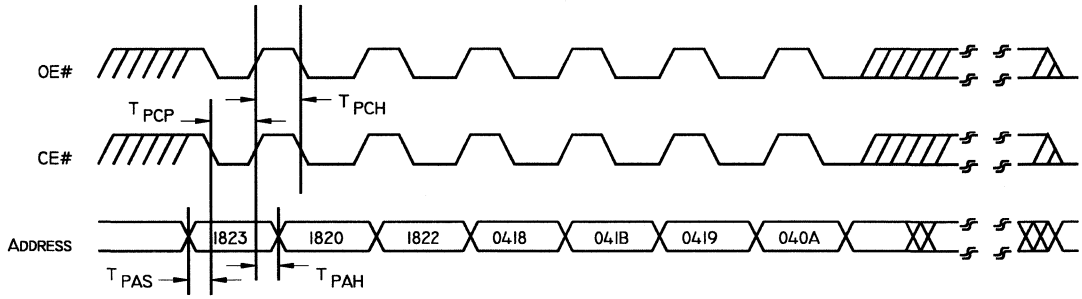
NOTE : A. ADDRESSES ARE LATCHED INTERNALLY ON THE RISING EDGE OF:

1. OE# IF CE# IS KEPT AT LOW ALL TIME.
2. CE# IF OE# IS KEPT AT LOW ALL TIME.
3. THE FIRST PIN TO GO HIGH IF BOTH ARE TOGGLED.

B. ABOVE ADDRESS VALUES ARE IN HEX.

C. ADDRESSES > A_{12} ARE "DON'T CARE"

Figure 10: Software Data Unprotect Timing Diagram



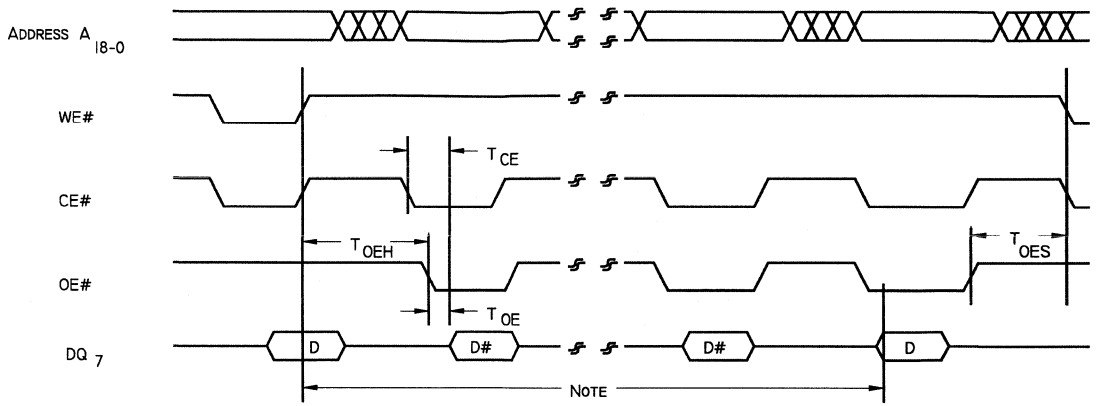
NOTE : A. ADDRESSES ARE LATCHED INTERNALLY ON THE RISING EDGE OF:

1. OE# IF CE# IS KEPT AT LOW ALL TIME.
2. CE# IF OE# IS KEPT AT LOW ALL TIME.
3. THE FIRST PIN TO GO HIGH IF BOTH ARE TOGGLED.

B. ABOVE ADDRESS VALUES ARE IN HEX.

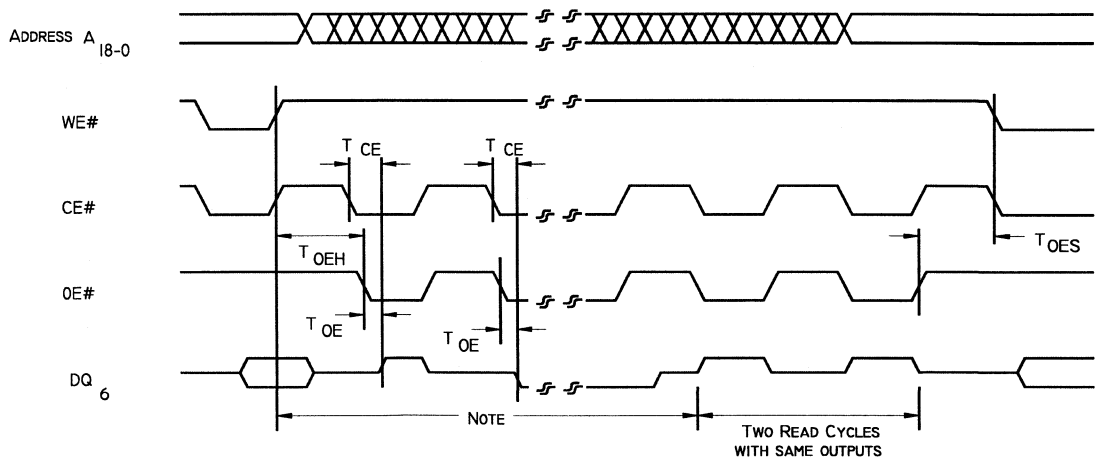
C. ADDRESSES > A_{12} ARE "DON'T CARE"

Figure 11: Software Data Protect Timing Diagram



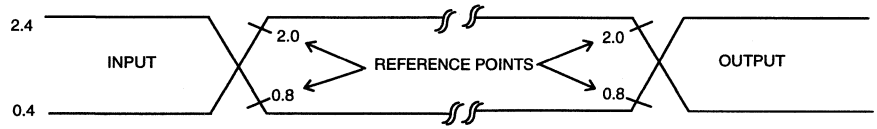
NOTE: THIS TIME INTERVAL SIGNAL CAN BE T_{SE} OR T_{BP} DEPENDING UPON THE SELECTED OPERATION MODE.

Figure 12: Data# Polling Timing Diagram



NOTE: THIS TIME INTERVAL SIGNAL CAN BE T_{SE} OR T_{BP} , DEPENDING UPON THE SELECTED OPERATION MODE.

Figure 13: Toggle Bit Timing Diagram



AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a logic "1" and V_{OL} (0.4 V_{TTL}) for a logic "0". Measurement reference points for inputs and outputs are V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Inputs rise and fall times (10% ↔ 90%) are <10 ns.

Figure 14: AC Input/Output Reference Waveform

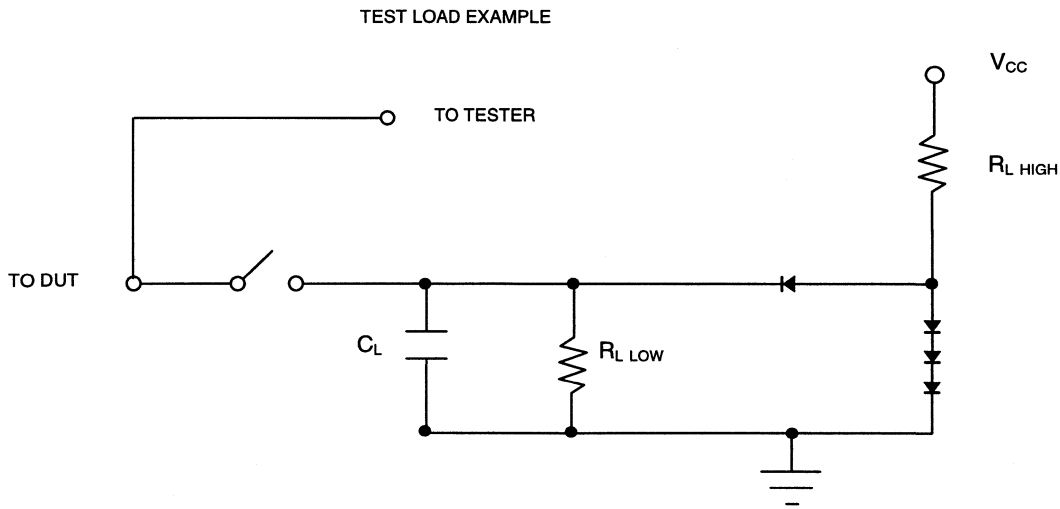


Figure 15: Test Load Example

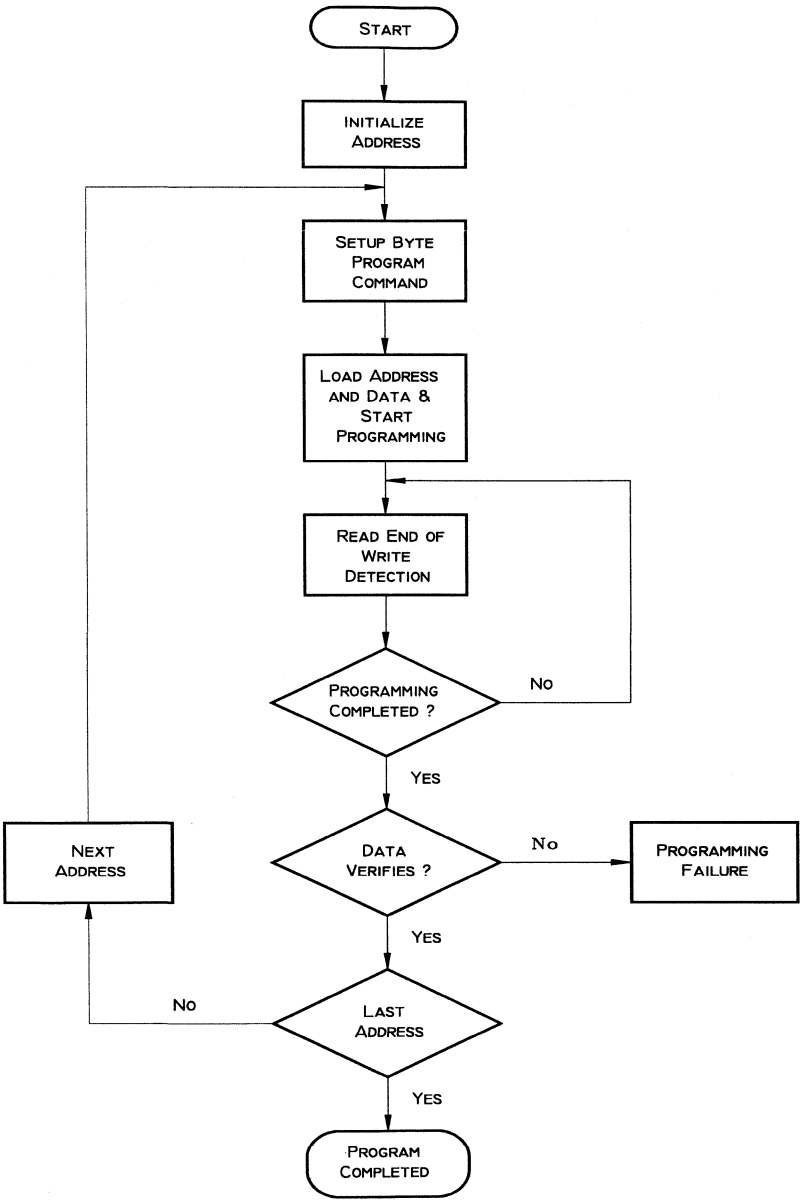


Figure 16: Byte Program Flowchart

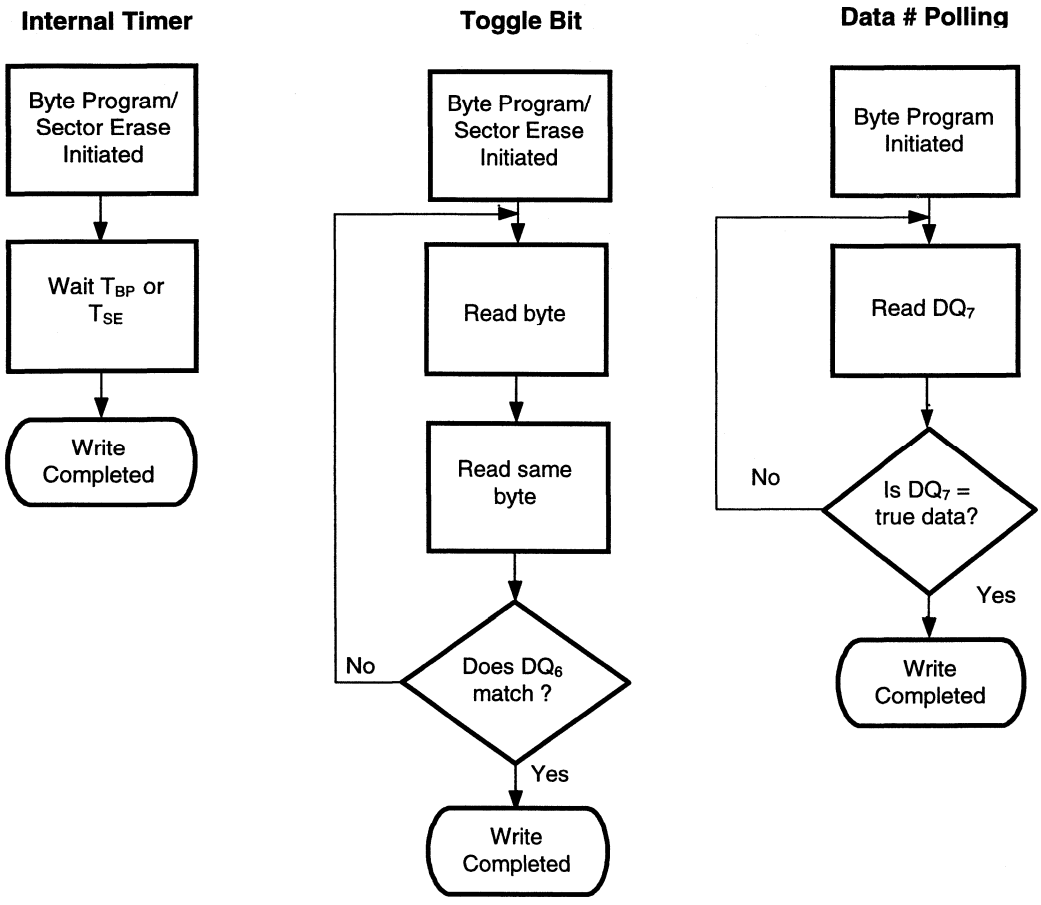


Figure 17: Write Wait Options

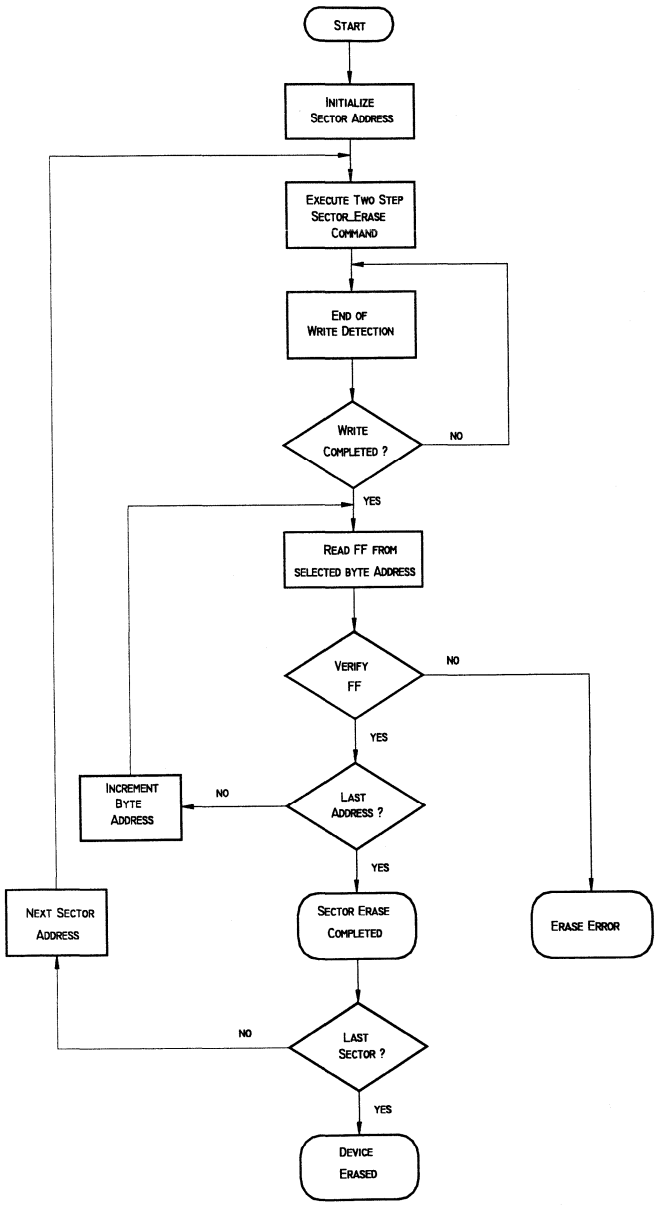


Figure 18: Sector_Erase Flowchart

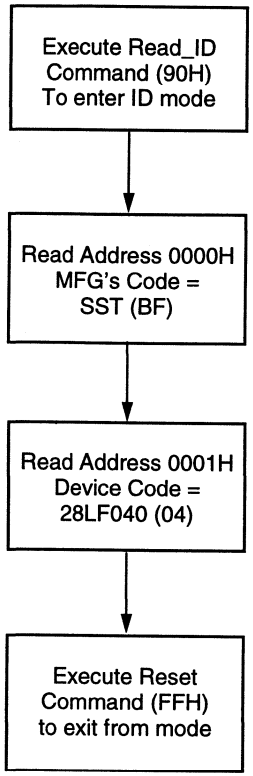
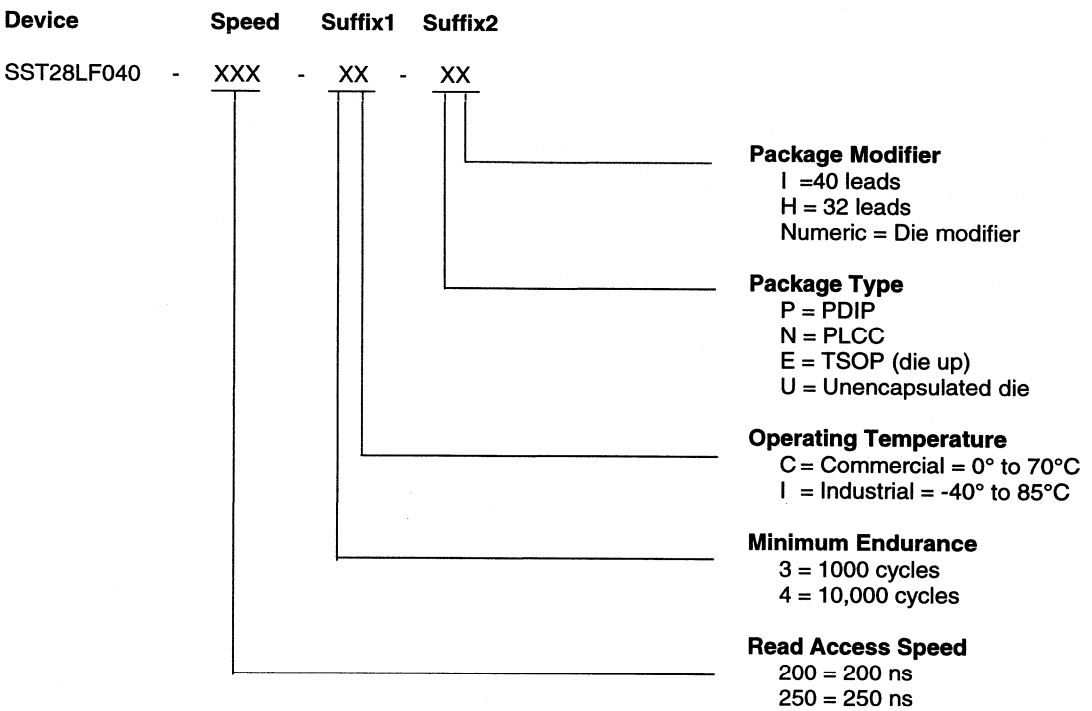


Figure 19: Software Product ID Flow

Product Ordering Information



Valid combinations

SST28LF040-200-4C- EH	SST28LF040-200-4C- EI	SST28LF040-200-4C- NH
SST28LF040-200-4C- PH		
SST28LF040-250-4C- EH	SST28LF040-250-4C- EI	SST28LF040-250-4C- NH
SST28LF040-250-4C- PH	SST28LF040-250-4C- U1	
SST28LF040-200-3C- EH	SST28LF040-200-3C- EI	SST28LF040-200-3C- NH
SST28LF040-200-3C- PH		
SST28LF040-250-3C- EH	SST28LF040-250-3C- EI	SST28LF040-250-3C- NH
SST28LF040-250-3C- PH	SST28LF040-250-3C- U1	
SST28LF040-200-4I- EH	SST28LF040-200-4I- EI	SST28LF040-200-4I- NH
SST28LF040-250-4I- EH	SST28LF040-250-4I- EI	SST28LF040-250-4I- NH
SST28LF040-200-3I- EH	SST28LF040-200-3I- EI	SST28LF040-200-3I- NH
SST28LF040-250-3I- EH	SST28LF040-250-3I- EI	SST28LF040-250-3I- NH

Example: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Preliminary Specifications

SST 28VF040
2.7V-only 4 Megabit SuperFlash EEPROM

July 1996

SST 28VF040
2.7V-only 4 Megabit SuperFlash EEPROM

Preliminary Specifications

Features:

Single 2.7-Volt Read and Write Operations
CMOS SuperFlash EEPROM Technology
Endurance: 100,000 Cycles (typical)
Greater than 100 years Data Retention
Memory Organization: 512K x 8
Sector Erase Capability: 256 bytes per Sector
Low Power Consumption:
Active Current: 10 mA (typical)
Standby Current: 5 µA (typical)
Fast Sector Erase/Byte Program Operation
Byte Program Time: 30 µs (typical)
Sector Erase Time: 2 ms (typical)
Complete Memory Rewrite: 20 sec (typical)
Fast Access Time: 250 and 300 ns
Latched Address and Data
Hardware and Software Data Protection
7-Read-Cycle-Sequence Software Data Protection
End of Write Detection
Toggle Bit
Data# Polling
TTL I/O Compatibility
Packages Available
40-Pin TSOP (10 mm x 20 mm)
32-Pin TSOP (8 mm x 20 mm)
32-Pin PLCC
32-Pin PDIP

Product Description

The 28VF040 is organized as a 512K x 8 (bits) CMOS sector erase, byte program EEPROM. The 28VF040 is manufactured using SST's proprietary, high performance CMOS SuperFlash EEPROM Technology. The split gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternative approaches. The 28VF040 erases and programs with a 2.7 volt only power supply. (V_{CC}: 2.7V to 3.6V) The 28VF040 conforms to JEDEC standard pinouts for byte wide memories and is compatible with existing industry standard EPROM, flash EPROM and EEPROM pinouts.

Featuring high performance programming, the 28VF040 typically byte programs in 30 µs. The 28VF040 typically sector erases in 2 ms. Both program and erase times can be optimized using interface features such as Toggle bit or Data# Polling to indicate the completion of the write cycle. To protect against an inadvertent write, the 28VF040 has on chip hardware and software data protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, the 28VF040 is offered with a guaranteed sector endurance of 10^4 and 10^3 cycles. Data retention is rated greater than 100 years.

The 28VF040 is best suited for applications that require reprogrammable nonvolatile mass storage of program, configuration, or data memory. For all system applications, the 28VF040 significantly improves performance and reliability, while lowering power consumption when compared with floppy diskettes or EPROM approaches. EEPROM technology makes possible convenient and economical updating of codes and control programs on-line. The 28VF040 improves flexibility, while lowering the cost of program and configuration storage application.

Figure 1 shows the functional blocks of the 28VF040. Figures 2A, 2B, and 3 show the pin assignments for the 40 pin TSOP, 32 pin TSOP, 32 pin PDIP, and 32 pin PLCC packages. Pin description and operation modes are described in Tables 1 through 4.

Device Operation

Commands are used to initiate the memory operation functions of the device. Commands are written to the device using standard microprocessor write sequences. A command is written by asserting WE# low while keeping CE# low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first. Note, during the software data protection sequence the address are latched on the rising edge of OE# or CE#, whichever occurs first.

Command Definitions

Table 3 contains a command list and a brief summary of the commands. The following is a detailed description of the operations initiated by each command.

Sector_Erase Operation

The Sector_Erase operation erases all bytes within a sector and is initiated by a setup command and an execute command. A sector contains 256 bytes. This sector erasability enhances the flexibility and usefulness of the 28VF040, since most applications only need to change a small number of bytes or sectors, not the entire chip.

The setup command is performed by writing 20H to the device. The execute command is performed by writing D0H to the device. The erase operation begins with the rising edge of the WE# or CE#, whichever occurs first and terminates automatically by using an internal timer. The end of Erase can be determined using either Data# Polling, Toggle Bit, or Successive Reads detection methods. See Figure 9 for timing waveforms.

The two-step sequence of setup command followed by an execute command ensures that only memory contents within the addressed sector are erased and other sectors are not inadvertently erased.

Sector_Erase Flowchart Description

Fast and reliable erasing of the memory contents within a sector is accomplished by following the sector erase flowchart as shown in Figure 18. The entire procedure consists of the execution of two commands. The Sector_Erase operation will terminate after a maximum of 4 ms. A Reset command can be executed to terminate the erase operation; however, if the erase operation is terminated prior to the 4 ms time-out, the sector may not be fully erased. An erase command can be reissued as many times as necessary to complete the erase operation. The 28VF040 cannot be "overerased".

Chip_Erase Operation

The Chip_Erase operation is initiated by a setup command (30H) and an execute command (30H). The Chip_Erase operation allows the entire array of the 28VF040 to erase in one operation, as opposed to 2048 sector erase operations. Using the Chip_Erase operation will minimize the time to rewrite the entire memory array. The Chip_Erase operation will terminate after a maximum of 20 ms. A Reset command can be executed to terminate the erase operation; however, if the erase operation is terminated prior to the 20 ms time-out, the Chip may not be completely erased. If an erase error occurs an erase command can be reissued as many times as necessary to complete the erase operation. The 28VF040 cannot be "overerased". (See Figure 8)

Byte_Program Operation

The Byte_Program operation is initiated by writing the setup command (10H). Once the program setup is performed, programming is executed by the next WE# pulse. See Figures 5 and 6 for timing waveforms. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first, and begins the program operation. The program operation is terminated automatically by an internal timer. See Figure 16 for the programming flowchart.

The two-step sequence of a setup command followed by an execute command ensures that only the addressed byte is programmed and other bytes are not inadvertently programmed.

The Byte_Program Flowchart Description

Programming data into the 28VF040 is accomplished by following the Byte_Program flowchart shown in Figure 16. The Byte_Program command sets up the byte for programming. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first and begins the program operation. The end of program can be detected using either the Data# Polling, Toggle bit, or Successive reads.

Reset Operation

The Reset command is provided as a means to safely abort the erase or program command sequences. Following either setup commands (erase or program) with a write of FFH will safely abort the operation. Memory contents will not be altered. After the Reset command, the device returns to the read mode. The Reset command does not enable software data protection. See Figure 7 for timing waveforms.

Read

The Read operation is initiated by setting CE#, and OE# to logic low and setting WE# to logic high (See Table 2). See Figure 4 for read memory timing waveform. The read operation from the host retrieves data from the array. The device remains enabled for read until another operation mode is accessed. During initial power-up, the device is in the read mode and is software data protected. The device must be unprotected to execute a write command.

The read operation of the 28VF040 is controlled by OE# and CE# at logic low. When CE # is high, the chip is deselected and only standby power will be consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when CE# and OE# are high.

Read_ID operation

The Read_ID operation is initiated by writing a single command (90H). A read of address 0000H will output the manufacturer's code (BFH). A read of address 0001H will output the device code (04H). Any other valid command will terminate this operation.

Data Protection

In order to protect the integrity of nonvolatile data storage, the 28VF040 provides both hardware and software features to prevent inadvertent writes to the device, for example, during system power-up or power-down. Such provisions are described below.

Hardware Data Protection

The 28VF040 is designed with hardware features to prevent inadvertent writes. This is done in the following ways:

1. Write Inhibit Mode: OE# low, CE#, or WE# high will inhibit the write operation.
2. Noise/Glitch Protection: A WE# pulse width of less than 15 ns will not initiate a write cycle.
3. V_{CC} Power Up/Down Detection: The write operation is inhibited when V_{CC} is less than 2.5V.
4. After power-up the device is in the read mode and the device is in the software data protect state.

Software Data Protection (SDP)

The 28VF040 has software methods to further prevent inadvertent writes. In order to perform an erase or program operation, a two-step command sequence consisting of a set-up command followed by an execute command avoids inadvertent erasing and programming of the device.

The 28VF040 will default to software data protection after power up. A sequence of seven consecutive reads at specific addresses will unprotect the device The address sequence is 1823H, 1820H, 1822H, 0418H, 041BH, 0419H, 041AH. The address bus is latched on the rising edge of OE# or CE#, whichever occurs first. A similar seven read sequence of 1823H, 1820H, 1822H, 0418H, 041BH, 0419H, 040AH will protect the device. Also refer to Figures 10 and 11 for the 7 read cycle sequence Software Data Protection. The I/O pins can be in any state (i.e., high, low, or tristate).

Write Operation Status Detection

The 28VF040 provides three means to detect the completion of a write cycle, in order to optimize the system write cycle time. The end of a write cycle (erase or program) can be detected by three means: 1) monitoring the Data# Polling bit; 2) monitoring the Toggle bit; or 3) by two successive read of the same data. These three detection mechanisms are described below.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with the DQ used. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the write cycle, otherwise the rejection is valid.

Data# Polling (DQ_7)

The 28VF040 features Data# Polling to indicate the write operation status. During a write operation, any attempt to read the last byte loaded during the byte-load cycle will receive the complement of the true data on DQ_7. Once the write cycle is completed, DQ_7 will show true data. The

device is then ready for the next operation. See Figure 12 for Data Polling timing waveforms. In order for Data# Polling to function correctly , the byte being polled must be erased prior to programming.

Toggle Bit (DQ_6)

An alternative means for determining the write operation status is by monitoring the Toggle Bit, DQ_6. During a write operation, consecutive attempts to read data from the device will result in DQ_6 toggling between logic 0 (low) and logic 1 (high). When the write cycle is completed, the toggling will stop. The device is then ready for the next operation. See Figure 13 for Toggle Bit timing waveforms.

Successive Reads

An Alternative means for determining an end of a write cycle is by reading the same address for two consecutive data matches.

Product Identification

The Product Identification mode identifies the device as 28VF040 and the manufacturer as SST. This mode may be accessed by hardware and software operations. The hardware operation is typically used by an external programmer to identify the correct algorithm for the 28VF040. Users may wish to use the software operation to identify the device (i.e., using the device code). For details see Table 2 for the hardware operation and Figure 19 for the software operation. The manufacturer and device codes are the same for both operations.

Product Identification Table

	Byte	Data
Manufacturer Code	0000 H	BF H
Device Code	0001 H	04 H

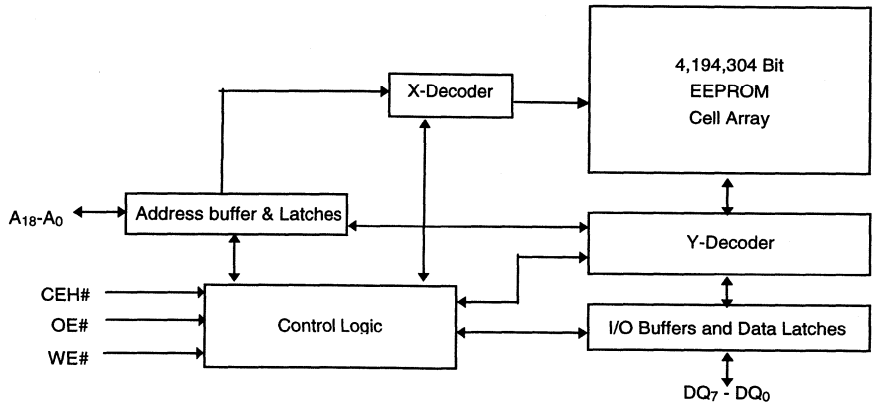


Figure 1: Functional Block Diagram of SST 28VF040

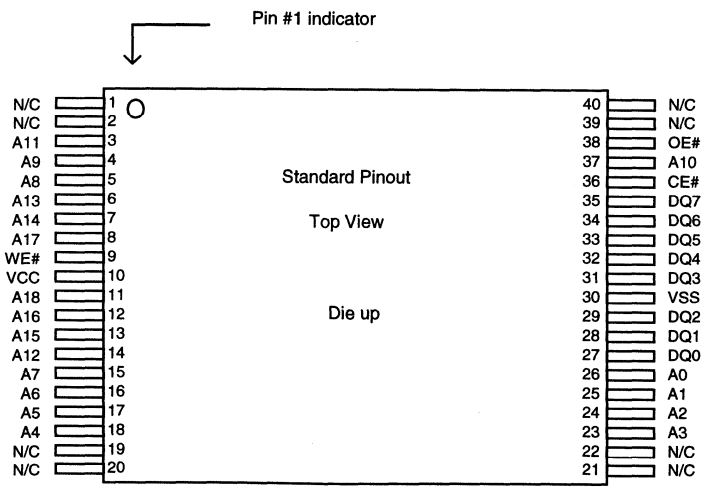


Figure 2A: Standard Pin Assignments for 40-pin TSOP Packages

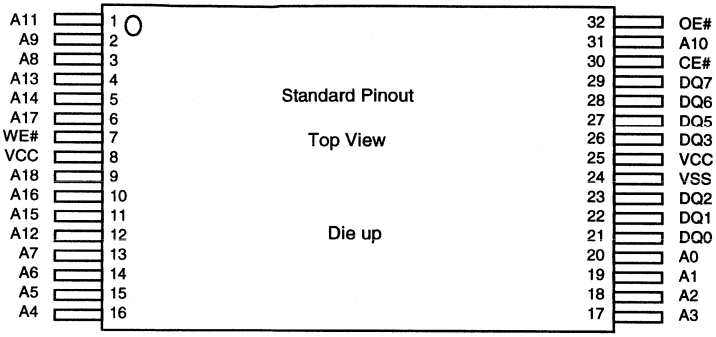


Figure 2B: Standard Pin Assignments for 32-pin TSOP Packages

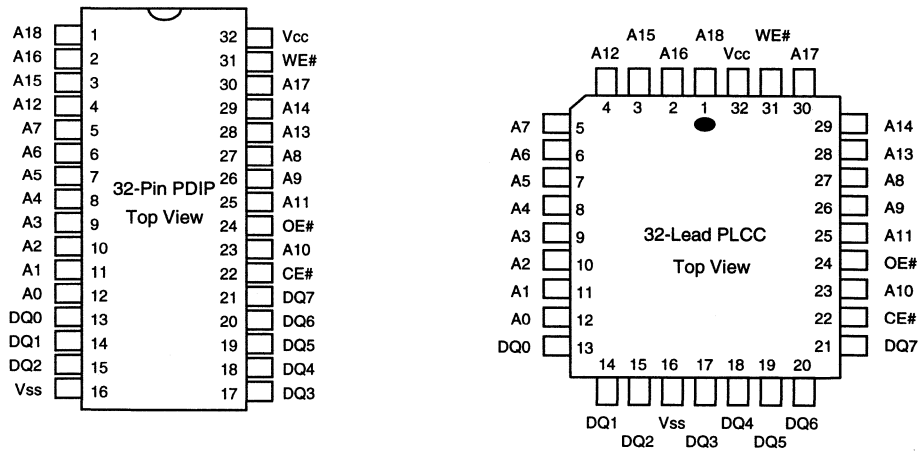


Figure 3: Pin Assignments for 32-pin Plastic DIPs and 32-pin PLCCs

Table 1: Pin Description

Symbol	Pin Name	Functions
A_{18}-A_8	Row Address Inputs	To provide memory addresses. Row addresses define a sector.
A_7-A_0	Column Address Inputs	Selects the byte within the sector.
DQ_7-DQ_0	Data Input/Output	To output data during read cycles and receive input data during write cycles. Data is internally latched during a write cycle. The outputs are in tri-state when OE#, CE # is high.
CE#	Chip Enable	To activate the device when CE # is low. (1)
OE#	Output Enable	To gate the data output buffers. (1)
WE#	Write Enable	To control the write operations. (1)
Vcc	Power Supply	To provide 3.0-volt supply (± 0.3 V)
Vss	Ground	

Note: (1)This pin is considered an input for the purposes of the DC Operation Characteristics Table.

Table 2: Operation Modes Selection

Mode	CE#	OE#	WE#	DQ	Address
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	A_{IN}
Byte Program	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}, See Table 3
Sector Erase	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}, See Table 3
Standby	V_{IH}	X	X	High Z	X
Write Inhibit	X	V_{IL}	X	High Z/ D_{OUT}	X
Write Inhibit	X	X	V_{IH}	High Z/ D_{OUT}	X
Software Chip Erase	V_{IL}	V_{IH}	V_{IL}	D_{IN}	See Table 3
Product Identification					
Hardware Mode	V_{IL}	V_{IL}	V_{IH}	Manufacturer Code (BF)	A_{18}-A_1=V_{IL}, A_9=V_H, A_0=V_{IL}
				Device Code (04)	A_{18}-A_1=V_{IL}, A_9=V_H, A_0=V_{IH}
Software Mode	V_{IL}	V_{IH}	V_{IL}		See Table 3
SDP Enable & Disable Mode	V_{IL}	V_{IH}	V_{IL}		See Table 3
Reset	V_{IL}	V_{IH}	V_{IL}		See Table 3

Table 3: Software Command Summary

Command Summary	Required Cycle(s)	Setup Command Cycle			Execute Command Cycle			SDP[5]
		Type[1]	Addr[2,3]	Data[4]	Type[1]	Addr[2,3]	Data[4]	
Sector_Erase	2	W	X	20H	W	SA	D0H	N
Byte_Program	2	W	X	10H	W	PA	PD	N
Chip_Erase	2	W	X	30H	W	X	30H	N
Reset	1	W	X	FFH				Y
Read_ID	3	W	X	90H	R	(8)	(8)	Y
Software_Data_Protect	7	R	(6)					
Software_Data_Unprotect	7	R	(7)					

Notes:

1. Type definition: W = Write, R = Read, X= don't care
2. Addr (Address) definition: SA = Sector Address = A_{18} - A_8, sector size = 256 bytes; A_7- A_0 = X for this command.
3. Addr (Address) definition: PA = Program Address = A_{18} - A_0.
4. Data definition: PD = Program Data, H = number in hex.
5. SDP = Software Data Protect mode using 7 Read Cycle Sequence.
   a) Y = the operation can be executed with protection enabled
   b) N = the operation cannot be executed with protection enabled
6. Refer to Figure 11 for the 7 Read Cycle sequence for Software_Data_Protect.
7. Refer to Figure 10 for the 7 Read Cycle sequence for Software_Data_Unprotect.
8. Address 0000H retrieves the manufacturer' code of BFH and address 0001H retrieves the device code of 04H.

Table 4: Memory Array Detail

Sector Select	Byte Select
A_{18} - A_8	A_7 - A_0

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential ..... -0.5V to V_{CC}+ 0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential ..... -1.0V to V_{CC}+ 1.0V
Voltage on A_9 Pin to Ground Potential ..... -0.5V to 14.0V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Through Soldering Temperature (10 Seconds)..... 300°C
Surface Mount Lead Soldering Temperature (3 Seconds) ..... 240°C
Output Short Circuit Current[1] ..... 100 mA

Note: [1] Outputs shorted for no more than one second. No more than one output shorted at a time.

Table 5: Operating Range

Range	Ambient Temp	V_{CC}
Commercial	0 °C to +70 °C	2.7 to 3.6V
Industrial	-40 °C to +85 °C	2.7 to 3.6V

Table 6: AC Conditions of Test

Input Rise/Fall Time.....10 ns
Output Load.....1 TTL Gate and C_L = 100 pF
See Figures 14 and 15

Table 7: DC Operating Characteristics

Symbol	Parameter	Limits		Units	Test Conditions
		Min	Max		
I_{CC}	Power Supply Current				CE# = OE# =V_{IL}, WE# =V_{IH}, all I/Os open
	Read		10	mA	Address input = V_{IL}/V_{IH}, at f=1/T_{RC} Min. V_{CC} = V_{CC} Max
	Program and Erase		25	mA	CE# =WE# =V_{IL}, OE# =V_{IH} V_{CC} =V_{CC} Max.
I_{SB1}	Standby V_{CC} Current (TTL input)		1	mA	CE# =OE# =WE# = V_{IH}, V_{CC}=V_{CC} Max
I_{SB2}	Standby V_{CC} Current (CMOS input)		20	µA	CE# = OE# = WE# = V_{CC} -0.3V, V_{CC}=V_{CC} Max
I_{LI}	Input Leakage Current		1	µA	V_{IN} = GND to V_{CC}, V_{CC} = V_{CC} Max.
I_{LO}	Output Leakage Current		10	µA	V_{OUT} =GND to V_{CC}, V_{CC} = V_{CC} Max.
V_{IL}	Input Low Voltage		0.8	V	V_{CC} = V_{CC} Max.
V_{IH}	Input High Voltage	2.0		V	V_{CC} = V_{CC} Max.
V_{OL}	Output Low Voltage		0.4	V	I_{OL}= 100 µA, V_{CC} = V_{CC} Min.
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -100 µA, V_{CC} = V_{CC} Min.
V_H	Supervoltage for A_9	11.6	12.4	V	CE#=OE#=V_{IL},WE#=V_{IH}
I_H	Supervoltage Current for A_9		200	µA	CE#=OE#=V_{IL},WE#=V_{IH}, A_9 = V_H Max.

Table 8: Power-up Timings

Symbol	Parameter	Maximum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	10	ms
$T_{PU-WRITE}$[1]	Power-up to Write Operation	10	ms

Table 9: Capacitance (Ta = 25 °C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0v	6 pF

Note: [1]This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 10: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}	Endurance	1,000 & 10,000[2]	Cycles	MIL-STD-883, Method 1033
T_{DR}[1]	Data Retention	100	Years	MIL-STD-883, Method 1008
V_{ZAP_HBM}[1]	ESD Susceptibility Human Body Model	1000	Volts	MIL-STD-883, Method 3015
V_{ZAP_MM}[1]	ESD Susceptibility Machine Model	200	Volts	JEDEC
I_{LTH}[1]	Latch Up	100	mA	JEDEC Standard 17

Note: [1]This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

[2]See Ordering Information for desired type.

AC Characteristics

Table 11: Read Cycle Timing Parameters

IEEE Symbol	Industry Symbol	Parameter	28VF040-250		28VF040-300		Units
			Min	Max	Min	Max	
tAVAV	T_{RC}	Read Cycle time	250		300		ns
tAVQV	T_{AA}	Address Access Time		250		300	ns
tELQV	T_{CE}	Chip Enable Access Time		250		300	ns
tGLQV	T_{OE}	Output Enable Access Time		120		150	ns
tEHQZ	T_{CLZ}(1)	CE# Low to Active Output	0		0		ns
tGHQZ	T_{OLZ}(1)	OE# Low to Active Output	0		0		ns
tELQX	T_{CHZ}(1)	CE# High to High-Z Output		60		60	ns
tGLQX	T_{OHZ}(1)	OE# High to High-Z Output		60		60	ns
tAXQX	T_{OH}(1)	Output Hold from Address Change	0		0		ns

Table 12: Erase/Program Cycle Timing Parameters

IEEE Symbol	Industry Symbol	Parameter	28VF040-250		28VF040-300		Units
			Min	Max	Min	Max	
tAVA	T_{BP}	Byte Program Cycle Time		35		35	µs
tWLWH	T_{WP}	Write Pulse Width (WE#)	200		200		ns
tAVWL	T_{AS}	Address Setup Time	10		10		ns
tWLAX	T_{AH}	Address Hold Time	100		100		ns
tELWL	T_{CS}	CE# Setup Time	0		0		ns
tWHEX	T_{CH}	CE# Hold Time	0		0		ns
tGHWL	T_{OES}	OE# High Setup Time	20		20		ns
tWGL	T_{OEH}	OE# High Hold Time	20		20		ns
tWLEH	T_{CP}	Write Pulse Width (CE#)	200		200		ns
tDVWH	T_{DS}	Data Setup Time	100		100		ns
tWHDX	T_{DH}	Data Hold Time	20		20		ns
tWHWL2	T_{SE}	Sector Erase Cycle Time		4		4	ms
	T_{RST}(1)	Reset Command Recovery Time		4		4	µs
tWHWL3	T_{SCE}	Software Chip_Erase Cycle Time		20		20	ms
tEHEL	T_{CPH}	CE# High Pulse Width	50		50		ns
tWHWL1	T_{WPH}	WE# High Pulse Width	50		50		ns
	T_{PCP}(1)	Protect Chip Enable Pulse Width	20		20		ns
	T_{PCH}(1)	Protect Chip Enable High Time	20		20		ns
	T_{PAS}(1)	Protect Address Setup Time	0		0		ns
	T_{PAH}(1)	Protect Address Hold Time	100		100		ns

Note: (1)This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.

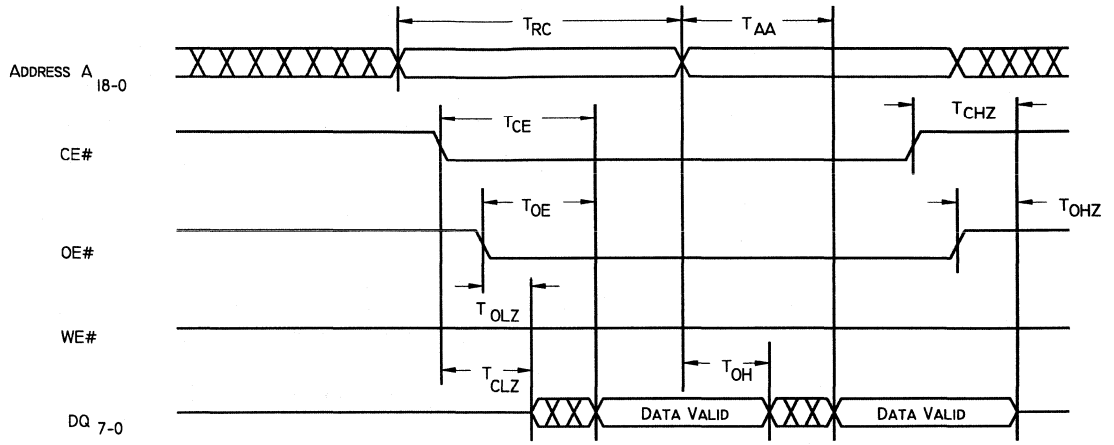


Figure 4: Read Cycle Timing Diagram

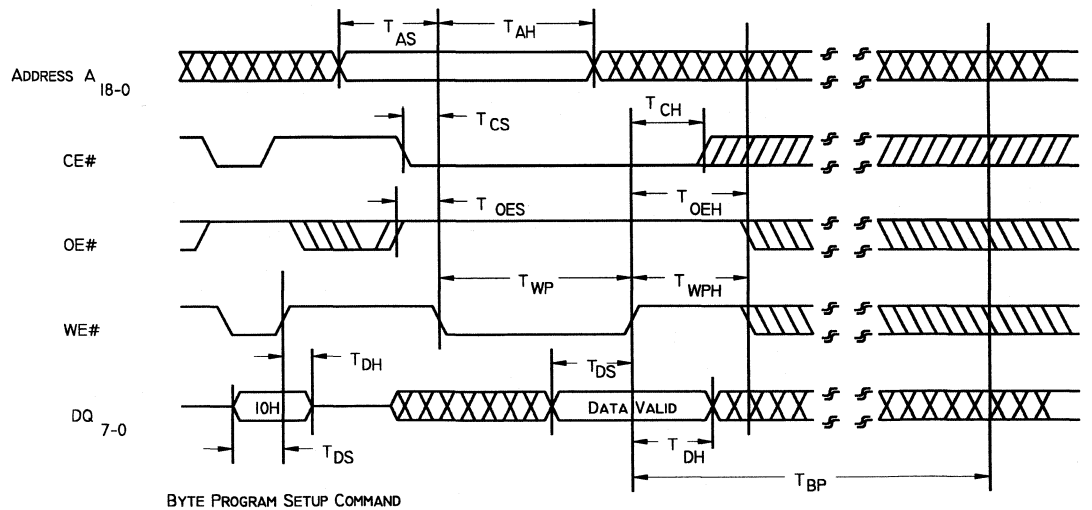


Figure 5: WE# Controlled Byte Program Timing Diagram

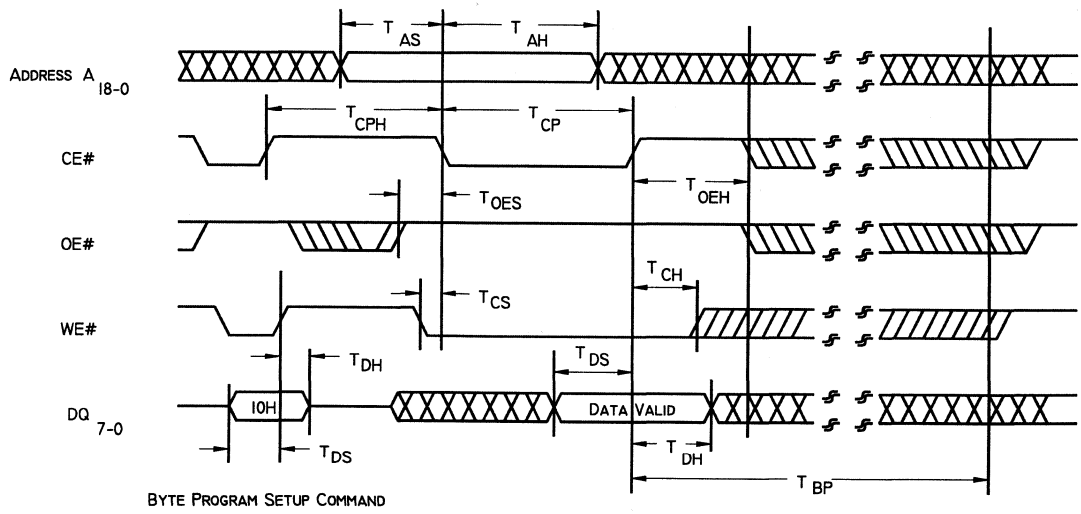


Figure 6: CE# Controlled Byte Program Timing Diagram

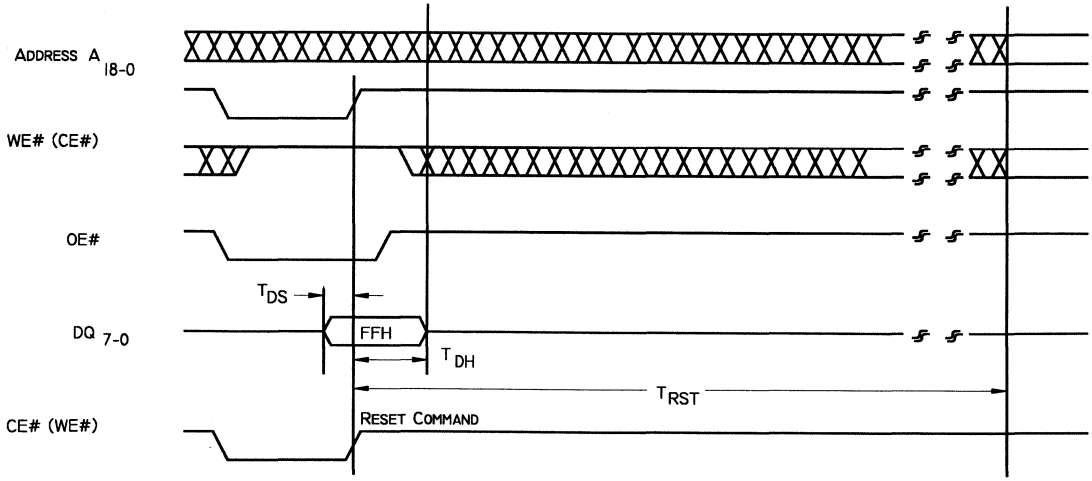


Figure 7: Reset Command Timing Diagram

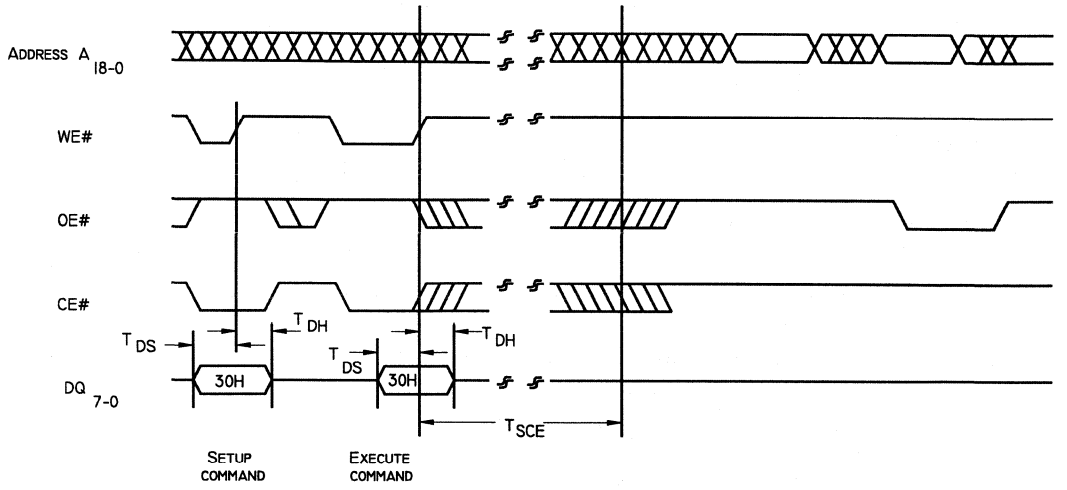


Figure 8: Chip_Erase Timing Diagram

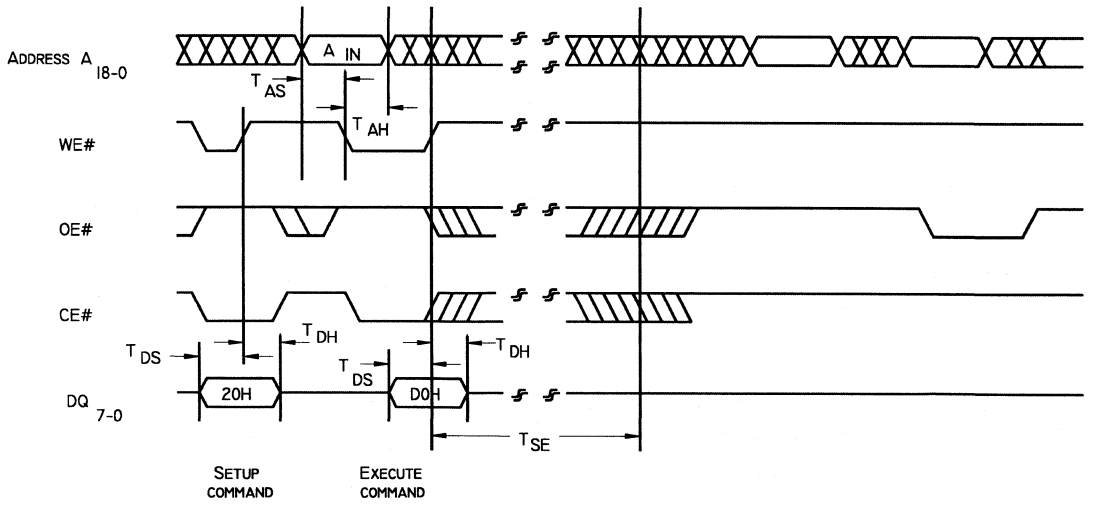
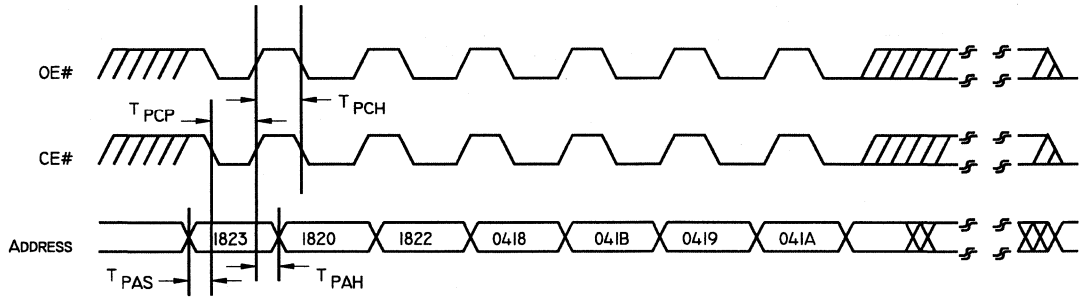


Figure 9: Sector Erase Timing Diagram



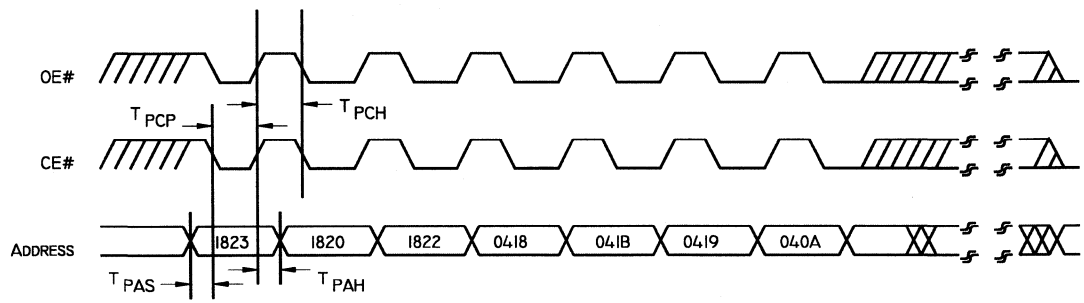
NOTE : A. ADDRESSES ARE LATCHED INTERNALLY ON THE RISING EDGE OF:

1. OE# IF CE# IS KEPT AT LOW ALL TIME.
2. CE# IF OE# IS KEPT AT LOW ALL TIME.
3. THE FIRST PIN TO GO HIGH IF BOTH ARE TOGGLED.

B. ABOVE ADDRESS VALUES ARE IN HEX.

C. ADDRESSES > A_{12} ARE "DON'T CARE"

Figure 10: Software Data Unprotect Timing Diagram



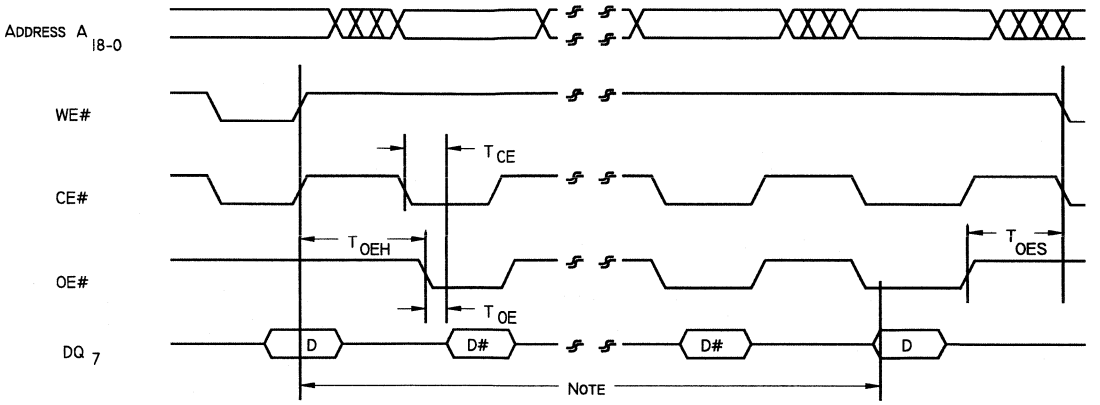
NOTE : A. ADDRESSES ARE LATCHED INTERNALLY ON THE RISING EDGE OF:

1. OE# IF CE# IS KEPT AT LOW ALL TIME.
2. CE# IF OE# IS KEPT AT LOW ALL TIME.
3. THE FIRST PIN TO GO HIGH IF BOTH ARE TOGGLED.

B. ABOVE ADDRESS VALUES ARE IN HEX.

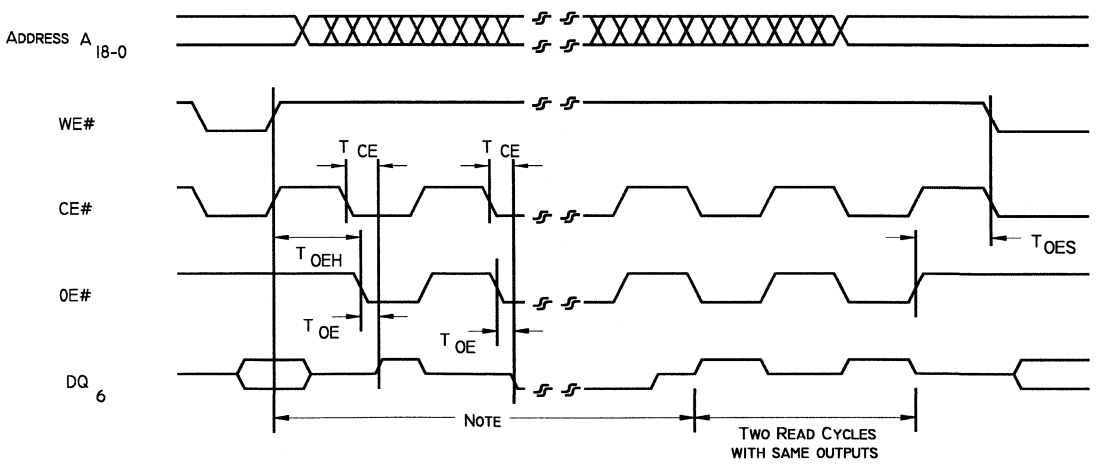
C. ADDRESSES > A_{12} ARE "DON'T CARE"

Figure 11: Software Data Protect Timing Diagram



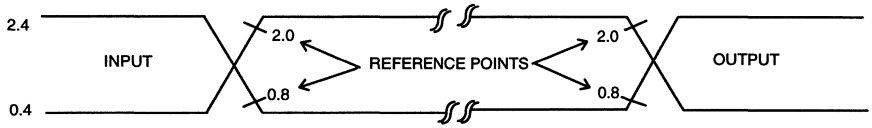
NOTE: THIS TIME INTERVAL SIGNAL CAN BE T_{SE} OR T_{BP} DEPENDING UPON THE SELECTED OPERATION MODE.

Figure 12: Data# Polling Timing Diagram



NOTE: THIS TIME INTERVAL SIGNAL CAN BE T_{SE} OR T_{BP} , DEPENDING UPON THE SELECTED OPERATION MODE.

Figure 13: Toggle Bit Timing Diagram



AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a logic "1" and V_{OL} (0.4 V_{TTL}) for a logic "0". Measurement reference points for inputs and outputs are V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Inputs rise and fall times (10% ↔ 90%) are <10 ns.

Figure 14: AC Input/Output Reference Waveform

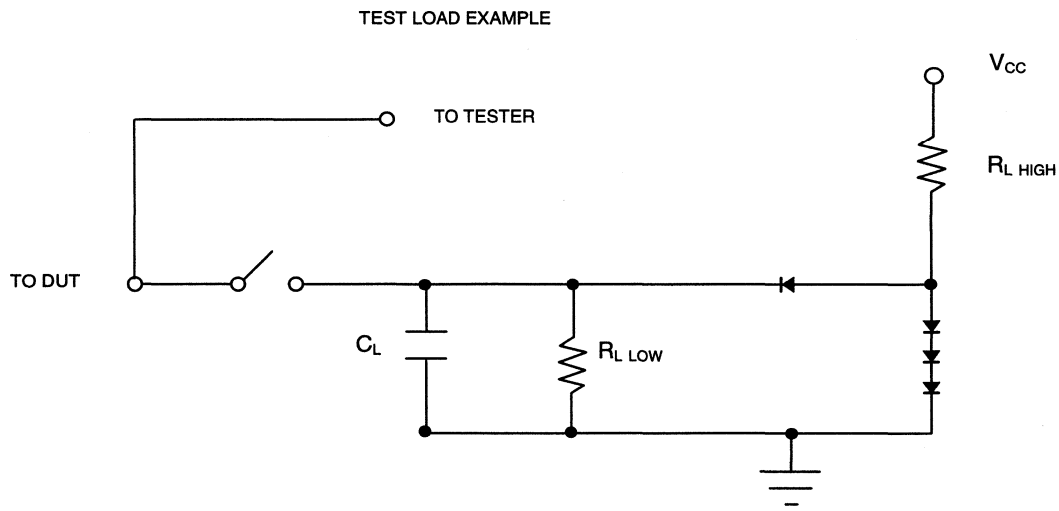


Figure 15: Test Load Example

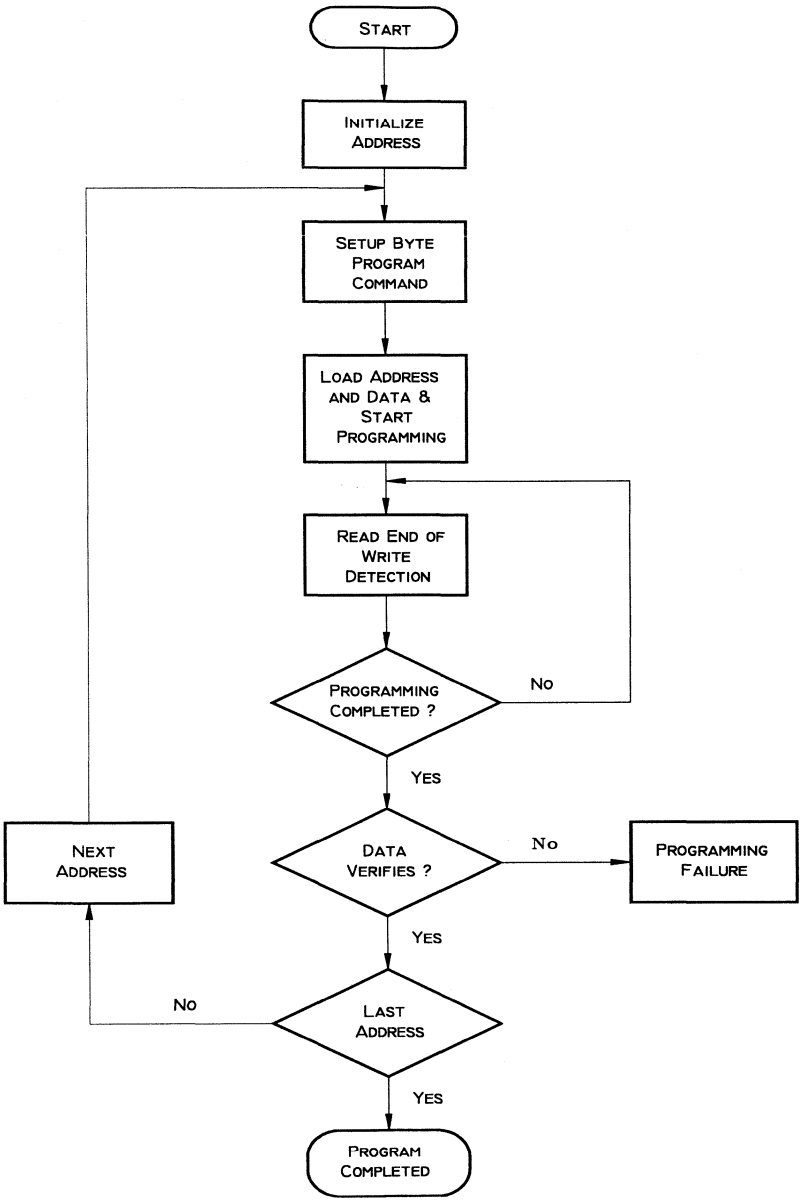


Figure 16: Byte Program Flowchart

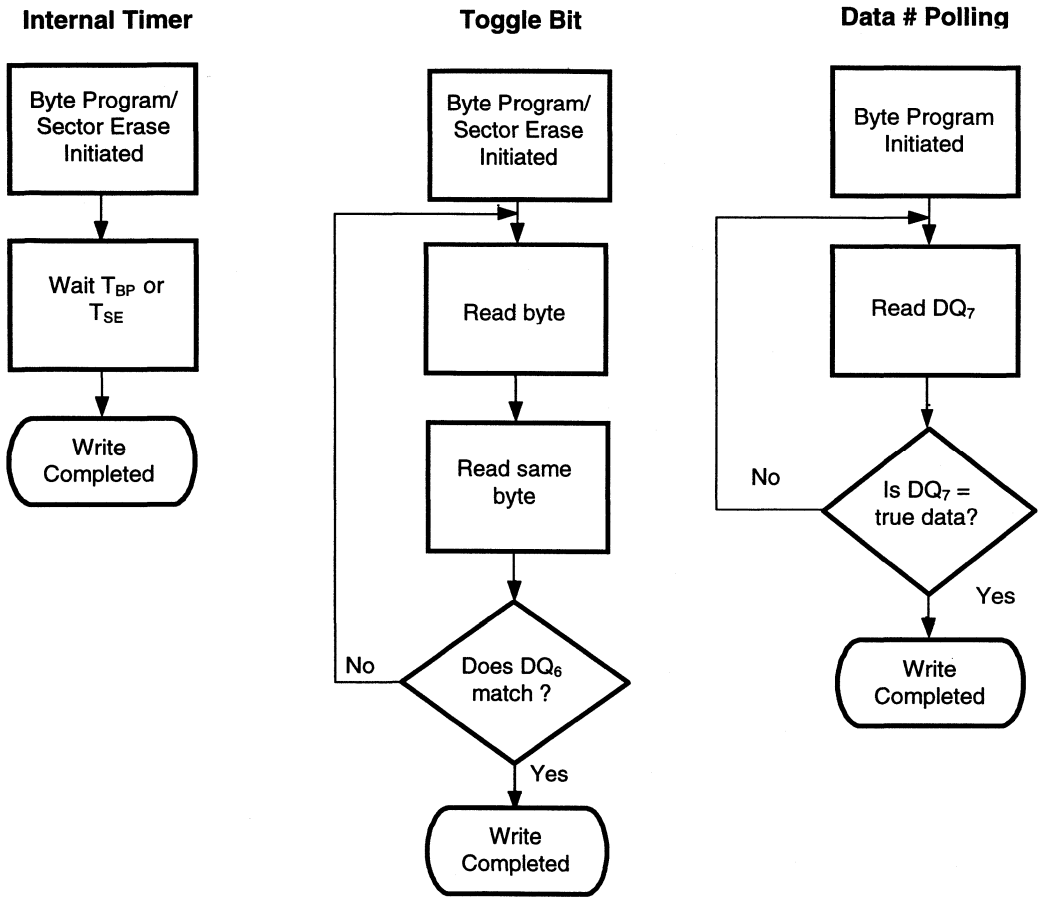


Figure 17: Write Wait Options

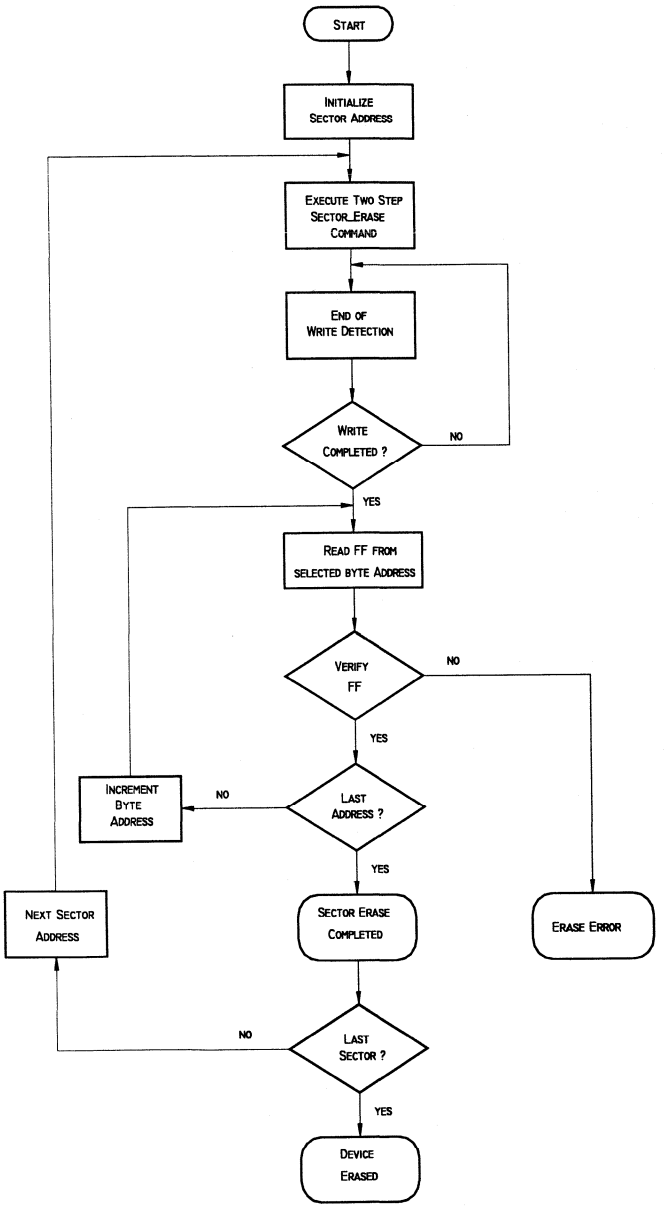


Figure 18: Sector_Erase Flowchart

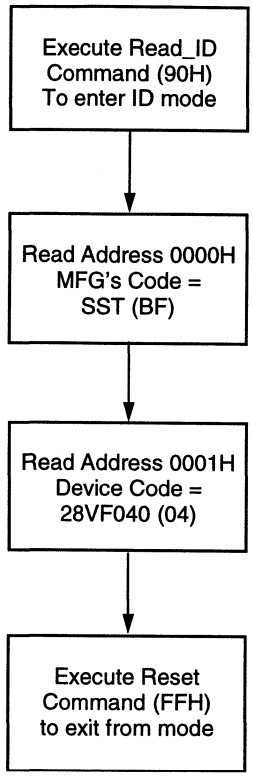
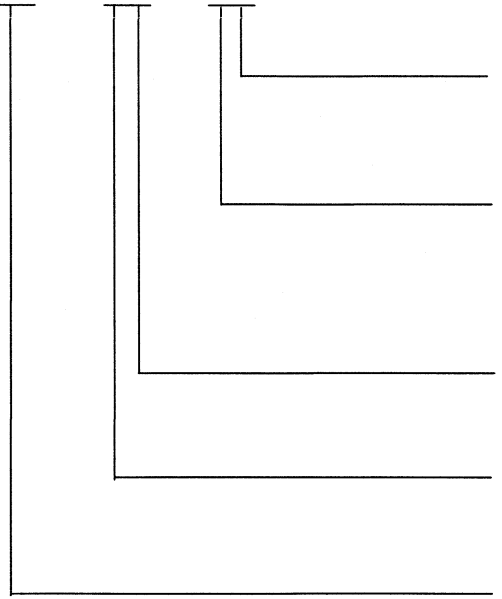


Figure 19: Software Product ID Flow

Product Ordering Information

Device **Speed** **Suffix1** **Suffix2**

SST28VF040 - XXX - XX - XX



Package Modifier
I =40 leads
H = 32 leads
Numeric = Die modifier

Package Type
P = PDIP
N = PLCC
E = TSOP (die up)
U = Unencapsulated die

Operating Temperature
C = Commercial = 0° to 70°C
I = Industrial = -40° to 85°C

Minimum Endurance
3 = 1000 cycles
4 = 10,000 cycles

Read Access Speed
250 = 250 ns
300 = 300 ns

Valid combinations

SST28VF040-250-4C- EH	SST28VF040-250-4C- EI	SST28VF040-250-4C- NH
SST28VF040-250-4C- PH		
SST28VF040-300-4C- EH	SST28VF040-300-4C- EI	SST28VF040-300-4C- NH
SST28VF040-300-4C- PH	SST28VF040-300-4C- U1	
SST28VF040-250-3C- EH	SST28VF040-250-3C- EI	SST28VF040-250-3C- NH
SST28VF040-250-3C- PH		
SST28VF040-300-3C- EH	SST28VF040-300-3C- EI	SST28VF040-300-3C- NH
SST28VF040-300-3C- PH	SST28VF040-300-3C- U1	
SST28VF040-250-4I- EH	SST28VF040-250-4I- EI	SST28VF040-250-4I- NH
SST28VF040-300-4I- EH	SST28VF040-300-4I- EI	SST28VF040-300-4I- NH
SST28VF040-250-3I- EH	SST28VF040-250-3I- EI	SST28VF040-250-3I- NH
SST28VF040-300-3I- EH	SST28VF040-300-3I- EI	SST28VF040-300-3I- NH

Example: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Data Sheet

SST 28PC040
5.0V-only 4 Megabit
PCMCIA Interface EEPROM

July 1996

SST 28PC040
5.0V-only 4 Megabit
PCMCIA Interface EEPROM

Features:

Single 5.0-Volt Read and Write Operations
CMOS SuperFlash EEPROM Technology
Endurance: 250,000 Cycles (typical)
Greater than 100 Years Data Retention
Memory Organization:
512K x 8/1M x 4 PCMCIA Common Memory
1K x 8/2K x 4 Attribute Memory for User Alterable PCMCIA Attribute Memory
Low Power Consumption:

Active Current:	15 mA	(typical)
Standby Current:	5 µA	(typical)

Fast Sector Erase/Byte Program Operation

Byte Program Time:	30 µs	(typical)
Sector Erase Time:	60 µs	(typical)
Complete Memory Rewrite:	15 sec	(typical)

Fast Access Time: 150 and 250 ns
Sector Erase Capability:
256 Bytes/512 Nibbles per Sector
Selectable single Nibble & dual Nibble Access
PCMCIA Byte-wide or Word wide selection
Latched Address and Data
Hardware and Software Data Protection
WP Pin Hardware Write Protection
7-Read-Cycle-Sequence Software Data Protection
End of Write Detection
Toggle Bit
Data# Polling
TTL I/O Compatibility
Packages Available
40-Pin TSOP (10 mm x 14 mm)

Product Description

The 28PC040 is organized as a 512K x 8 (bits) common memory array plus a 1K x 8 attribute memory array. The attribute memory can be accessed by asserting REG# or issuing an Enable_Attribute command. Either one nibble or two nibbles in a byte can be read in one cycle with internal decoding of CEL#, CEH#, and HB. The 28PC040 must be configured as a pair per 1Mbyte of PCMCIA application memory. Each byte in the PCMCIA memory map consists of two nibbles, one from each 28PC040 in the pair.

Each 28PC040 has 4M bits of common memory and 8K bits of attribute memory and is manufactured using SST's proprietary, high performance CMOS SuperFlash EEPROM Technology. The split gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternative approaches. The 28PC040 erases and programs with a 5.0 volt only power supply.

Figure 1 shows the functional blocks of the 28PC040, and shows the memory map consisting of common memory array and the attribute memory array. Figure 2 shows the pin assignments for the TSOP package. Pin description and operation modes are described in Tables 1 through 6.

Device Operation

Commands are used to initiate the memory operations functions of the device. Commands are written to the device using standard microprocessor write sequences. The device is selected by applying the proper input levels to CS_0 and CS_1 (see Table 2A). A command is written by asserting WE# low while keeping CEL# or CEH# low. The address bus is latched on the falling edge of WE#, CEL#, or CEH#, whichever occurs last. The data bus is latched on the rising edge of WE# or CEL#, whichever occurs first. Note, during the software data protection sequence the address are latched on the rising edge of OE# or CEL#, whichever occurs first.

Memory Map

The 28PC040 consists of two memory arrays: the common memory and the attribute memory. The common memory consists of 1M-nibbles and is used for storing data, program codes and other user files. The total available attribute memory is 2K nibbles. The selection between the common and attribute memory maps is controlled by the REG# pin. When REG# is high, the common memory is active. Alternatively, the attribute memory can be accessed through an Enable_Attribute command, which enables the attribute memory access independent of REG#.

Two sectors of the attribute memory are used to store the map of nonconforming sectors. Refer to

Table 9 for details. A maximum of zero nonconforming attribute memory sectors and five nonconforming common memory sectors are allowed when the 28PC040 is shipped.

Command Definitions

Table 7 contains a command list and a brief summary of the commands. The following is a detailed description of the operations initiated by each command.

Sector_Erase Operation

The Sector_Erase operation erases all byte within a sector and is initiated by a setup command and an execute command. A sector contains 512 nibbles. This sector erasability enhances the flexibility and usefulness of the 28PC040, since most applications only need to change a small number of bytes or sectors, not the entire chip.

The setup command is performed by writing 22H to the device. To execute the Sector_Erase operation, the execute command (DDH) must be written to the device. The erase operation begins with the rising edge of the WE# pulse and terminates with the Reset command. The device has an internal timer that will terminate the erase (into the read mode) after T_{SE} if no Reset command has been sent. The end of Erase can be determined using either Data# Polling, Toggle Bit or Successive Reads detection methods. See Figure 9 for timing waveforms.

The two-step sequence of setup command followed by an execute command ensures that only memory contents within the addressed sector are erased and other sectors are not inadvertently erased.

Erase_Verify

The Erase_Verify operation is initiated by writing a single command (AAH). The address bus is latched on the falling edge of WE#, CEL#, or CEH#, whichever occurs last. The Erase_Verify is used only to verify that the device has erased prior to programming. The Erase_Verify uses an internal reference level to provide extra margin compared to normal read levels for "FF" data. This operation automatically resets after reading the byte.

Sector_Erase Flowchart Description

Fast and reliable erasing of the memory contents within a sector is accomplished by following the algorithmic sector erase flowchart as shown in Figure 20. The Sector_Erase operation will terminate after a maximum of 2 ms, if not interrupted. After the initial 40 µs of erase time, a Reset command can be executed to terminate the erase operation followed by an Erase_Verify operation to assure complete erasure. The algorithmic Sector_Erase operation allows for up to seven erase iterations to complete the Sector_Erase. A sector erase iteration is perform by doubling the algorithmic sector erase sector time (T_{ASE} = 40 µs , 80 µs, 160 µs, 320 µs, 640 µs, 1.28 ms and 2.56 ms). The purpose of the successive erase attempts is to optimize the total time required to erase the sector. An additional 150 erase retries at maximum T_{ASE} is allowed to ensure erasure.

Byte_Program Operation

The Byte_Program operation is initiated by writing the setup command (11H). Once the program setup is performed, programming is executed by the next WE# pulse. See Figures 5 and 6 for timing waveforms. The address bus is latched on the falling edge of WE#, CEL# or CEH#, whichever occurs last. The data bus is latched on the rising edge of WE#, CEL# or CEH#, whichever occurs first. The rising edge of WE#, CEL# or CEH#, whichever occurs first, begins the program operation. The program operation is terminated automatically by an internal timer. See Figure 18 for the programming flowchart.

The two-step sequence of a setup command followed command ensures that only the addressed byte is programmed and other bytes are not inadvertently programmed.

The Byte_Program Flowchart Description

Programming data into the 28PC040 is accomplished by following the Byte_Program flowchart shown in Figure 18. The Byte_Program command sets up the byte for programming. The address bus is latched on the falling edge of WE#, CEL# or CEH#, whichever occurs last. The data bus is latched on the rising edge of WE#, CEL# or CEH#, whichever occurs first and begins the program operation. The end of program can be

detected using either the Data# Polling or Toggle bit.

Reset Operation

The Reset command is provided as a means to safely abort the erase or program command sequences. Follow either setup commands (erase or program) with a write of FFH will safely abort the operation. Memory contents will not be altered. After the Reset command, the device returns to the read mode. The Reset command does not enable software data protection. See Figure 7 for timing waveforms.

Read

The Read operation is initiated by setting CEL#, CEH#, and OE# to logic low and setting WE# to logic high (See Table 3). See Figure 4 for read memory timing diagram. The read operation from the host retrieves data from the array. The device remains enabled for read until another operation mode is accessed. During initial power-up, the device is in the read mode and is software data protected. The device must be unprotected to execute a write command.

The read operation of the 28PC040 is controlled by OE# at logic low and either CEL# and/or CEH# at logic low. When CEL# and CEH# are high, the chip is deselected and only standby power will be consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when both CEL# and CEH# are high or OE# is high.

Enable_Attribute Operation

Attribute memory is access by initiating the Enable_Attribute operation with a single command (88H). Read, Sector_Erase, and Byte Program operations can be performed in the attribute memory. The 1K byte of memory includes the PCMCIA attribute memory information. The REG# pin status has no effect on the operation. To return to common memory operations, a Reset command must be issued. The Reset command enables access to the common memory. (See Figure 8)

Read_ID operation

The Read_ID operation is initiated by writing a single command (99H). A read of address 0000H will output the manufacturer's code (BFH). A read of address 0001H will output the device code (11H). Any other valid command will terminate this operation.

Data Protection

In order to protect the integrity of nonvolatile data storage, the 28PC040 provides both hardware and software features to prevent inadvertent writes to the device, for example, during system power-up or power-down. Such provisions are described below.

Hardware Data Protection

The 28PC040 is designed with hardware features to prevent inadvertent writes. This is done in the following ways:

1. Write Inhibit Mode: OE# low, CEL# high, CEH# high, or WE# high will inhibit the write operation.
2. Noise/Glitch Protection: A WE# pulse width of less than 15 ns will not initiate a write cycle.
3. V_{CC} Power Up/Down Detection: The write operation is inhibited when V_{CC} is less than 2.5 V.
4. After power-down the device is in the read mode and the device is in the software data protect state.
5. The WP pin at V_{IH} will put the device in the Write Protect mode.

Software Data Protection (SDP)

The 28PC040 has software methods to further prevent inadvertent writes. In order to perform an erase or program operation, a two-step command sequence consisting of a set-up command followed by an execute command avoids inadvertent erasing and programming of the device.

The 28PC040 will default to software data protection after power up. A sequence of seven consecutive reads at specific addresses will unprotect the device The address sequence is 1823H, 1820H, 1822H, 0418H, 041BH, 0419H, 041AH. The address bus is latched on the rising edge of OE# or CEL#, whichever occurs first. A similar seven read sequence of 1823H, 1820H, 1822H, 0418H, 041BH, 0419H, 040AH will protect the device. Also refer to Figures 10 and 11 for the

7 read cycle sequence Software Data Protection. The I/O pins can be in any state (i.e., high, low, or tristate).

Write Operation Status Detection

The 28PC040 provides two software means to detect the completion of a write cycle, in order to optimize the system write cycle time. The end of a write cycle (erase or program) can be detected by three means: 1) monitoring the Data# Polling bit; 2) monitoring the Toggle bit; or by two successive read of the same data. These three detection mechanisms are described below.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with the DQ used. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the write cycle, otherwise the rejection is valid.

Data# Polling (DQ_3, DQ_7)

The 28PC040 features Data# Polling to indicate the write operation status. During a write operation, any attempt to read the last byte loaded will receive the complement of the true data on DQ_3 and DQ_7. Once the write cycle is completed, DQ_3 for the low nibble and DQ_7 for the high nibble will show true data. The device is then ready for the next operation. See Figure 14 for Data Polling timing waveforms. In order for Data# Polling to function correctly, the byte being polled must be erased prior to programming.

Toggle Bit (DQ_2, DQ_6)

An alternative means for determining the write operation status is by monitoring the Toggle Bit, DQ_2 for the low nibble and DQ_6 for the high nibble. During a write operation, consecutive attempts to read data from the device will result in DQ_2 and DQ_6 toggling between logic 0 (low) and logic 1 (high). When the write cycle is completed, the toggling will stop. The device is then ready for the next operation. See Figure 15 for Toggle Bit timing waveforms.

Successive Reads

An alternative means for determining an end of a write cycle is by reading the same address for two consecutive data matches.

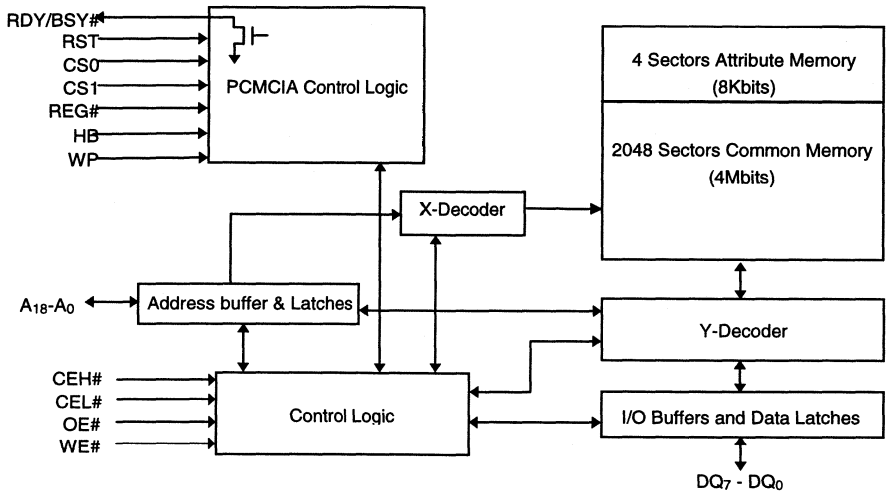


Figure 1: Functional Block Diagram of SST 28PC040

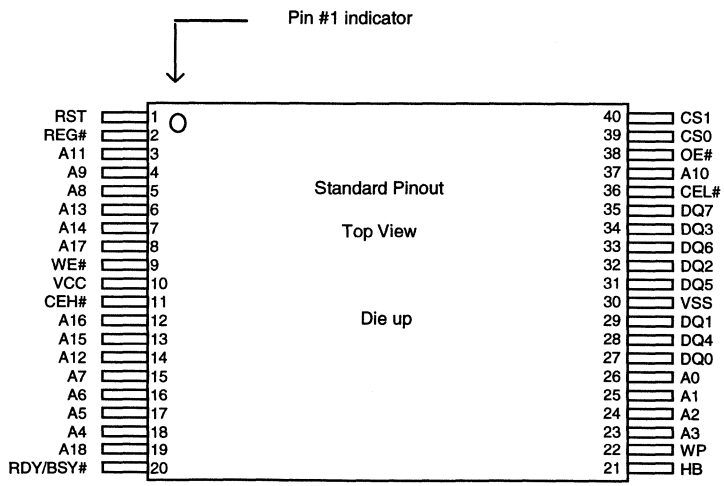


Figure 2: Standard Pin Assignments for 40-pin TSOP Packages.

Table 1: Pin Description

Symbol	Pin Name	Functions
A_{18}-A_8	Row Address Inputs	To provide memory addresses. Row addresses define a sector.
A_7-A_0	Column Address Inputs	Selects the byte within the sector.
DQ_7-DQ_0	Data Input/Output	To output data during read cycles and receive input data during write cycles. Data is internally latched during a write cycle. The outputs are in tri-state when OE#, CEL# or CEH# is high.
CEL#, CEH#	Chip Enable	To activate the device when CEL# or CEH# is low. (1) CEL# to enable the low nibble of DQ_0 to DQ_3 CEH# to enable the high nibble of DQ_4 to DQ_7
OE#	Output Enable	To gate the data output buffers. (1)
WE#	Write Enable	To control the write operations. (1)
Vcc	Power Supply	To provide 5-volt supply (± 10%)
Vss	Ground	
CS_0 - CS_1	Chip Selects	Preset chip selects used for memory pair select.(1) See Table 2A
HB	Half-Byte	Selects Odd/Even nibble for chip.(1)
WP	Write Protect	To activate write protect state. (1) When WP is high, the device becomes a ROM, acknowledging all read operation, and will ignore all operations attempting to alter memory array data. See Table 7.
RDY/BSY#	Read/Busy	This open-drain output requires a 1K pull-up resistor (minimum). (2) This pin is low to indicate the chip is busy internally. Any new instruction must be performed only when RDY/BSY# is high.
REG#	Attribute Memory	To switch from common memory to attribute memory. (1) There are 1Kbits of attribute memory in the 28PC040 decoded by A_9 to A_0. REG# can be overridden by the Enable_Attribute command.
RST	Reset	To reset the device after power-on. (1) RST must be asserted after power-up. After the falling edge of the RST pulse, the 28PC040 will be ready (RDY/BSY#) in ~ 10ms.

Note: (1) This pin is considered as an input for the purposes of the DC Operation Characteristics Table.
(2) This pin is considered as an output for the purposes of the DC Operation Characteristics Table.

Table 2: Operation Modes Selection

Mode	CEL#, CEH#	OE#	WE#	DQ	Address
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	A_{IN}
Byte Program	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}
Sector Erase	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}
Standby	V_{IH}	X	X	High Z	X
Write Inhibit	X	V_{IL}	X	High Z/ D_{OUT}	X
Write Inhibit	X	X	V_{IH}	High Z/ D_{OUT}	X
Software Chip Erase	V_{IL}	V_{IH}	V_{IL}	D_{IN}	See Table 7
Product Identification					
Hardware Mode	V_{IL}	V_{IL}	V_{IH}	Manufacturer Code (BF)	A_{18}-A_1=V_{IL}, A_9=V_H, A_0=V_{IL}
				Device Code (11)	A_{18}-A_1=V_{IL}, A_9=V_H, A_0=V_{IH}
Software Mode	V_{IL}	V_{IH}	V_{IL}		See Table 7
SDP Enable & Disable Mode	V_{IL}	V_{IH}	V_{IL}		See Table 7
Enable_Attribute	V_{IL}	V_{IH}	V_{IL}		See Table 7
Reset	V_{IL}	V_{IH}	V_{IL}		See Table 7

Table 2A: Card Decode Table

Device Part# Suffix	CS_1	CS_0
PCS00A	0	0
PCS01B	0	1
PCS10C	1	0
PCS11D	1	1

Note: The chip is selected by applying the listed logic levels to CS_0 and CS_1. The device part # suffix indicates the preset state.

Table 3: Main Memory Read Functions

Function Mode	REG#	CEH#	CEL#	HB	OE#	WE#	DQ_{7-4} (1)	DQ_{3-0} (2)	A_{18}-A_0 (3)
Standby Mode	X	H	H	X	X	X	High Z	High Z	X
Nibble Access (x4)	H	H	L	L	L	H	High Z	Even Nibble	A_{IN}
Nibble Access (x4)	H	H	L	H	L	H	High Z	Odd Nibble	A_{IN}
Byte Access (x8)	H	L	L	X	L	H	Odd Nibble	Even Nibble	A_{IN}
Odd Nibble Access	H	L	H	X	L	H	Odd Nibble	High Z	A_{IN}

Note: (1) D_{15}-D_8

(2) D_7-D_0

(3) A_{max}-A_1 for 1 Mbyte or higher density applications consisting of one or more pairs of 28PC040.

Table 4: Main Memory Write Functions

Function Mode	REG#	CEH#	CEL#	HB	OE#	WE#	DQ_{7-4}[1]	DQ_{3-0}[2]	A_{18}-A_0[3]
Standby Mode	X	H	H	X	X	X	X	X	X
Nibble Access (x4)	H	H	L	L	H	L	X	Even Nibble	A_{IN}
Nibble Access (x4)	H	H	L	H	H	L	X	Odd Nibble	A_{IN}
Byte Access (x8)	H	L	L	X	H	L	Odd Nibble	Even Nibble	A_{IN}
Odd Nibble Access	H	L	H	X	H	L	Odd Nibble	X	A_{IN}
Write Inhibit	X	X	X	X	L	X	X	X	X

Notes: [1]D_{15}-D_8

[2]D_7-D_0

[3]A_{max}-A_1 for 1 Mbyte or higher density applications consisting of one or more pairs of 28PC040

Table 5: Attribute Memory Read Functions

Function Mode	REG#	CEH#	CEL#	HB	OE#	WE#	DQ_{7-4}[1]	DQ_{3-0}[2]	A_9-A_0[3]
Standby Mode	X	H	H	X	X	X	High Z	High Z	X
Nibble Access (x4)	L	H	L	L	L	H	High Z	Even Nibble	A_{IN}
Nibble Access (x4)	L	H	L	H	L	H	High Z	Odd Nibble	A_{IN}
Byte Access (x8)	L	L	L	X	L	H	Odd Nibble	Even Nibble	A_{IN}
Odd Nibble Access	L	L	H	X	L	H	Odd Nibble	High Z	A_{IN}

Note: [1]D_{15}-D_8

[2]D_7-D_0 for 1 Mbyte or higher density applications consisting of one or more pairs of 28PC040

[3]Other addresses are "don't care"

Table 6: Attribute Memory Write Functions

Function Mode	REG#	CEH#	CEL#	HB	OE#	WE#	DQ_{7-4}[1]	DQ_{3-0}[2]	A_9-A_0
Standby Mode	X	H	H	X	X	X	X	X	X
Nibble Access (x4)	L	H	L	L	H	L	X	Even Nibble	A_{IN}
Nibble Access (x4)	L	H	L	H	H	L	X	Odd Nibble	A_{IN}
Byte Access (x8)	L	L	L	X	H	L	Odd Nibble	Even Nibble	A_{IN}
Odd Nibble Access	L	L	H	X	H	L	Odd Nibble	X	A_{IN}
Write Inhibit	X	X	X	X	L	X	X	X	X

Note: [1]D_{15}-D_8

[2]D_7-D_0; for 1 Mbyte or higher density applications consisting of one or more pairs of 28PC040

[3]Other addresses are "don't care"

Table 7: Software Command Summary

Command Summary	Required	Setup Command Cycle			Execute Command Cycle			WP[6]	SDP[6]
	Cycle(s)	Type[1]	Addr[2,3]	Data[4]	Type[1]	Addr[2,3]	Data[4]		
Sector_Erase	2	W	X	22H	W	SA	DDH	N	N
Byte_Program	2	W	X	11H	W	PA	PD	N	N
Erase_Verify	2	W	VA[5]	AAH	R	X	D_{OUT}	Y	Y
Reset	1	W	X	FFH				Y	Y
Enable_Attribute	1	W	X	88H				Y	Y
Read_ID	3	W	X	99H	R	(9)	(9)	Y	Y
Software_Data_Protect	7	R	(7)						
Software_Data_Unprotect	7	R	(8)						

Notes:

1. Type definition: W = Write, R = Read, X= don't care
2. Addr (Address) definition: SA = Sector Address = A_{18} - A_8, sector size = 512 nibbles; A_7- A_0 = X for this command.
3. Addr (Address) definition: PA = Program Address = A_{18} - A_0.
4. Data definition: PD = Program Data, H = number in hex.
5. Addr (Address) definition: VA = Verify Address = A_{18} - A_0.
6. WP = Hardware Write Protect mode using WP pin, SDP = Software Data Protect mode using 7 Read Cycle Sequence.
   a) Y = the operation can be executed with protection enabled
   b) N = the operation cannot be executed with protection enabled
7. Refer to Figure 13 for the 7 Read Cycle sequence for Software_Data_Protect.
8. Refer to Figure 12 for the 7 Read Cycle sequence for Software_Data_Unprotect.
9. Address 0000H retrieves the manufacturer's code of BFH and address 0001H retrieves the device code of 11H.

Table 8: Memory Array Detail

Memory Array	Sector Select	Byte Select	Nibble Select
Common Memory	A_{18} - A_8	A_7 - A_0	HB
Attribute Memory	A_9 - A_8	A_7 - A_0	HB

Table 9: Nonconforming Sector Map

Attribute Byte Address	D7	D6	D5	D4	D3	D2	D1	D0	Attribute Byte Address	D7	D6	D5	D4	D3	D2	D1	D0
200	X	X	X	X	SNS SUM [3:0]				300	X	X	X	X	SNS SUM [3:0]			
201	X	X	X	X	SNS SUM [7:4]				301	X	X	X	X	SNS SUM [7:4]			
202	X	X	X	X	16	14	12	10	302	X	X	X	X	17	15	13	11
203	X	X	X	X	1E	1C	1A	18	303	X	X	X	X	1F	1D	1B	19
.	X	X	X	X					.	X	X	X	X				
.	X	X	X	X					.	X	X	X	X				
.	X	X	X	X					.	X	X	X	X				
.	X	X	X	X					.	X	X	X	X				
2FE	X	X	X	X	7F6	7F4	7F2	7F0	3FE	X	X	X	X	7F7	7F5	7F3	7F1
2FF	X	X	X	X	7FE	7FC	7FA	7F8	3FF	X	X	X	X	7FF	7FD	7FB	7F9

Note: The Attribute memory bit is "0" when the corresponding Common memory sector is nonconforming. The first 8 sectors of Common memory are always conforming.

Definitions:

1. The SNS sum is the sum of the number of nonconforming sectors and is calculated by summing the "0"s in the remaining bytes of the nonconforming sector map.
2. SNS Sum = Sum of Nonconforming Sector sum. The byte data from these addresses are not included in the sum.
   a) [3:0] = The lower nibble of the SNS sum.
   b) [7:4] = The higher nibble of the SNS sum.
3. Only the lower nibble is used in the attribute memory to map the location of the nonconforming sector(s).

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential ..... -0.5V to V_{CC}+ 0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential ..... -1.0V to V_{CC}+ 1.0V
Voltage on A_9 Pin to Ground Potential ..... -0.5V to 14.0V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Surface Mount Lead Soldering Temperature (3 Seconds) ..... 240°C
Output Short Circuit Current[1] ..... 100 mA

Note: [1]Outputs shorted for no more than one second. No more than one output shorted at a time.

Table 10: Operating Range

Range	Ambient Temp	V_{CC}
Commercial	0 °C to +70 °C	5V±10%

Table 11: AC Conditions of Test

Input Rise/Fall Time.....10 ns
Output Load.....1 TTL Gate and C_L = 100 pF
See Figures 16 and 17

Table 12: DC Operating Characteristics

Symbol	Parameter	Limits		Units	Test Conditions
		Min	Max		
I_{CC}	Power Supply Current				CE# (L or H) = OE# =V_{IL}, WE# =V_{IH}, all I/Os open
	Read		25	mA	Address input = V_{IL}/V_{IH}, at f=1/T_{RC} Min. V_{CC} = V_{CC} Max
	Program and Erase		40	mA	CE# (L or H) =WE# =V_{IL}, OE# =V_{IH} V_{CC} =V_{CC} Max.
I_{SB1}	Standby V_{CC} Current (TTL input)		3	mA	CE# =OE# =WE# = V_{IH}, V_{CC}=V_{CC} Max
I_{SB2}	Standby V_{CC} Current (CMOS input)		20	µA	CE# = OE# = WE# = V_{CC} -0.3V, V_{CC}=V_{CC} Max
I_{LI}	Input Leakage Current		1	µA	V_{IN} = GND to V_{CC}, V_{CC} = V_{CC} Max.
I_{LO}	Output Leakage Current		10	µA	V_{OUT} =GND to V_{CC}, V_{CC} = V_{CC} Max.
V_{IL}	Input Low Voltage		0.8	V	V_{CC} = V_{CC} Max.
V_{IH}	Input High Voltage	2.0		V	V_{CC} = V_{CC} Max.
V_{IL2}	Input Low Voltage, CMOS		0.2	V	V_{CC} = V_{CC} Max.
V_{IH2}	Input High Voltage, CMOS	$V_{CC-0.2}$		V	V_{CC} = V_{CC} Max.
V_{OL}	Output Low Voltage		0.4	V	I_{OL}= 3.2 mA, V_{CC} = V_{CC} Min.
V_{OH}	Output High Voltage	2.4		V	I_{OH} = 2.0 mA, V_{CC} = V_{CC} Min.
V_H	Supervoltage for A_9	11.6	12.4	V	CE#=OE#=V_{IL}, WE#=V_{IH}
I_H	Supervoltage Current for A_9		200	µA	CE#=OE#=V_{IL}, WE#=V_{IH}, A_9 = V_H Max.

Table 13: Power-up Timings

Symbol	Parameter	Maximum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	10	ms
$T_{PU-WRITE}$[1]	Power-up to Write Operation	10	ms

Table 14: Capacitance (Ta = 25 °C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0v	6 pF

Note: [1]This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 15: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}	Endurance	100,000	Cycles	MIL-STD-883, Method 1033
T_{DR}[1]	Data Retention	100	Years	MIL-STD-883, Method 1008
V_{ZAP_HBM}[1]	ESD Susceptibility Human Body Model	1,000	Volts	MIL-STD-883, Method 3015
V_{ZAP_MM}[1]	ESD Susceptibility Machine Model	200	Volts	JEDEC
I_{LTH}[1]	Latch Up	100	mA	JEDEC Standard 17

Note: [1]This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

AC Characteristics

Table 16: Read Cycle Timing Parameters

PCMCIA Symbol	IEEE Symbol	Industry Symbol	Parameter	28PC040-150		28PC040-250		Units
				Min	Max	Min	Max	
tCR	tAVAV	T_{RC}	Read Cycle time	150		250		ns
ta(A)	tAVQV	T_{AA}	Address Access Time		150		250	ns
ta(CE)	tELQV	T_{CE}	Chip Enable Access Time		150		250	ns
ta(OE)	tGLQV	T_{OE}	Output Enable Access Time		70		100	ns
tdis(CE)	tEHQZ	T_{CLZ}[1]	CE# Low to Active Output	0		0		ns
tdis(OE)	tGHQZ	T_{OLZ}[1]	OE# Low to Active Output	0		0		ns
ten(CE)	tELQX	T_{CHZ}[1]	CE# High to High-Z Output		40		40	ns
ten(OE)	tGLQX	T_{OHZ}[1]	OE# High to High-Z Output		40		40	ns
tv(A)	tAXQX	T_{OH}[1]	Output Hold from Address Change	0		0		ns

Table 17: Erase/Progarm Cycle Timing Parameters

PCMCIA Symbol	IEEE Symbol	Industrial Symbol	Parameter	28PC040-150		28PC040-250		Units
				Min	Max	Min	Max	
tCW	tAVA	T_{BP}	Byte Program Cycle Time		35		35	µs
tw(WE)	tWLWH	T_{WP}	Write Pulse Width (WE#)	80		100		ns
tsu(A)	tAVWL	T_{AS}	Address Setup Time	10		10		ns
th(a)	tWLAX	T_{AH}	Address Hold Time	50		50		ns
tsu(CE)	tELWL	T_{CS}	CE# Setup Time	0		0		ns
th(CE)	tWHEX	T_{CH}	CE# Hold Time	0		0		ns
tsu(OE-WE)	tGHWL	T_{OES}	OE# High Setup Time	10		10		ns
th(OE-WE)	tWGL	T_{OEH}	OE# High Hold Time	10		10		ns
tw(CE)	tWLEH	T_{CP}	Write Pulse Width (CE#)	80		100		ns
tsu(D-WEH)	tDVWH	T_{DS}	Data Setup Time	50		50		ns
th(D)	tWHDX	T_{DH}	Data Hold Time	10		10		ns
	tWHWL2	T_{SE}	Sector Erase Cycle Time		2		2	ms
		T_{RST}[1]	Reset Command Recovery Time		4		4	µs
		T_{EVD}	Erase Verify Timing Delay	.025		0.25		µs
		T_{ERD}	Erase Reset Timing Delay	4		4		µs
		T_{ASE}	Algorithmic Sector Erase Cycle Time	0.04	2.56	0.04	2.56	ms
	tEHEL	T_{CPH}	CE# High Pulse Width	50		50		ns
	tWHWL1	T_{WPH}	WE# High Pulse Width	50		50		ns
	tRHRL	T_{HR}[1]	Hardware Reset Pulse Width	10		10		µs
	tRHBL	T_{RBS}[1]	Hardware Reset High to RDY/BSY# Active	10		10		µs
		T_{PCP}[1]	Protect Chip Enable Pulse Width	10		10		ns
		T_{PCH}[1]	Protect Chip Enable High Time	10		10		ns
		T_{PAS}[1]	Protect Address Setup Time	0		0		ns
		T_{PAH}[1]	Protect Address Hold Time	50		50		ns

Note: [1]This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.

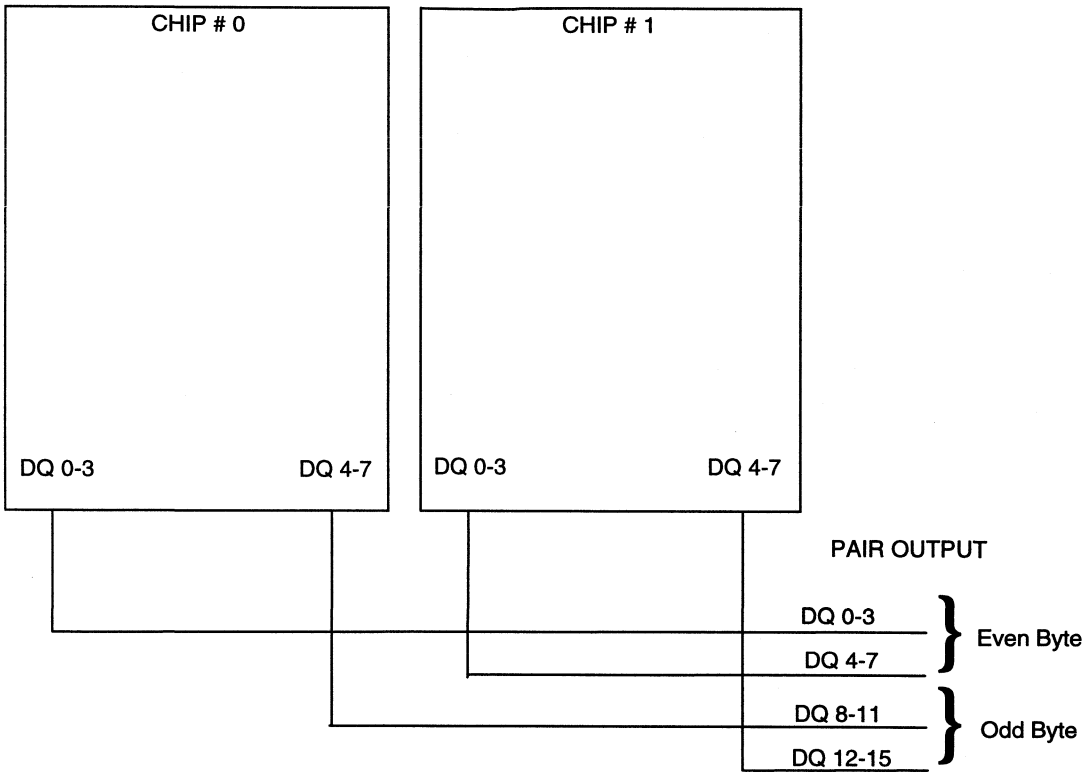


Figure 3: Chip Pair Mapping (Nibble Access)

Table 18: Nibble Access Table

Byte	Nibble	Outputs	CEL#	CEH#	HB
Even	Even Nibble	0-3	L	H	L
Even	Odd Nibble	4-7	L	H	H
Odd	Even Nibble	8-11	H	L	L
Odd	Odd Nibble	12-15	H	L	H

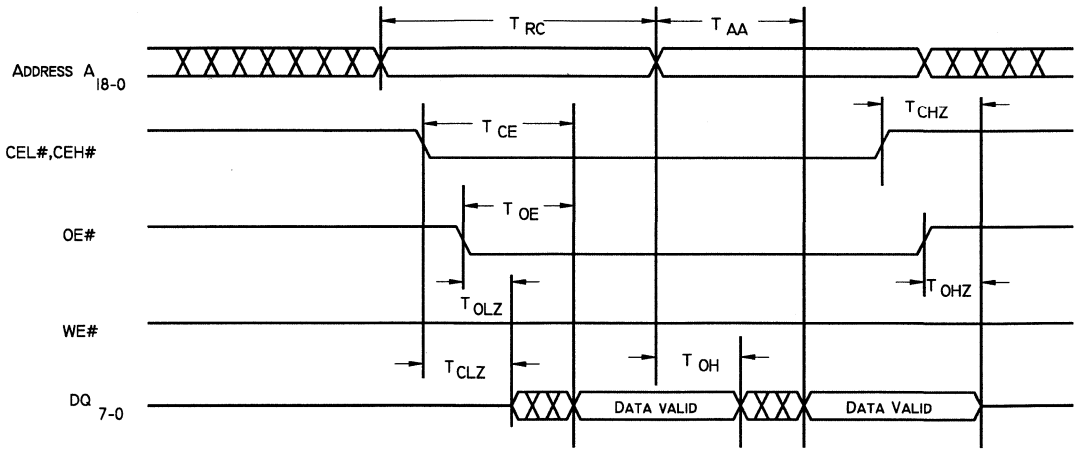


Figure 4: Read Cycle Timing Diagram

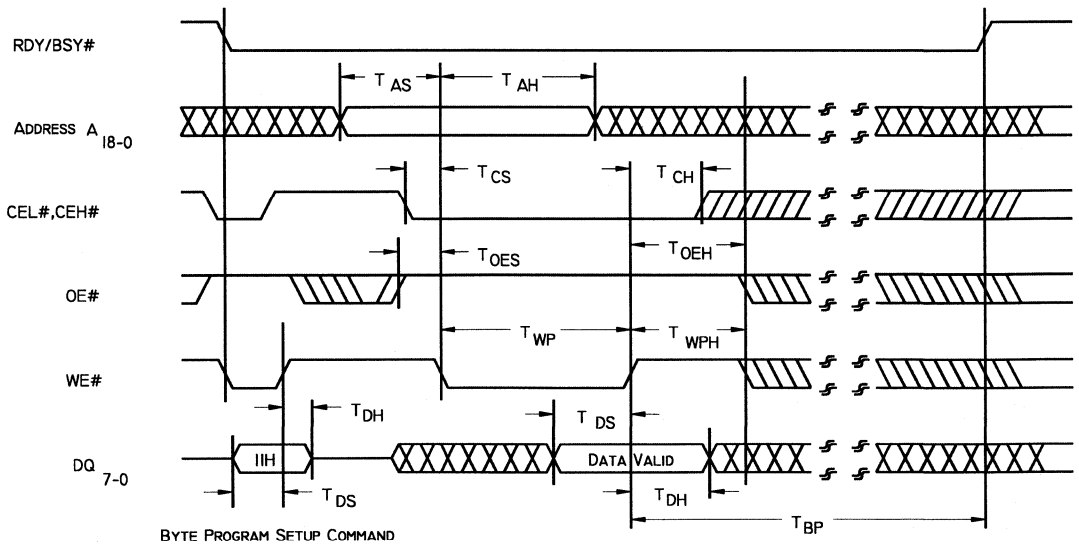


Figure 5: WE# Controlled Byte Program Timing Diagram

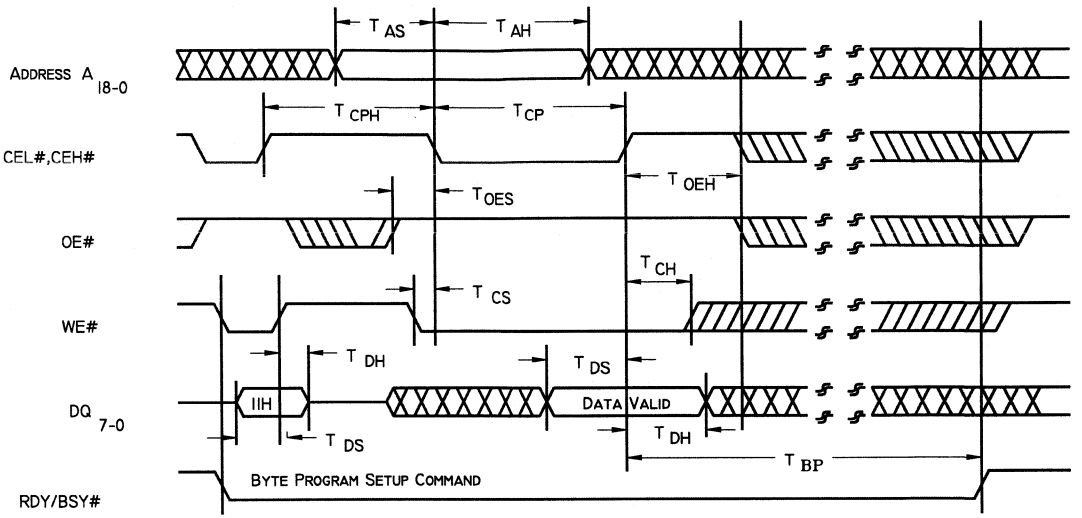


Figure 6: CE# Controlled Byte Program Timing Diagram

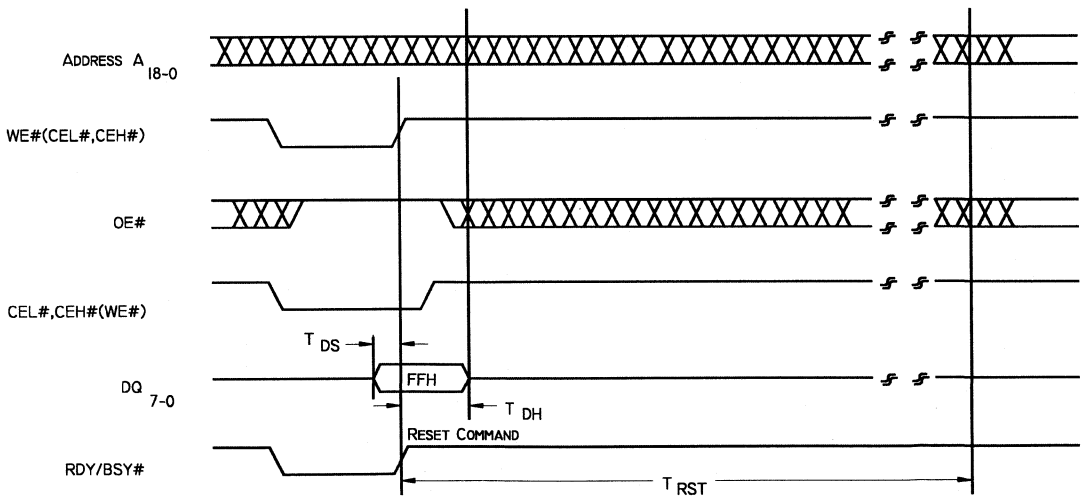
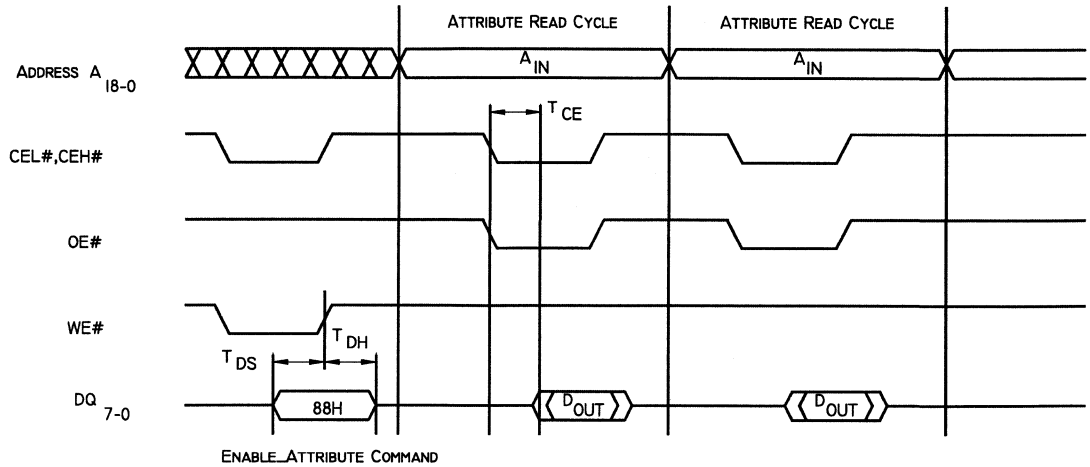


Figure 7: Reset Command Timing Diagram



1) READ, SECTOR_ERASE, BYTE_PROGRAM OPERATIONS CAN BE PERFORMED AT THIS TIME. THE READ OPERATION IS INTENDED AS AN EXAMPLE FOR THIS TIMING DIAGRAM ONLY.

Figure 8: Enable_Attribute Timing Diagram

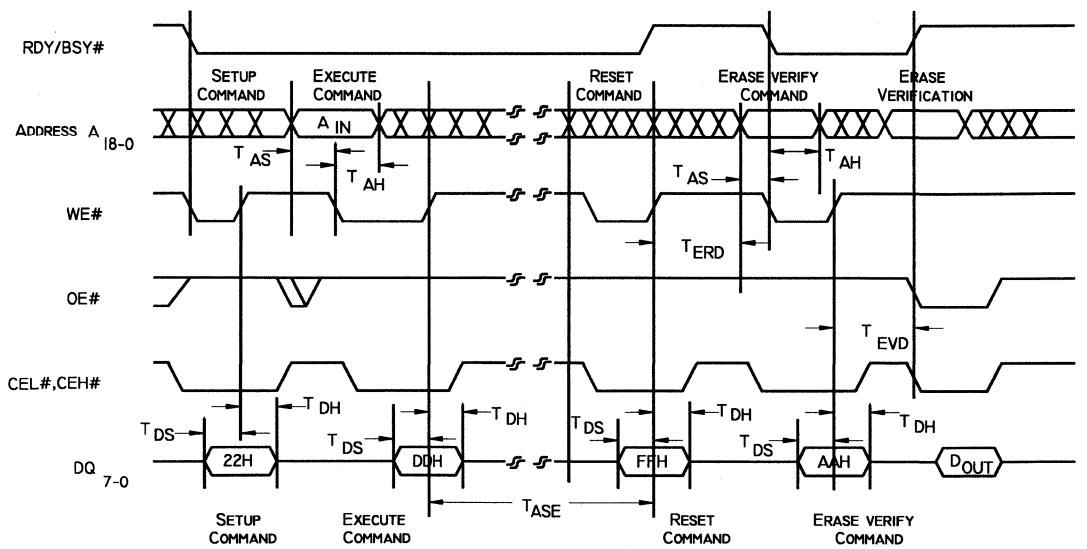
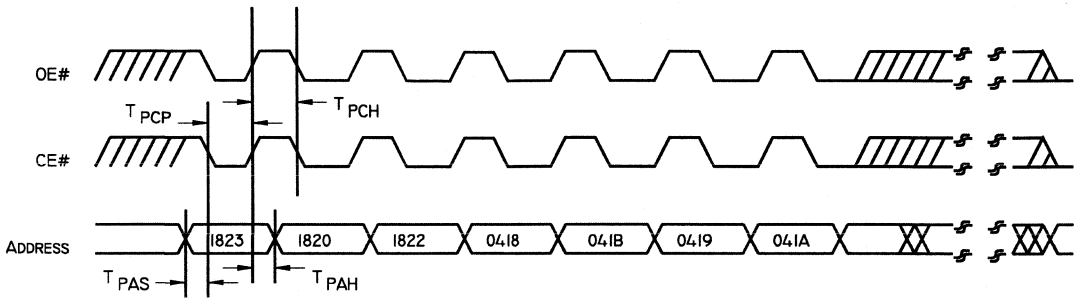


Figure 9: Sector Erase Timing Diagram



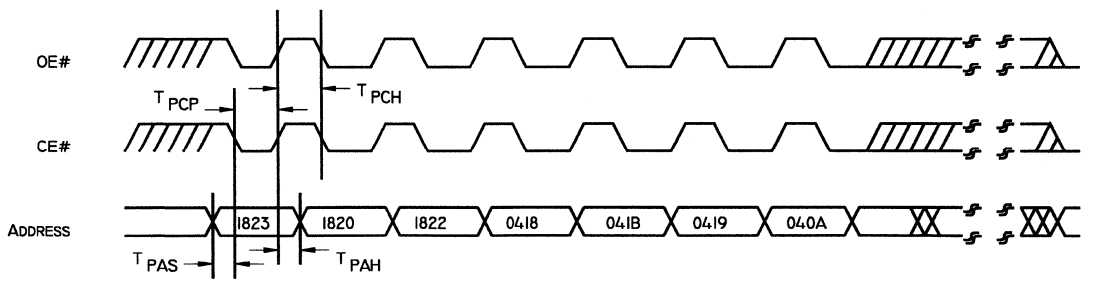
NOTE : A. ADDRESSES ARE LATCHED INTERNALLY ON THE RISING EDGE OF:

1. OE# IF CE# IS KEPT AT LOW ALL TIME.
2. CE# IF OE# IS KEPT AT LOW ALL TIME.
3. THE FIRST PIN TO GO HIGH IF BOTH ARE TOGGLED.

B. ABOVE ADDRESS VALUES ARE IN HEX.

C. ADDRESSES > A_{12} ARE "DON'T CARE"

Figure 10: Software Data Unprotect Timing Diagram



NOTE : A. ADDRESSES ARE LATCHED INTERNALLY ON THE RISING EDGE OF:

1. OE# IF CE# IS KEPT AT LOW ALL TIME.
2. CE# IF OE# IS KEPT AT LOW ALL TIME.
3. THE FIRST PIN TO GO HIGH IF BOTH ARE TOGGLED.

B. ABOVE ADDRESS VALUES ARE IN HEX.

C. ADDRESSES > A_{12} ARE "DON'T CARE"

Figure 11: Software Data Protect Timing Diagram

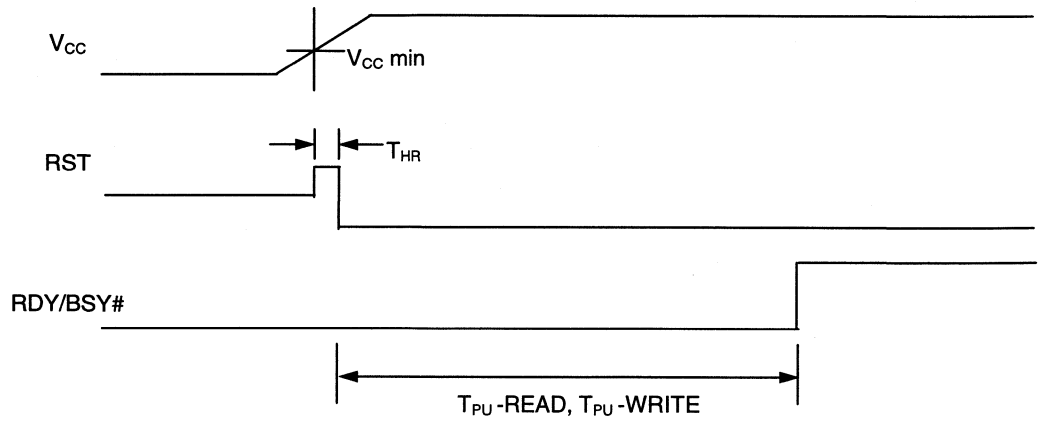


Figure 12: RST and RDY/BSY# waveforms - Power up to Read and Write

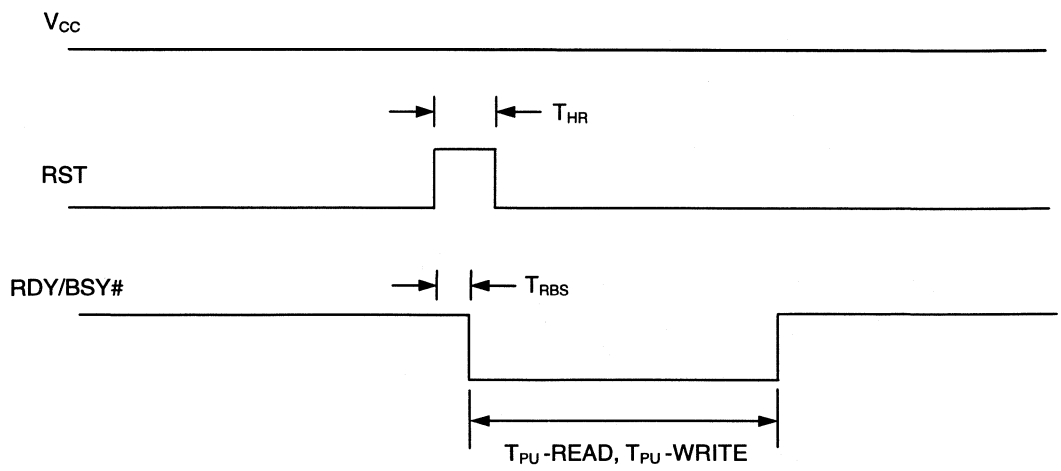
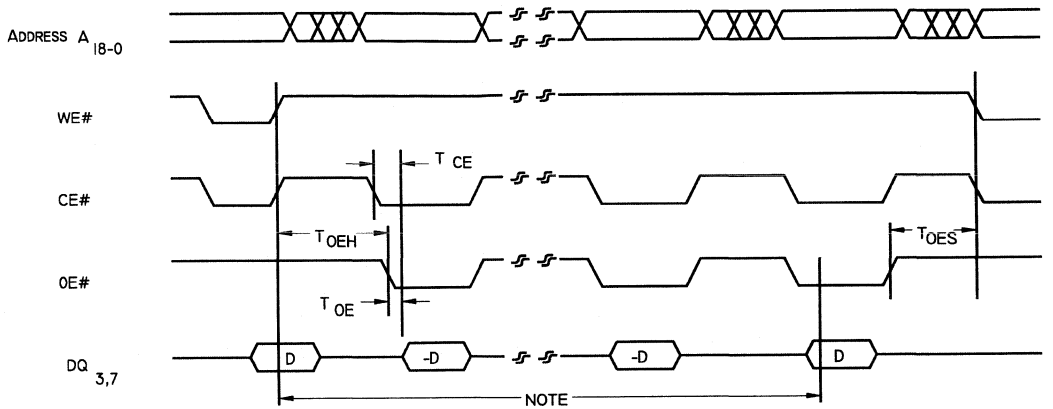
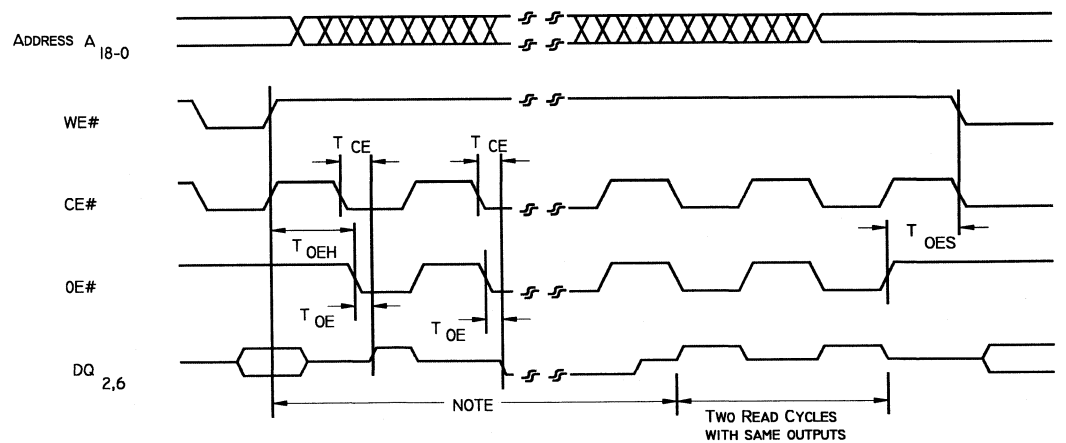


Figure 13: RST and RDY/BSY# waveforms - Hardware Reset



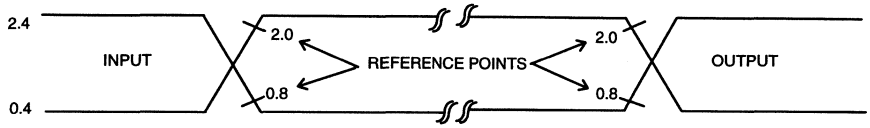
NOTE: THIS TIME INTERVAL SIGNAL CAN BE T_{SE} OR T_{BP}, DEPENDING UPON THE SELECTED OPERATION MODE.

Figure 14: Data# Polling Timing Diagram



NOTE: THIS TIME INTERVAL SIGNAL CAN BE T_{SE} OR T_{BP}, DEPENDING UPON THE SELECTED OPERATION MODE.

Figure 15: Toggle Bit Timing Diagram



AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a logic "1" and V_{OL} (0.4 V_{TTL}) for a logic "0". Measurement reference points for inputs and outputs are V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Inputs rise and fall times (10% ↔ 90%) are <10 ns.

Figure 16: AC Input/Output Reference Waveform

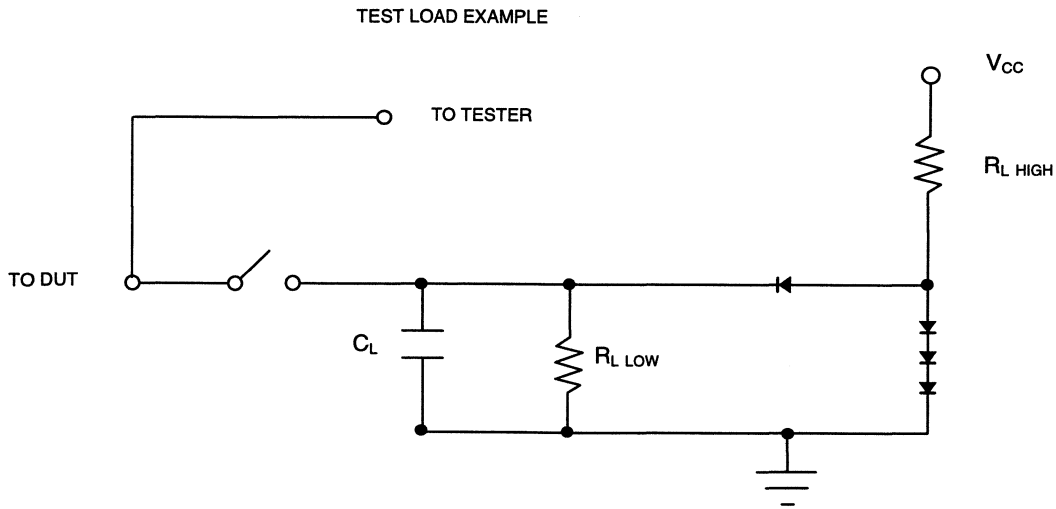


Figure 17: Test Load Example

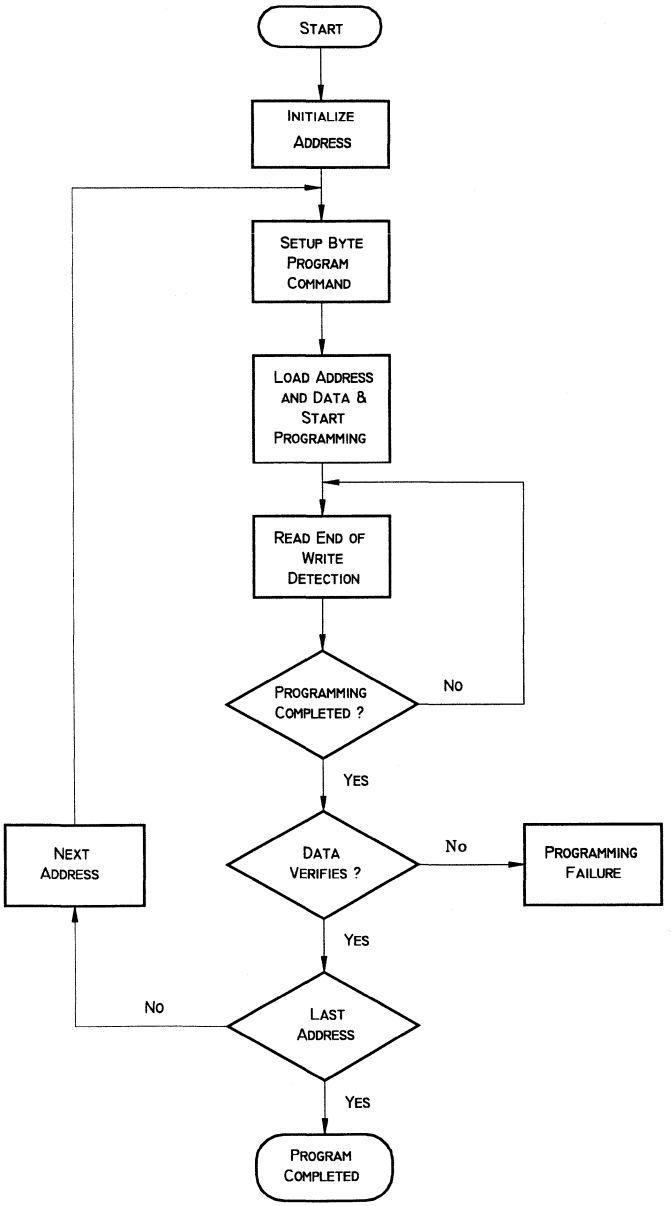


Figure 18: Byte Program Flowchart

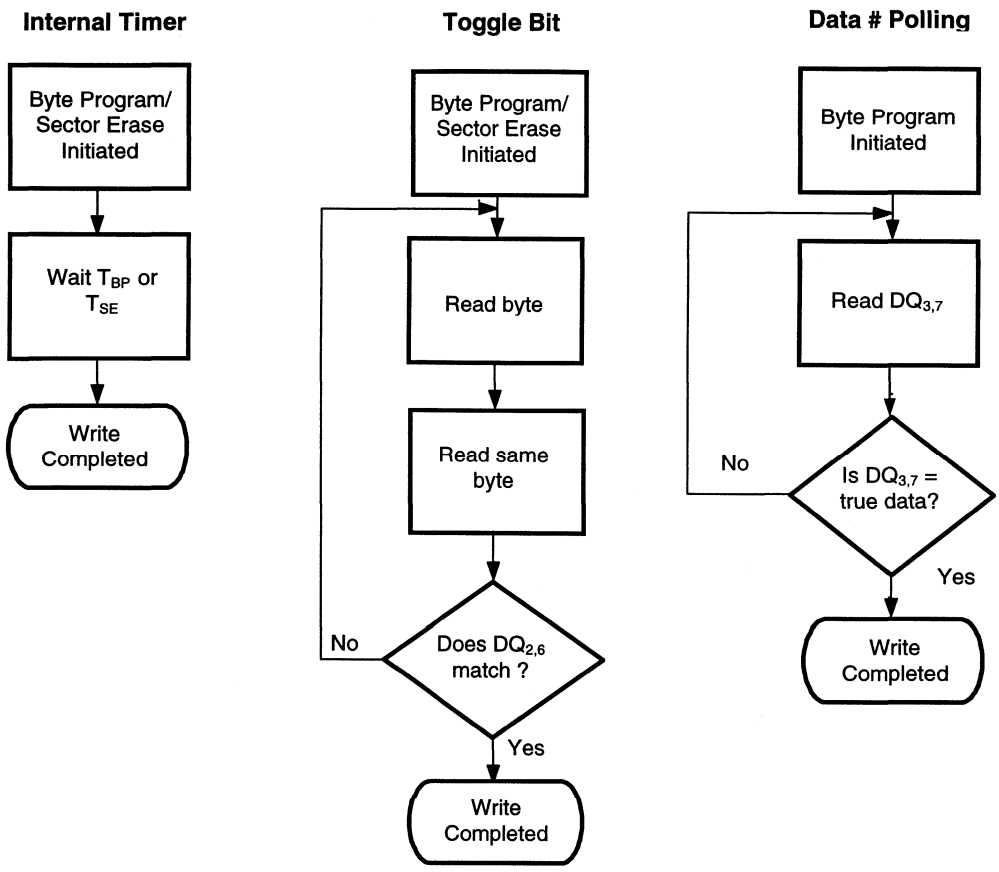


Figure 19: Write Wait Options

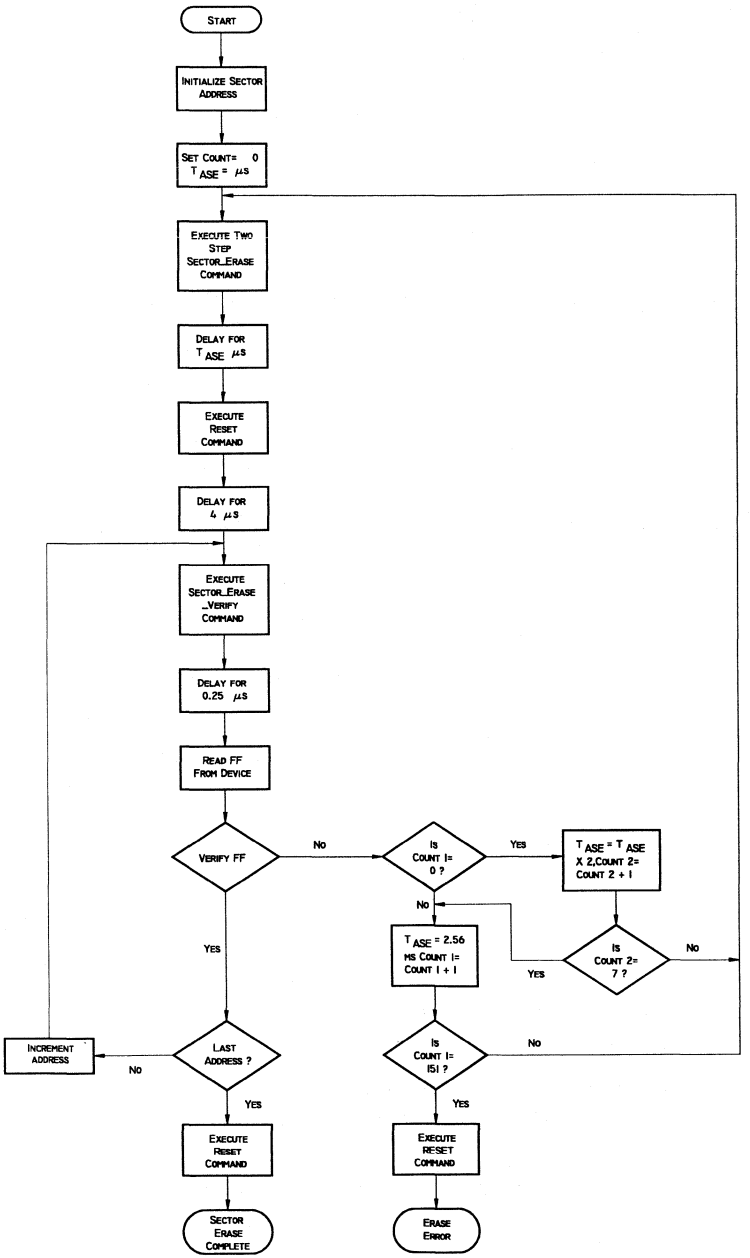


Figure 20: Sector_Erase Flowchart

Product Ordering Information

Device **Speed** **Suffix1** **Suffix2** **Suffix3**

SST28PC040 - XXX - XX - XX XXXX

Card Decode
S00A = PCS00A
S01B = PCS01B
S10C = PCS10C
S11D = PCS11D

Package Modifier
I = 40 leads

Package Type
W = TSOP (die up)

Operating Temperature
C = Commercial = 0° to 70°C

Minimum Endurance
5 = 100,000 cycles

Read Access Speed
250 = 250 ns
150 = 150 ns

Valid combinations

SST28PC040-250-5C-WI-S00A	SST28PC040-250-5C-WI-S01B
SST28PC040-150-5C-WI-S00A	SST28PC040-150-5C-WI-S01B
SST28PC040-250-5C-WI-S10C	SST28PC040-250-5C-WI-S11D
SST28PC040-150-5C-WI-S10C	SST28PC040-150-5C-WI-S11D

Example: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Preliminary Specifications

SST 28LP040
3.0V-only 4 Megabit
PCMCIA Interface EEPROM

July 1996

SST 28LP040
3.0V-only 4 Megabit PCMCIA Interface EEPROM

Preliminary Specifications

Features:

Single 3.0-Volt Read and Write Operations
CMOS SuperFlash EEPROM Technology
- Endurance: 250,000 Cycles (typical)
- Greater than 100 years Data Retention

Memory Organization:
- 512K x 8/1M x 4 PCMCIA common memory
- 1K x 8/2K x 4 attribute memory for user alterable PCMCIA attribute memory

Low Power Consumption:

Active Current:	10 mA	(typical)
Standby Current:	5 µA	(typical)

Fast Sector Erase and Byte Program Operation

Byte Program Time:	30 µs	(typical)
Sector Erase Time:	60 µs	(typical)
Complete Memory Rewrite:	15 sec	(typical)

Fast Access Time: 250 ns

Sector Erase Capability:
- 256 bytes/512 nibbles per Sector

Selectable single Nibble & dual Nibble Access
PCMCIA Byte-wide or Word wide selection
Latched Address and Data
Hardware and Software Data Protection
- WP pin Hardware Write Protection
- 7-read-cycle-sequence Software Data Protection

End of Write Detection
- Toggle Bit
- Data# Polling

TTL I/O Compatibility
Packages Available
- 40-Pin TSOP (10 mm x 14 mm)

Product Description

The 28LP040 is organized as a 512K x 8 (bits) common memory array plus a 1K x 8 attribute memory array. The attribute memory can be accessed by asserting REG# or issuing an Enable_Attribute command. Either one nibble or two nibbles in a byte can be read in one cycle with internal decoding of CEL#, CEH#, and HB. The 28LP040 must be configured as a pair per 1Mbyte of PCMCIA application memory. Each byte in the PCMCIA memory map consists of two nibbles, one from each 28LP040 in the pair.

Each 28LP040 has 4M bits of common memory and 8K bits of attribute memory and is manufactured using SST's proprietary, high performance CMOS SuperFlash EEPROM Technology. The split gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternative approaches. The 28LP040 erases and programs with a 3.0 volt only power supply. (V_{CC}: 3.0V to 3.6V)

Figure 1 shows the functional blocks of the 28LP040, and shows the memory map consisting of common memory array and the attribute memory array. Figure 2 shows the pin assignments for the TSOP package. Pin description and operation modes are described in Tables 1 through 6.

Device Operation

Commands are used to initiate the memory operations functions of the device. Commands are written to the device using standard microprocessor write sequences. The device is selected by applying the proper input levels to CS_0 and CS_1 (see Table 2A). A command is written by asserting WE# low while keeping CEL# or CEH# low. The address bus is latched on the falling edge of WE#, CEL#, or CEH#, whichever occurs last. The data bus is latched on the rising edge of WE# or CEL#, whichever occurs first. Note, during the software data protection sequence the address are latched on the rising edge of OE# or CEL#, whichever occurs first.

Memory Map

The 28LP040 consists of two memory arrays: the common memory and the attribute memory. The common memory consists of 1M-nibbles and is used for storing data, program codes and other user files. The total available attribute memory is 2K nibbles. The selection between the common and attribute memory maps is controlled by the REG# pin. When REG# is high, the common memory is active. Alternatively, the attribute memory can be accessed through an Enable_Attribute command, which enables the attribute memory access independent of REG#.

Two sectors of the attribute memory are used to store the map of nonconforming sectors. Refer to Table 9 for details. A maximum of zero nonconforming attribute memory sectors and five nonconforming common memory sectors are allowed when the 28LP040 is shipped.

Command Definitions

Table 7 contains a command list and a brief summary of the commands. The following is a detailed description of the operations initiated by each command.

Sector_Erase Operation

The Sector_Erase operation erases all byte within a sector and is initiated by a setup command and an execute command. A sector contains 512 nibbles. This sector erasability enhances the flexibility and usefulness of the 28LP040, since most applications only need to change a small number of bytes or sectors, not the entire chip.

The setup command is performed by writing 22H to the device. To execute the Sector_Erase operation, the execute command (DDH) must be written to the device. The erase operation begins with the rising edge of the WE# pulse and terminates with the Reset command. The device has an internal timer that will terminate the erase (into the read mode) after T_{SE} if no Reset command has been sent. The end of Erase can be determined using either Data# Polling, Toggle Bit or Successive Reads detection methods. See Figure 9 for timing waveforms.

The two-step sequence of setup command followed by an execute command ensures that only memory contents within the addressed sector are erased and other sectors are not inadvertently erased.

Erase_Verify

The Erase_Verify operation is initiated by writing a single command (AAH). The address bus is latched on the falling edge of WE#, CEL#, or CEH#, whichever occurs last. The Erase_Verify is used only to verify that the device has erased prior to programming. The Erase_Verify uses an internal reference level to provide extra margin compared to normal read levels for "FF" data. This operation automatically resets after reading the byte.

Sector_Erase Flowchart Description

Fast and reliable erasing of the memory contents within a sector is accomplished by following the algorithmic sector erase flowchart as shown in Figure 20. The Sector_Erase operation will terminate after a maximum of 2 ms, if not interrupted. After the initial 40 µs of erase time, a Reset command can be executed to terminate the erase operation followed by an Erase_Verify operation to assure complete erasure. The algorithmic Sector_Erase operation allows for up to seven erase iterations to complete the Sector_Erase. A sector erase iteration is perform by doubling the algorithmic sector erase sector time (T_{ASE} = 40 µs , 80 µs, 160 µs, 320 µs, 640 µs, 1.28 ms and 2.56 ms). The purpose of the successive erase attempts is to optimize the total time required to erase the sector. An additional 150 erase retries at maximum T_{ASE} is allowed to ensure erasure.

Byte_Program Operation

The Byte_Program operation is initiated by writing the setup command (11H). Once the program setup is performed, programming is executed by the next WE# pulse. See Figures 5 and 6 for timing waveforms. The address bus is latched on the falling edge of WE#, CEL# or CEH#, which ever occurs last. The data bus is latched on the rising edge of WE#, CEL# or CEH#, which ever occurs first. The rising edge of WE#, CEL# or CEH#, which ever occurs first, begins the program operation. The program operation is terminated automatically by an internal timer. See Figure 18 for the programming flowchart.

The two-step sequence of a setup command followed command ensures that only the addressed byte is programmed and other bytes are not inadvertently programmed.

The Byte_Program Flowchart Description

Programming data into the 28LP040 is accomplished by following the Byte_Program flowchart shown in Figure 18. The Byte_Program command sets up the byte for programming. The address bus is latched on the falling edge of WE#, CEL# or CEH#, which ever occurs last. The data bus is latched on the rising edge of WE#, CEL# or CEH#, which ever occurs first and begins the pro

gram operation. The end of program can be detected using either the Data# Polling or Toggle bit.

Reset Operation

The Reset command is provided as a means to safely abort the erase or program command sequences. Follow either setup commands (erase or program) with a write of FFH will safely abort the operation. Memory contents will not be altered. After the Reset command, the device returns to the read mode. The Reset command does not enable software data protection. See Figure 7 for timing waveforms.

Read

The Read operation is initiated by setting CEL#, CEH#, and OE# to logic low and setting WE# to logic high (See Table 3). See Figure 4 for read memory timing diagram. The read operation from the host retrieves data from the array. The device remains enabled for read until another operation mode is accessed. During initial power-up, the device is in the read mode and is software data protected. The device must be unprotected to execute a write command.

The read operation of the 28LP040 is controlled by OE# at logic low and either CEL# and/or CEH# at logic low. When CEL# and CEH# are high, the chip is deselected and only standby power will be consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when both CEL# and CEH# are high or OE# is high.

Enable_Attribute Operation

Attribute memory is access by initiating the Enable_Attribute operation with a single command (88H). Read, Sector_Erase, and Byte Program operations can be performed in the attribute memory. The 1K byte of memory includes the PCMCIA attribute memory information. The REG# pin status has no effect on the operation. To return to common memory operations, a Reset command must be issued. The Reset command enables access to the common memory. (See Figure 8)

Read_ID operation

The Read_ID operation is initiated by writing a single command (99H). A read of address 0000H will output the manufacturer's code (BFH). A read of address 0001H will output the device code (11H). Any other valid command will terminate this operation.

Data Protection

In order to protect the integrity of nonvolatile data storage, the 28LP040 provides both hardware and software features to prevent inadvertent writes to the device, for example, during system power-up or power-down. Such provisions are described below.

Hardware Data Protection

The 28LP040 is designed with hardware features to prevent inadvertent writes. This is done in the following ways:

1. Write Inhibit Mode: OE# low, CEL# high, CEH# high, or WE# high will inhibit the write operation.
2. Noise/Glitch Protection: A WE# pulse width of less than 15 ns will not initiate a write cycle.
3. V_{CC} Power Up/Down Detection: The write operation is inhibited when V_{CC} is less than 2.5 V.
4. After power-down the device is in the read mode and the device is in the software data protect state.
5. The WP pin at V_{IH} will put the device in the Write Protect mode.

Software Data Protection (SDP)

The 28LP040 has software methods to further prevent inadvertent writes. In order to perform an erase or program operation, a two-step command sequence consisting of a set-up command followed by an execute command avoid inadvertent erasing and programming of the device.

The 28LP040 will default to software data protection after power up. A sequence of seven consecutive reads at specific addresses will unprotect the device The address sequence is 1823H, 1820H, 1822H, 0418H, 041BH, 0419H, 041AH. The address bus is latched on the rising

edge of OE# or CEL#, whichever occurs first. A similar seven read sequence of 1823H, 1820H, 1822H, 0418H, 041BH, 0419H, 040AH will protect the device. Also refer to Figures 10 and 11 for the 7 read cycle sequence Software Data Protection. The I/O pins can be in any state (i.e., high, low, or tristate).

Write Operation Status Detection

The 28LP040 provides three software means to detect the completion of a write cycle, in order to optimize the system write cycle time. The end of a write cycle (erase or program) can be detected by three means: 1) monitoring the Data# Polling bit; 2) monitoring the Toggle bit; or by two successive read of the same data. These three detection mechanisms are described below.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with the DQ used. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the write cycle, otherwise the rejection is valid.

Data# Polling (DQ_3, DQ_7)

The 28LP040 features Data# Polling to indicate the write operation status. During a write operation, any attempt to read the last byte loaded will receive the complement of the true data on DQ_3 and DQ_7. Once the write cycle is completed, DQ_3 for the low nibble and DQ_7 for the high nibble will show true data. The device is then ready for the next operation. See Figure 14 for Data Polling timing waveforms. In order for Data# Polling to function correctly, the byte being polled must be erased prior to programming.

Toggle Bit (DQ_2, DQ_6)

An alternative means for determining the write operation status is by monitoring the Toggle Bit, DQ_2 for the low nibble and DQ_6 for the high nibble. During a write operation, consecutive attempts to read data from the device will result in DQ_2 and DQ_6 toggling between logic 0 (low) and logic 1 (high). When the write cycle is completed, the toggling will stop. The device is then ready for the next operation. See Figure 15 for Toggle Bit timing waveforms.

Successive Reads

An alternative means for determining an end of a write cycle is by reading the same address for two consecutive data matches.

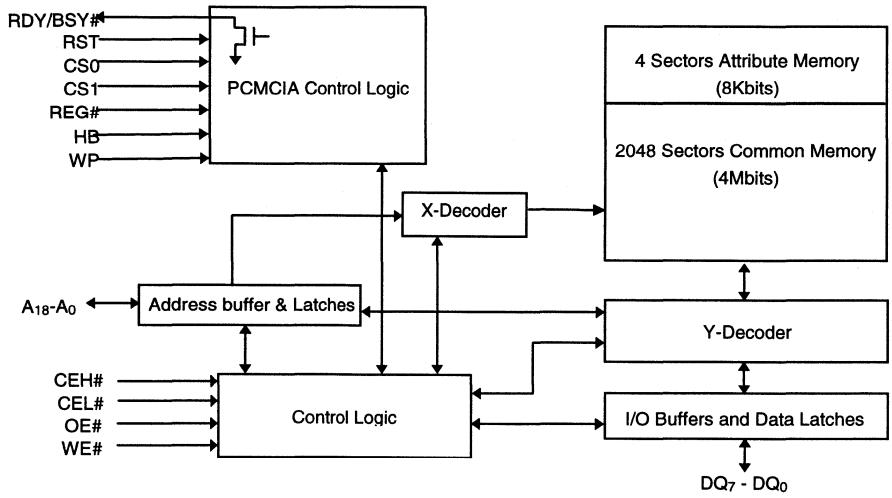


Figure 1: Functional Block Diagram of SST 28LP040

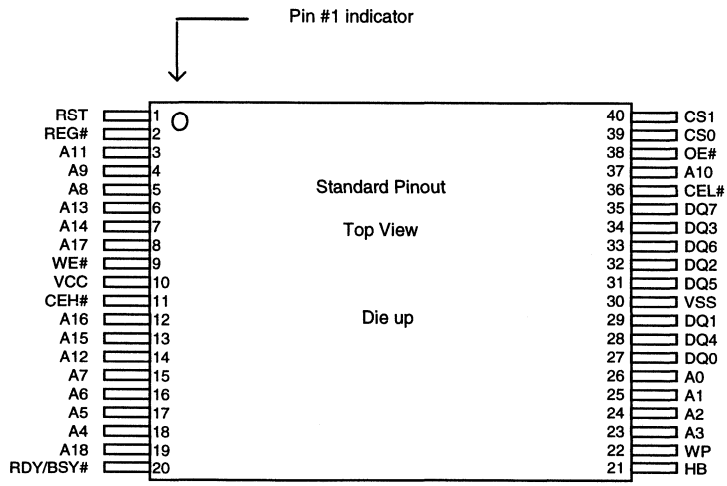


Figure 2: Standard Pin Assignments for 40-pin TSOP Packages.

Table 1: Pin Description

Symbol	Pin Name	Functions
A_{18}-A_8	Row Address Inputs	To provide memory addresses. Row addresses define a sector.
A_7-A_0	Column Address Inputs	Selects the byte within the sector.
DQ_7-DQ_0	Data Input/Output	To output data during read cycles and receive input data during write cycles. Data is internally latched during a write cycle. The outputs are in tri-state when OE#, CEL# or CEH# is high.
CEL#, CEH#	Chip Enable	To activate the device when CEL# or CEH# is low. (1) CEL# to enable the low nibble of DQ_0 to DQ_3 CEH# to enable the high nibble of DQ_4 to DQ_7
OE#	Output Enable	To gate the data output buffers. (1)
WE#	Write Enable	To control the write operations. (1)
Vcc	Power Supply	To provide 3.3-volt supply (± 0.3V)
Vss	Ground	
CS_0 - CS_1	Chip Selects	Preset chip selects used for memory pair select. (1) See Table 2A
HB	Half-Byte	Selects Odd/Even nibble for chip. (1)
WP	Write Protect	To activate write protect state. (1) When WP is high, the device becomes a ROM, acknowledging all read operation, and will ignore all operations attempting to alter memory array data. See Table 7.
RDY/BSY#	Read/Busy	This open-drain output requires a 1K pull-up resistor (minimum). (2) This pin is low to indicate the chip is busy internally. Any new instruction must be performed only when RDY/BSY# is high.
REG#	Attribute Memory	To switch from common memory to attribute memory. (1) There are 1Kbits of attribute memory in the 28LP040 decoded by A_9 to A_0. REG# can be overridden by the Enable_Attribute command.
RST	Reset	To reset the device after power-on. (1) RST must be asserted after power-up. After the falling edge of the RST pulse, the 28LP040 will be ready (RDY/BSY#) in ~ 10ms.

Note: (1) This pin is considered as an input for the purposes of the DC Operation Characteristics Table.

(2) This pin is considered as an output for the purposes of the DC Operation Characteristics Table.

Table 2: Operation Modes Selection

Mode	CEL#, CEH#	OE#	WE#	DQ	Address
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	A_{IN}
Byte Program	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}
Sector Erase	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}
Standby	V_{IH}	X	X	High Z	X
Write Inhibit	X	V_{IL}	X	High Z/ D_{OUT}	X
Write Inhibit	X	X	V_{IH}	High Z/ D_{OUT}	X
Software Chip Erase	V_{IL}	V_{IH}	V_{IL}	D_{IN}	See Table 7
Product Identification					
Hardware Mode	V_{IL}	V_{IL}	V_{IH}	Manufacturer Code (BF)	A_{18}-A_1=V_{IL}, A_9=V_H, A_0=V_{IL}
				Device Code (11)	A_{18}-A_1=V_{IL}, A_9=V_H, A_0=V_{IH}
Software Mode	V_{IL}	V_{IH}	V_{IL}		See Table 7
SDP Enable & Disable Mode	V_{IL}	V_{IH}	V_{IL}		See Table 7
Enable_Attribute	V_{IL}	V_{IH}	V_{IL}		See Table 7
Reset	V_{IL}	V_{IH}	V_{IL}		See Table 7

Table 2A: Card Decode Table

Device Part# Suffix	CS_1	CS_0
PCS00A	0	0
PCS01B	0	1
PCS10C	1	0
PCS11D	1	1

Note: The chip is selected by applying the listed logic levels to CS_0 and CS_1. The device part # suffix indicates the preset state.

Table 3: Main Memory Read Functions

Function Mode	REG#	CEH#	CEL#	HB	OE#	WE#	DQ_{7-4} (1)	DQ_{3-0} (2)	A_{18}-A_0 (3)
Standby Mode	X	H	H	X	X	X	High Z	High Z	X
Nibble Access (x4)	H	H	L	L	L	H	High Z	Even Nibble	A_{IN}
Nibble Access (x4)	H	H	L	H	L	H	High Z	Odd Nibble	A_{IN}
Byte Access (x8)	H	L	L	X	L	H	Odd Nibble	Even Nibble	A_{IN}
Odd Nibble Access	H	L	H	X	L	H	Odd Nibble	High Z	A_{IN}

Note: (1) D_{15}-D_8

(2) D_7-D_0

(3) A_{max}-A_1 for 1 Mbyte or higher density applications consisting of one or more pairs of 28LP040.

Table 4: Main Memory Write Functions

Function Mode	REG#	CEH#	CEL#	HB	OE#	WE#	DQ_{7-4}[1]	DQ_{3-0}[2]	A_{18}-A_0[3]
Standby Mode	X	H	H	X	X	X	X	X	X
Nibble Access (x4)	H	H	L	L	H	L	X	Even Nibble	A_{IN}
Nibble Access (x4)	H	H	L	H	H	L	X	Odd Nibble	A_{IN}
Byte Access (x8)	H	L	L	X	H	L	Odd Nibble	Even Nibble	A_{IN}
Odd Nibble Access	H	L	H	X	H	L	Odd Nibble	X	A_{IN}
Write Inhibit	X	X	X	X	L	X	X	X	X

Note: [1]D_{15}-D_8

[2]D_7-D_0

[3]A_{max}-A_1 for 1 Mbyte or higher density applications consisting of one or more pairs of 28LP040

Table 5: Attribute Memory Read Functions

Function Mode	REG#	CEH#	CEL#	HB	OE#	WE#	DQ_{7-4}[1]	DQ_{3-0}[2]	A_9-A_0[3]
Standby Mode	X	H	H	X	X	X	High Z	High Z	X
Nibble Access (x4)	L	H	L	L	L	H	High Z	Even Nibble	A_{IN}
Nibble Access (x4)	L	H	L	H	L	H	High Z	Odd Nibble	A_{IN}
Byte Access (x8)	L	L	L	X	L	H	Odd Nibble	Even Nibble	A_{IN}
Odd Nibble Access	L	L	H	X	L	H	Odd Nibble	High Z	A_{IN}

Note: [1]D_{15}-D_8

[2]D_7-D_0 for 1 Mbyte or higher density applications consisting of one or more pairs of 28LP040

[3]Other addresses are "don't care"

Table 6: Attribute Memory Write Functions

Function Mode	REG#	CEH#	CEL#	HB	OE#	WE#	DQ_{7-4}[1]	DQ_{3-0}[2]	A_9-A_0
Standby Mode	X	H	H	X	X	X	X	X	X
Nibble Access (x4)	L	H	L	L	H	L	X	Even Nibble	A_{IN}
Nibble Access (x4)	L	H	L	H	H	L	X	Odd Nibble	A_{IN}
Byte Access (x8)	L	L	L	X	H	L	Odd Nibble	Even Nibble	A_{IN}
Odd Nibble Access	L	L	H	X	H	L	Odd Nibble	X	A_{IN}
Write Inhibit	X	X	X	X	L	X	X	X	X

Note: [1]D_{15}-D_8

[2]D_7-D_0; for 1 Mbyte or higher density applications consisting of one or more pairs of 28LP040

[3]Other addresses are "don't care"

Table 7: Software Command Summary

Command Summary	Required Cycle(s)	Setup Command Cycle			Execute Command Cycle			WP[6]	SDP[6]
		Type[1]	Addr[2,3]	Data[4]	Type[1]	Addr[2,3]	Data[4]		
Sector_Erase	2	W	X	22H	W	SA	DDH	N	N
Byte_Program	2	W	X	11H	W	PA	PD	N	N
Erase_Verify	2	W	VA[5]	AAH	R	X	D_{OUT}	Y	Y
Reset	1	W	X	FFH				Y	Y
Enable_Attribute	1	W	X	88H				Y	Y
Read_ID	3	W	X	99H	R	(9)	(9)	Y	Y
Software_Data_Protect	7	R	(7)						
Software_Data_Unprotect	7	R	(8)						

Notes:

1. Type definition: W = Write, R = Read, X= don't care
2. Addr (Address) definition: SA = Sector Address = A_{18} - A_8, sector size = 512 nibbles; A_7- A_0 = X for this command.
3. Addr (Address) definition: PA = Program Address = A_{18} - A_0.
4. Data definition: PD = Program Data, H = number in hex.
5. Addr (Address) definition: VA = Verify Address = A_{18} - A_0.
6. WP = Hardware Write Protect mode using WP pin, SDP = Software Data Protect mode using 7 Read Cycle Sequence.
   a) Y = the operation can be executed with protection enabled
   b) N = the operation cannot be executed with protection enabled
7. Refer to Figure 13 for the 7 Read Cycle sequence for Software_Data_Protect.
8. Refer to Figure 12 for the 7 Read Cycle sequence for Software_Data_Unprotect.
9. Address 0000H retrieves the manufacturer' code of BFH and address 0001H retrieves the device code of 11H.

Table 8: Memory Array Detail

Memory Array	Sector Select	Byte Select	Nibble Select
Common Memory	A_{18} - A_8	A_7 - A_0	HB
Attribute Memory	A_9 - A_8	A_7 - A_0	HB

Table 9: Nonconforming Sector Map

Attribute Byte Address	D7	D6	D5	D4	D3	D2	D1	D0	Attribute Byte Address	D7	D6	D5	D4	D3	D2	D1	D0
200	X	X	X	X	SNS SUM [3:0]				300	X	X	X	X	SNS SUM [3:0]			
201	X	X	X	X	SNS SUM [7:4]				301	X	X	X	X	SNS SUM [7:4]			
202	X	X	X	X	16	14	12	10	302	X	X	X	X	17	15	13	11
203	X	X	X	X	1E	1C	1A	18	303	X	X	X	X	1F	1D	1B	19
.	X	X	X	X					.	X	X	X	X				
.	X	X	X	X					.	X	X	X	X				
.	X	X	X	X					.	X	X	X	X				
.	X	X	X	X					.	X	X	X	X				
2FE	X	X	X	X	7F6	7F4	7F2	7F0	3FE	X	X	X	X	7F7	7F5	7F3	7F1
2FF	X	X	X	X	7FE	7FC	7FA	7F8	3FF	X	X	X	X	7FF	7FD	7FB	7F9

Notes: The Attribute memory bit is "0" when the corresponding Common memory sector is nonconforming. The first 8 sectors of Common memory are always conforming.

Definitions:

1. The SNS sum is the sum of the number of nonconforming sectors and is calculated by summing the "0"s in the remaining bytes of the nonconforming sector map.
2. SNS Sum = Sum of Nonconforming Sector sum. The byte data from these addresses are not included in the sum.
   a) [3:0] = The lower nibble of the SNS sum.
   b) [7:4] = The higher nibble of the SNS sum.
3. Only the lower nibble is used in the attribute memory to map the location of the nonconforming sector(s).

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential ..... -0.5V to V_{CC}+ 0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential ..... -1.0V to V_{CC}+ 1.0V
Voltage on A_9 Pin to Ground Potential ..... -0.5V to 14.0V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Surface Mount Lead Soldering Temperature (3 Seconds) ..... 240°C
Output Short Circuit Current[1] ..... 100 mA

Note: [1] Outputs shorted for no more than one second. No more than one output shorted at a time.

Table 10: Operating Range

Range	Ambient Temp	V_{CC}
Commercial	0 °C to +70 °C	3.0V to 3.6V

Table 11: AC Conditions of Test

Input Rise/Fall Time.....10 ns
Output Load.....1 TTL Gate and C_L = 100 pF
See Figures 16 and 17

Table 12: DC Operating Characteristics

Symbol	Parameter	Limits		Units	Test Conditions
		Min	Max		
I_{CC}	Power Supply Current				CE# (L or H) = OE# =V_{IL}, WE# =V_{IH}, all I/Os open
	Read		10	mA	Address input = V_{IL}/V_{IH}, at f=1/T_{RC} Min. V_{CC} = V_{CC} Max
	Program and Erase		25	mA	CE# (L or H) =WE# =V_{IL}, OE# =V_{IH} V_{CC} =V_{CC} Max.
I_{SB1}	Standby V_{CC} Current (TTL input)		1	mA	CE# =OE# =WE# = V_{IH}, V_{CC}=V_{CC} Max
I_{SB2}	Standby V_{CC} Current (CMOS input)		20	µA	CE# = OE# = WE# = V_{CC} -0.3V, V_{CC}=V_{CC} Max
I_{LI}	Input Leakage Current		1	µA	V_{IN} = GND to V_{CC}, V_{CC} = V_{CC} Max.
I_{LO}	Output Leakage Current		10	µA	V_{OUT} =GND to V_{CC}, V_{CC} = V_{CC} Max.
V_{IL}	Input Low Voltage		0.8	V	V_{CC} = V_{CC} Max.
V_{IH}	Input High Voltage	2.0		V	V_{CC} = V_{CC} Max.
V_{IL2}	Input Low Voltage, CMOS		0.2	V	V_{CC} = V_{CC} Max.
V_{IH2}	Input High Voltage, CMOS	$V_{CC-0.2}$		V	V_{CC} = V_{CC} Max.
V_{OL}	Output Low Voltage		0.4	V	I_{OL}= 3.2 mA, V_{CC} = V_{CC} Min.
V_{OH}	Output High Voltage	2.4		V	I_{OH} = 2.0 mA, V_{CC} = V_{CC} Min.
V_H	Supervoltage for A_9	11.6	12.4	V	CE#=OE#=V_{IL}, WE#=V_{IH}
I_H	Supervoltage Current for A_9		200	µA	CE#=OE#=V_{IL},WE#=V_{IH} , A_9 = V_H Max.

Table 13: Power-up Timings

Symbol	Parameter	Maximum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	10	ms
$T_{PU-WRITE}$[1]	Power-up to Write Operation	10	ms

Table 14: Capacitance (Ta = 25 °C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0v	6 pF

Note: [1]This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 15: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}	Endurance	100,000	Cycles	MIL-STD-883, Method 1033
T_{DR}[1]	Data Retention	100	Years	MIL-STD-883, Method 1008
V_{ZAP_HBM}[1]	ESD Susceptibility Human Body Model	1000	Volts	MIL-STD-883, Method 3015
V_{ZAP_MM}[1]	ESD Susceptibility Machine Model	200	Volts	JEDEC
I_{LTH}[1]	Latch Up	100	mA	JEDEC Standard 17

Note: [1]This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

AC Characteristics

Table 16: Read Cycle Timing Parameters

PCMCIA Symbol	IEEE Symbol	Industry Symbol	Parameter	28LP040-250 Min	28LP040-250 Max	Units
tCR	tAVAV	T_{RC}	Read Cycle time	250		ns
ta(A)	tAVQV	T_{AA}	Address Access Time		250	ns
ta(CE)	tELQV	T_{CE}	Chip Enable Access Time		250	ns
ta(OE)	tGLQV	T_{OE}	Output Enable Access Time		100	ns
tdis(CE)	tEHQZ	T_{CLZ}[1]	CE# Low to Active Output	0		ns
tdis(OE)	tGHQZ	T_{OLZ}[1]	OE# Low to Active Output	0		ns
ten(CE)	tELQX	T_{CHZ}[1]	OE# High to High-Z Output		75	ns
ten(OE)	tGLQX	T_{OHZ}[1]	OE# High to High-Z Output		75	ns
tv(A)	tAXQX	T_{OH}[1]	Output Hold from Address Change	0		ns

Table 17: Erase/Program Cycle Timing Parameters

PCMCIA Symbol	IEEE Symbol	Industrial Symbol	Parameter	28LP040-250 Min	28LP040-250 Max	Units
tCW	tAVA	T_{BP}	Byte Program Cycle Time		35	µs
tw(WE)	tWLWH	T_{WP}	Write Pulse Width (WE#)	160		ns
tsu(A)	tAVWL	T_{AS}	Address Setup Time	10		ns
th(a)	tWLAX	T_{AH}	Address Hold Time	100		ns
tsu(CE)	tELWL	T_{CS}	CE# Setup Time	0		ns
th(CE)	tWHEX	T_{CH}	CE# Hold Time	0		ns
tsu(OE-WE)	tGHWL	T_{OES}	OE# High Setup Time	20		ns
th(OE-WE)	tWGL	T_{OEH}	OE# High Hold Time	20		ns
tw(CE)	tWLEH	T_{CP}	Write Pulse Width (CE#)	160		ns
tsu(D-WEH)	tDVWH	T_{DS}	Data Setup Time	120		ns
th(D)	tWHDX	T_{DH}	Data Hold Time	20		ns
	tWHWL2	T_{SE}	Sector Erase Cycle Time		2	ms
		T_{RST}[1]	Reset Command Recovery Time		4	µs
		T_{EVD}	Erase Verify Timing Delay	.025		µs
		T_{ERD}	Erase Reset Timing Delay	4		µs
		T_{ASE}	Algorithmic Sector Erase Cycle Time	0.04	2.56	ms
	tEHEL	T_{CPH}	CE# High Pulse Width	50		ns
	tWHWL1	T_{WPH}	WE# High Pulse Width	50		ns
	tRHRL	T_{HR}[1]	Hardware Reset Pulse Width	10		µs
	tRHBL	T_{RBS}[1]	Hardware Reset High to RDY/BSY# Active	10		µs
		T_{PCP}[1]	Protect Chip Enable Pulse Width	20		ns
		T_{PCH}[1]	Protect Chip Enable High Time	20		ns
		T_{PAS}[1]	Protect Address Setup Time	0		ns
		T_{PAH}[1]	Protect Address Hold Time	100		ns

Note: [1]This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.

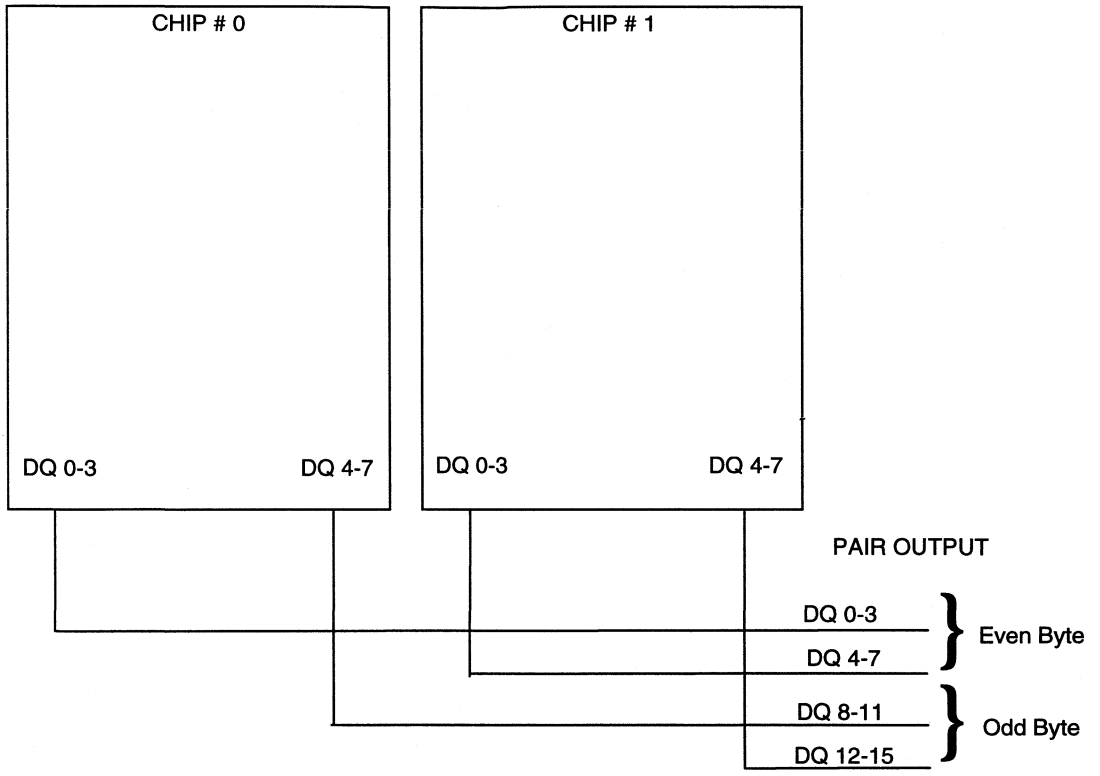


Figure 3: Chip Pair Mapping (Nibble Access)

Table 18: Nibble Access Table

Byte	Nibble	Outputs	CEL#	CEH#	HB
Even	Even Nibble	0-3	L	H	L
Even	Odd Nibble	4-7	L	H	H
Odd	Even Nibble	8-11	H	L	L
Odd	Odd Nibble	12-15	H	L	H

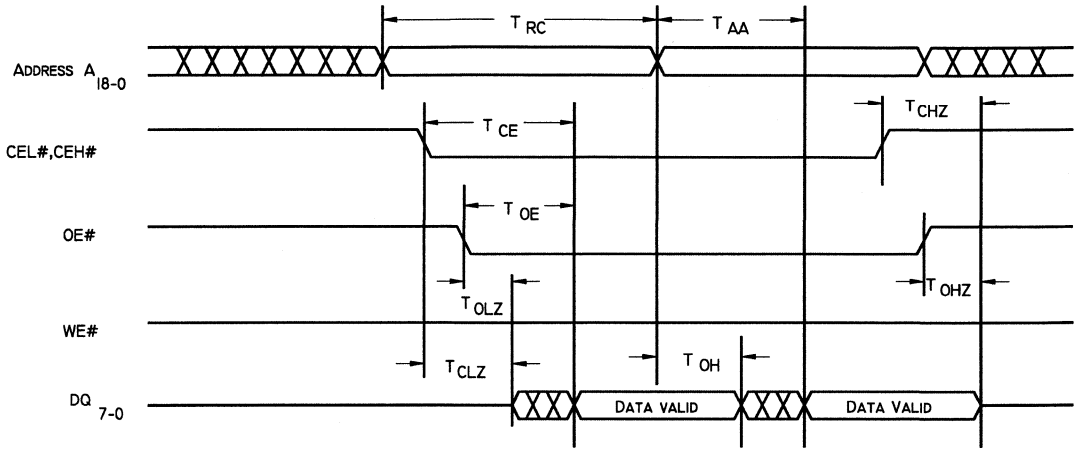


Figure 4: Read Cycle Timing Diagram

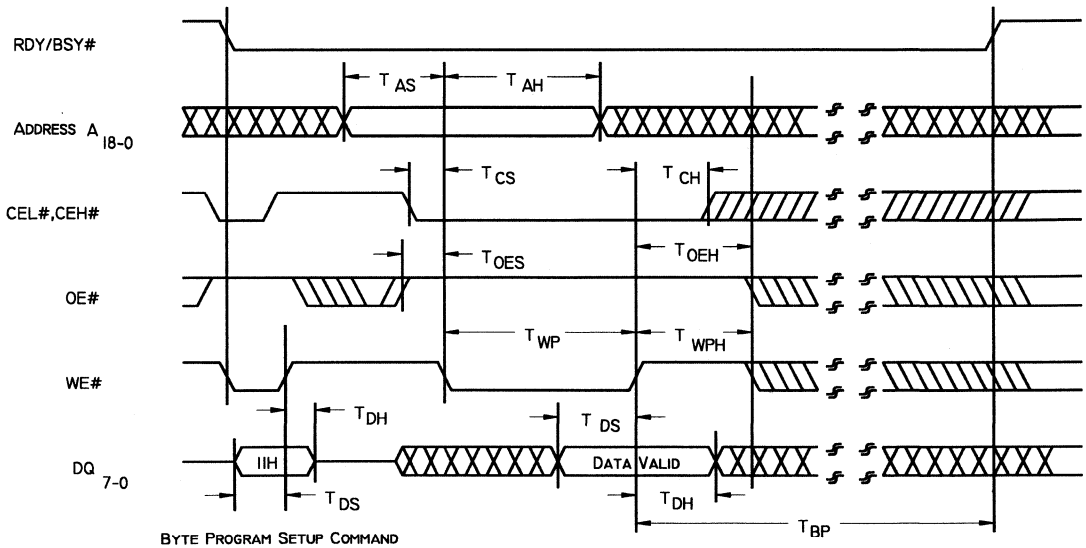


Figure 5: WE# Controlled Byte Program Timing Diagram

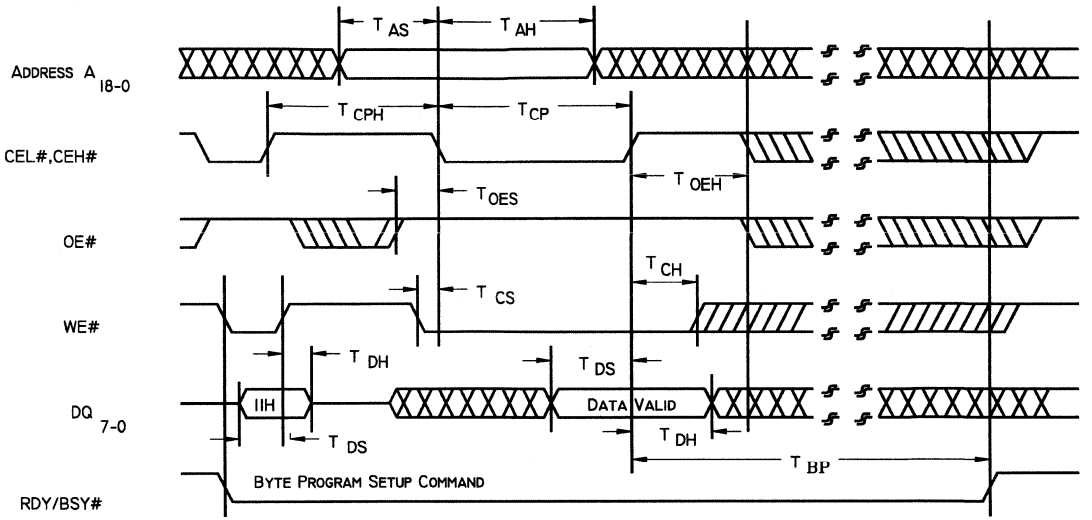


Figure 6: CE# Controlled Byte Program Timing Diagram

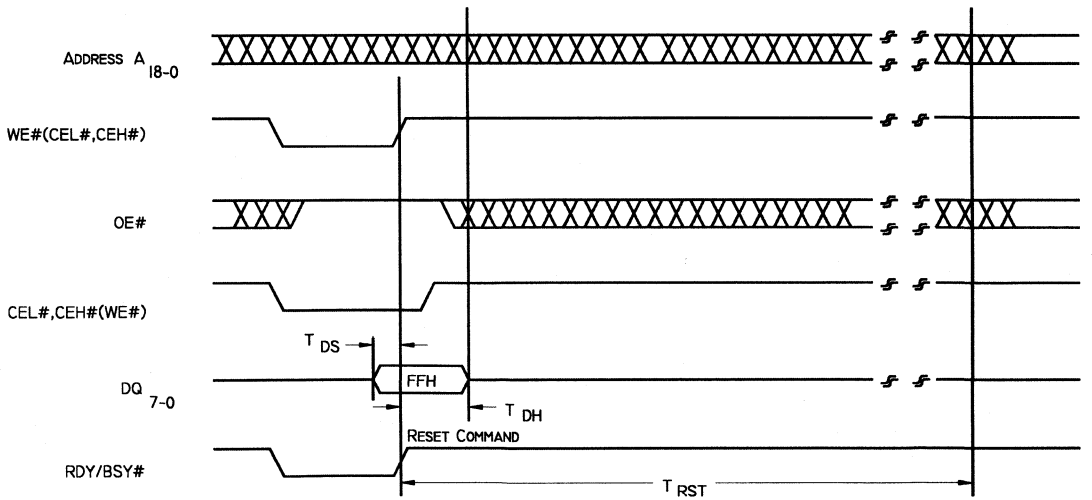
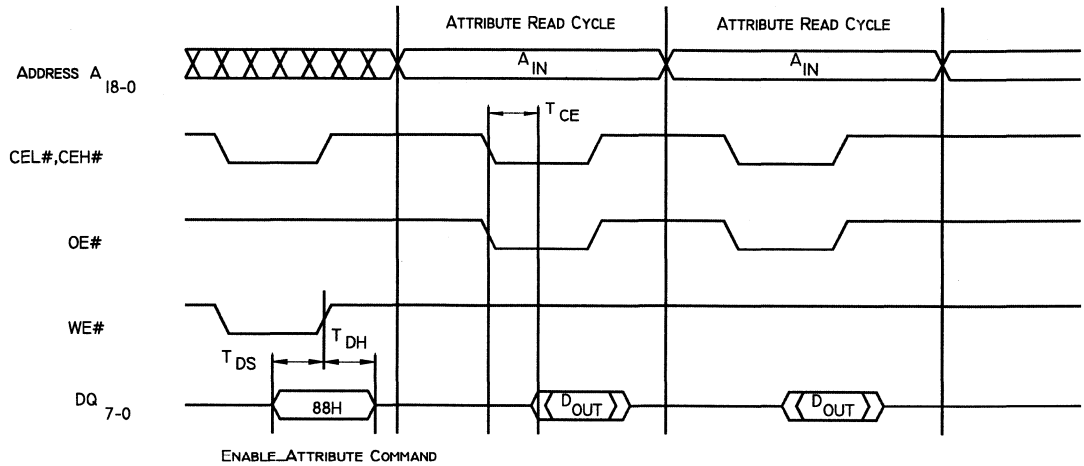


Figure 7: Reset Command Timing Diagram



1) READ, SECTOR_ERASE, BYTE_PROGRAM OPERATIONS CAN BE PERFORMED AT THIS TIME. THE READ OPERATION IS INTENDED AS AN EXAMPLE FOR THIS TIMING DIAGRAM ONLY.

Figure 8: Enable_Attribute Timing Diagram

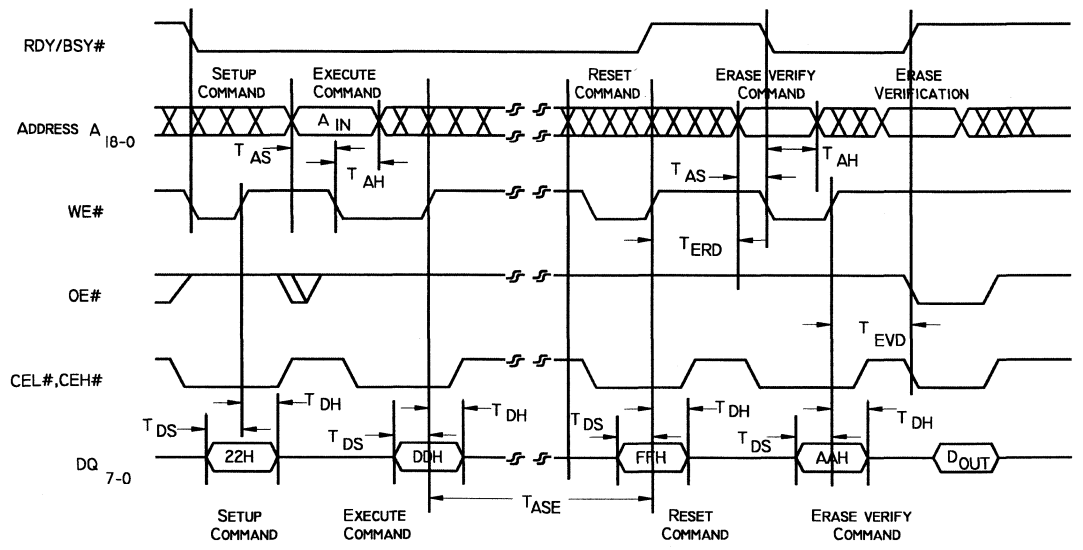
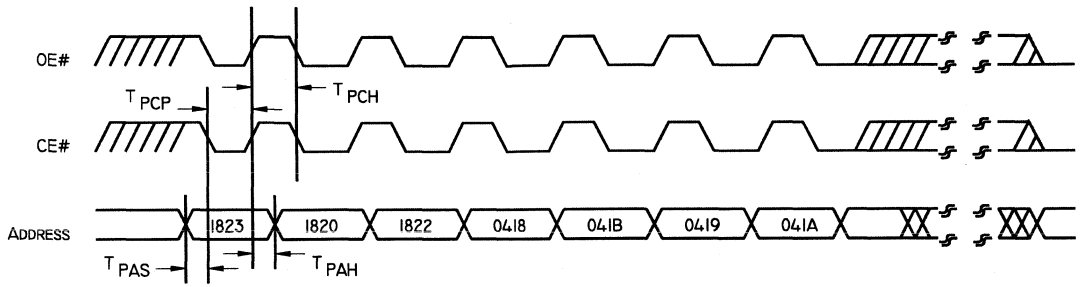


Figure 9: Sector Erase Timing Diagram



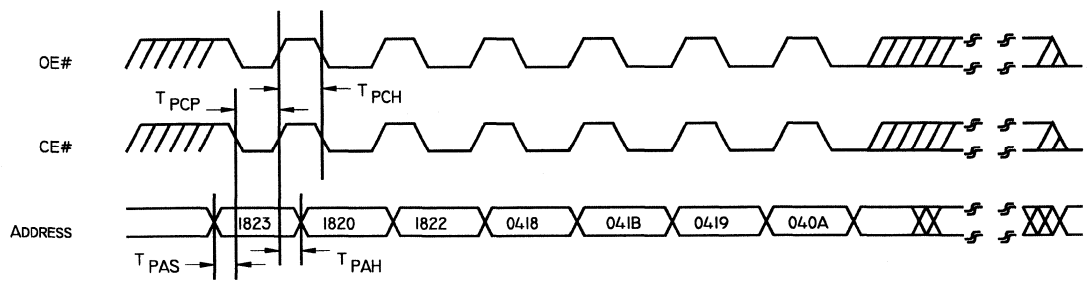
NOTE : A. ADDRESSES ARE LATCHED INTERNALLY ON THE RISING EDGE OF:

1. OE# IF CE# IS KEPT AT LOW ALL TIME.
2. CE# IF OE# IS KEPT AT LOW ALL TIME.
3. THE FIRST PIN TO GO HIGH IF BOTH ARE TOGGLED.

B. ABOVE ADDRESS VALUES ARE IN HEX.

C. ADDRESSES > A_{12} ARE "DON'T CARE"

Figure 10: Software Data Unprotect Timing Diagram



NOTE : A. ADDRESSES ARE LATCHED INTERNALLY ON THE RISING EDGE OF:

1. OE# IF CE# IS KEPT AT LOW ALL TIME.
2. CE# IF OE# IS KEPT AT LOW ALL TIME.
3. THE FIRST PIN TO GO HIGH IF BOTH ARE TOGGLED.

B. ABOVE ADDRESS VALUES ARE IN HEX.

C. ADDRESSES > A_{12} ARE "DON'T CARE"

Figure 11: Software Data Protect Timing Diagram

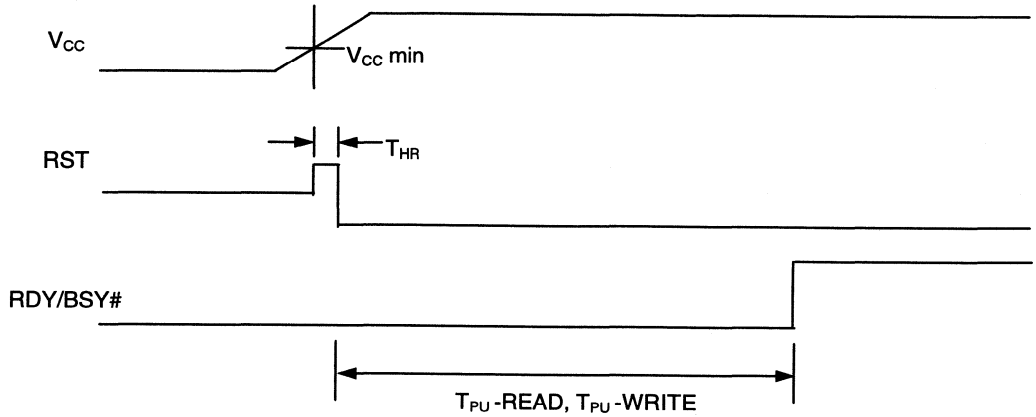


Figure 12: RST and RDY/BSY# waveforms - Power up to Read and Write

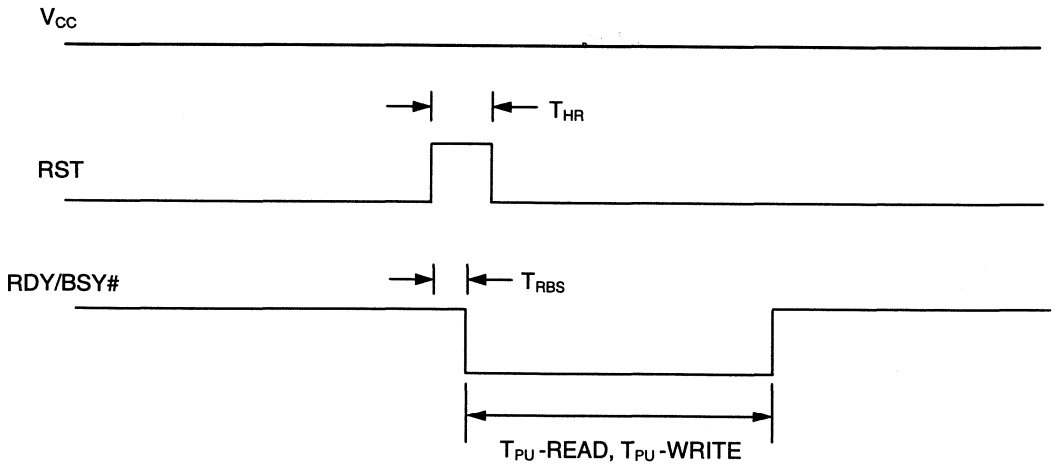
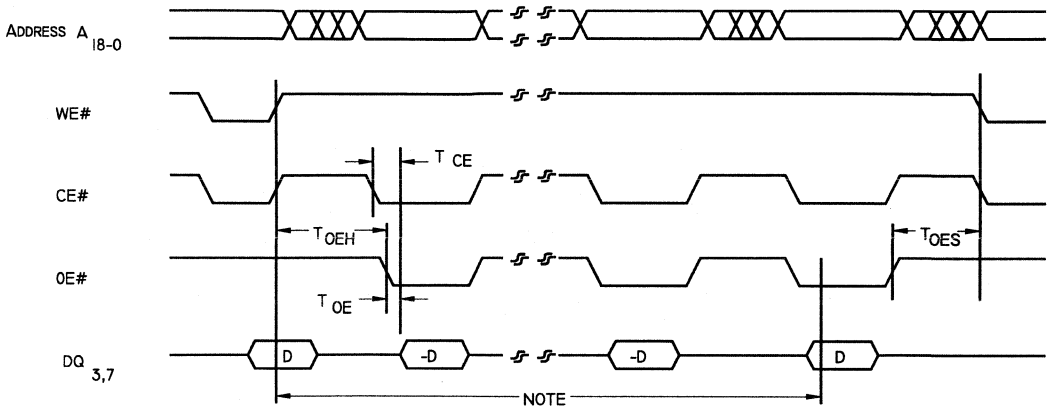
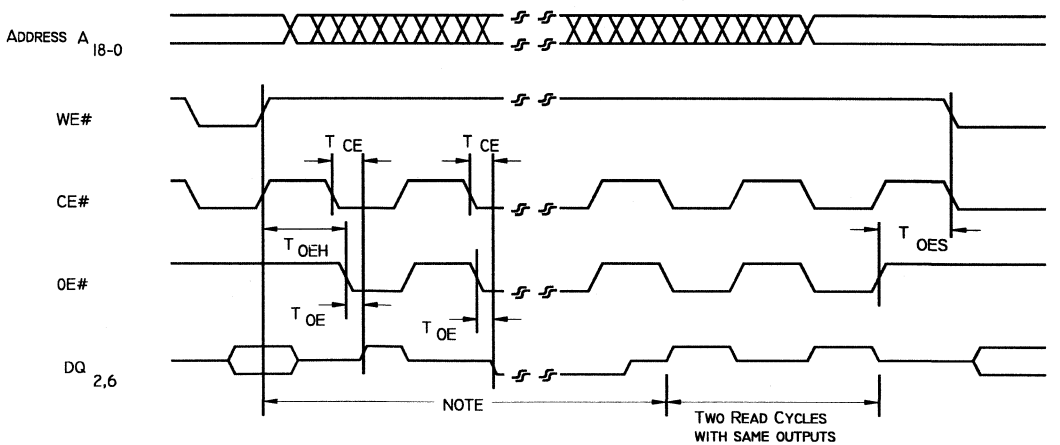


Figure 13: RST and RDY/BSY# waveforms - Hardware Reset



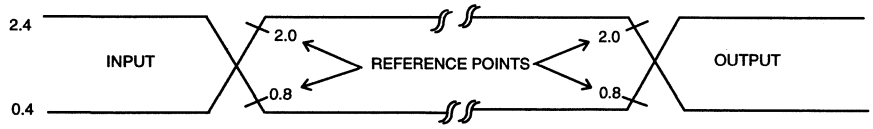
NOTE: THIS TIME INTERVAL SIGNAL CAN BE T_{SE} OR T_{BP}, DEPENDING UPON THE SELECTED OPERATION MODE.

Figure 14: Data# Polling Timing Diagram



NOTE: THIS TIME INTERVAL SIGNAL CAN BE T_{SE} OR T_{BP}, DEPENDING UPON THE SELECTED OPERATION MODE.

Figure 15: Toggle Bit Timing Diagram



AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a logic "1" and V_{OL} (0.4 V_{TTL}) for a logic "0". Measurement reference points for inputs and outputs are V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Inputs rise and fall times (10% ↔ 90%) are <10 ns.

Figure 16: AC Input/Output Reference Waveform

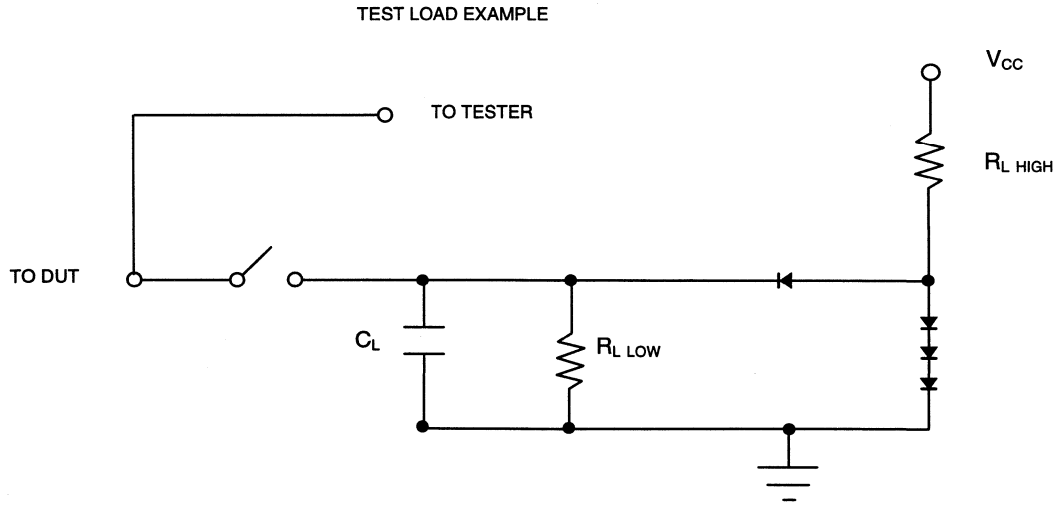


Figure 17: Test Load Example

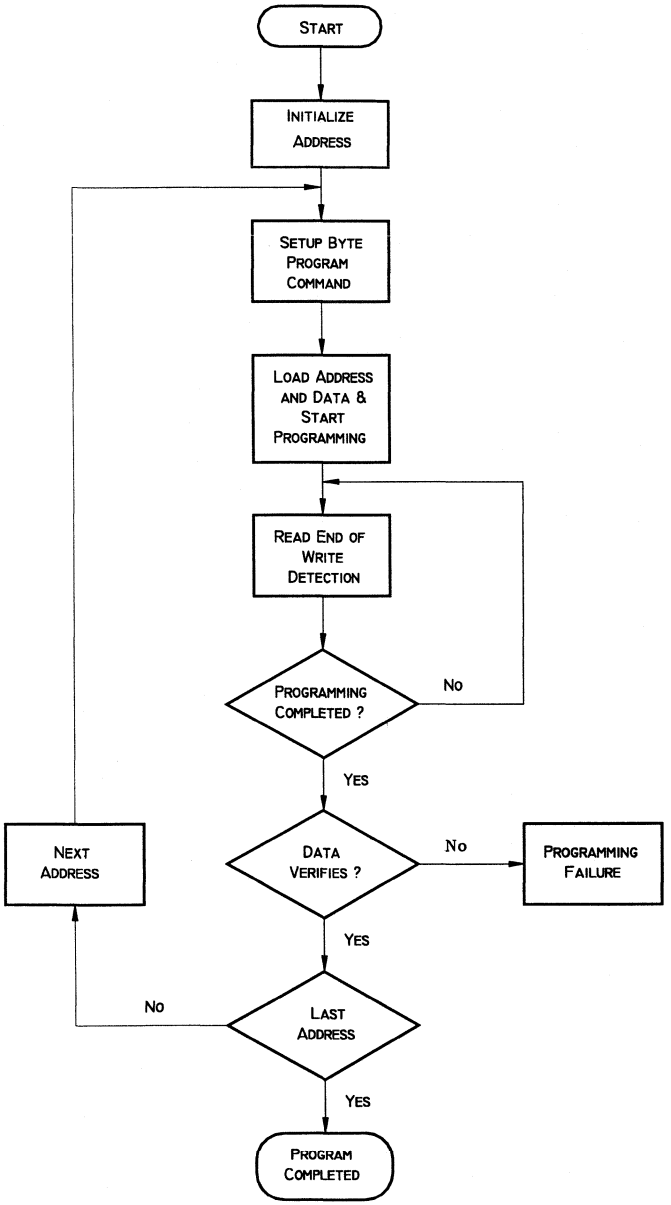


Figure 18: Byte Program Flowchart

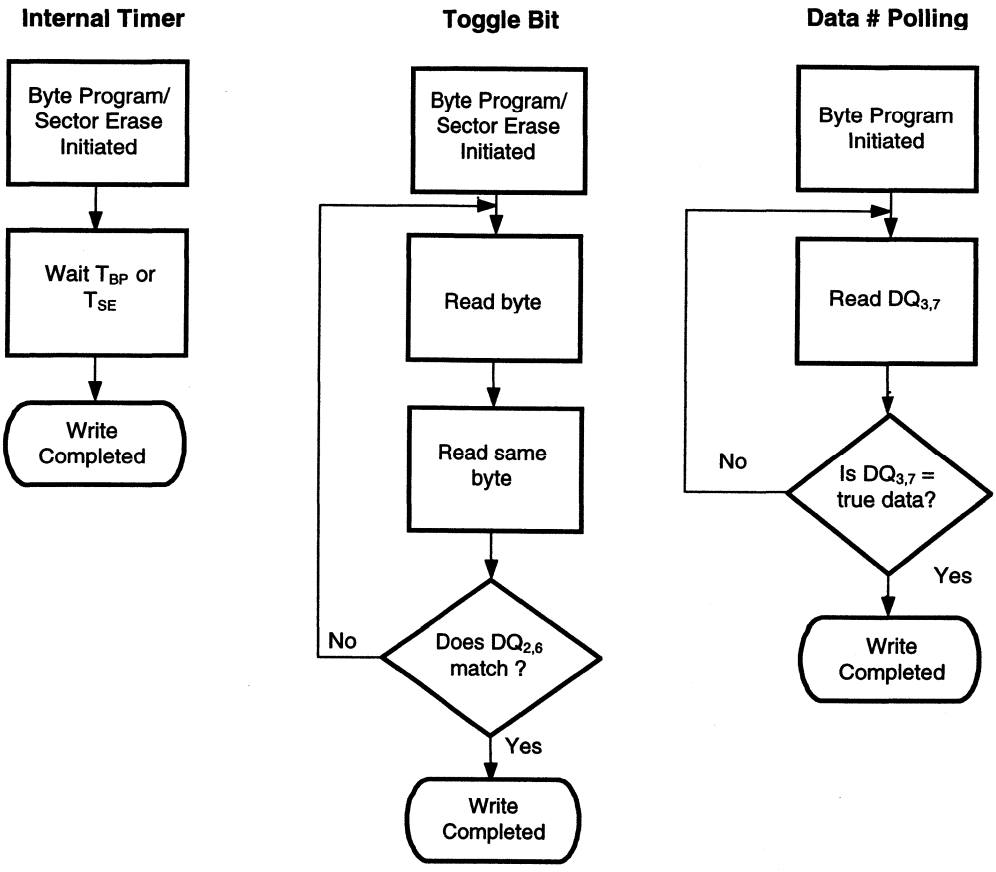


Figure 19: Write Wait Options

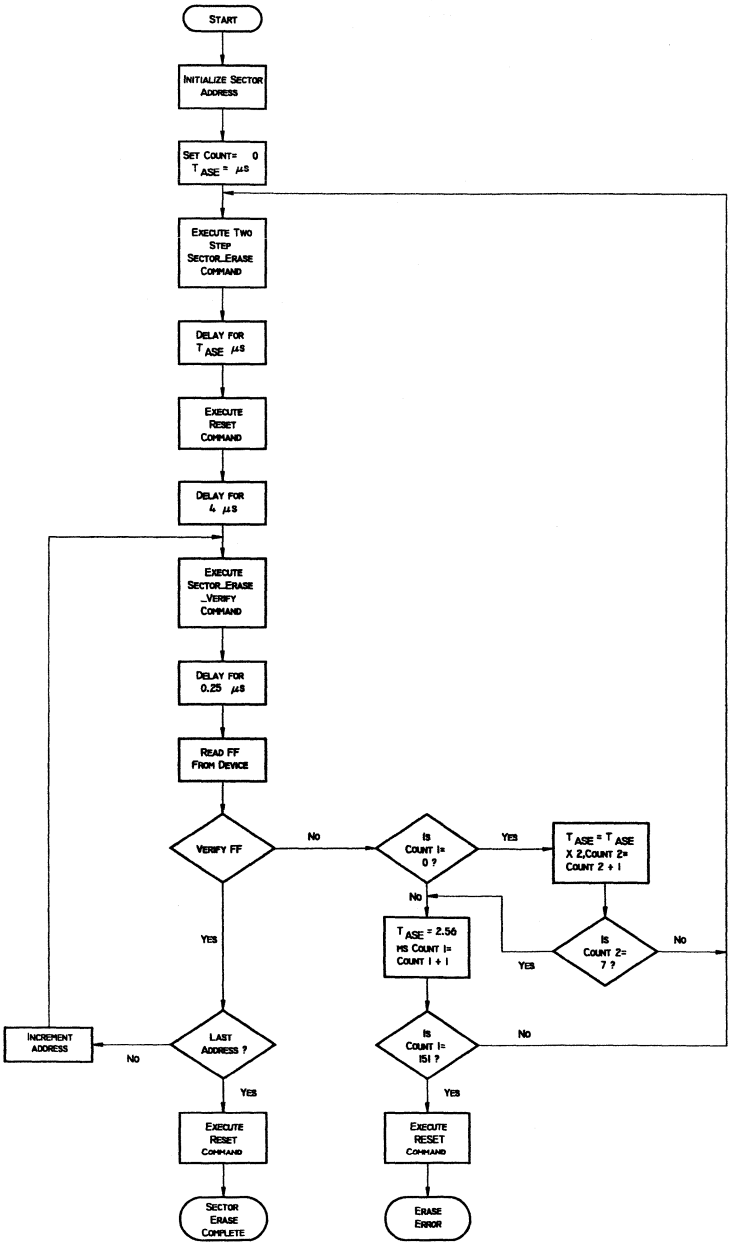


Figure 20: Sector_Erase Flowchart

Product Ordering Information

Device **Speed** **Suffix1** **Suffix2** **Suffix3**

SST28LP040 - XXX - XX - XX XXXX

Card Decode
S00A = PCS00A
S01B = PCS01B
S10C = PCS10C
S11D = PCS11D

Package Modifier
I = 40 leads

Package Type
W = TSOP (die up)

Operating Temperature
C = Commercial = 0° to 70°C

Minimum Endurance
5 = 100,000 cycles

Read Access Speed
250 = 250 ns

Valid combinations

SST28LP040-250-5C-WI-S00A SST28LP040-250-5C-WI-S01B

SST28LP040-250-5C-WI-S10C SST28LP040-250-5C-WI-S11D

Example: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Die Sales Specifications

July 1996

Die Sales Specifications

Introduction to Unecapsulated Die

This document provides the user with guidelines for process, testing, and applications issues associated with purchasing unencapsulated SST flash EEPROM die. Product electrical specification, functional descriptions, and bonding diagrams are not included. This information is available in the appropiate sections of SST's data book or directly from SST.

This guide provides recommendations for die attach and wire bonding methods. Typicals for die thickness, topside glassivation composition and thickness, and metalization glassivation composition and thickness are included. Application information covering some application issues encountered when using SST flash EEPROM die is provided.

Properly package die will perform according to the functional, timing, and parametric parameters listed in the device data sheet. Procedures to demonstrate conformace to these specifications should be established contractually with SST on an individual basis.

Standard Die Sales Guidelines

Reliability Expectations:

1. Endurance/Data Retention: Same as packaged units.
2. Life Test: Same as packaged units.

Guarantees:

1. Endurance/Data Retention: 5%AOQL
2. 1% AOQL for Industy Standard Commercial Visual criteria for die
3. Packing/Shipping per "Standard Die Packing" section.

Correlated Yields:

1. Expect inital yields while doing correlation to be: >75%.
2. After correlation, yields should be >95%.
3. SST performs a sort-bake-sort for endurance and data retention infant mortality screening. Sort includes parametric, functional and timing tests.

Test Modes:

SST uses control fuses for various built-in test modes and other functions within the device. Exposure to UV light or misapplication of high voltages can erase or program the fuses, causing loss of functionality. Control fuses are used for redundancy repair to improve manufacturing yield and for chip functions to reduce test time.

Standard Die Packing

All die shipped by SST are packed per the following:

1. The die are placed in a StatPro-150 "waffle pack" with a cavity of proper size to restrict movement and prevent die orientation change.
2. An antistatic lint-free paper insert is placed over the die. The waffle pack StatPro-150 lid is placed on top and secured with StatPro-150 locking clips.
3. A set of waffle packs (as required) are stacked and vacuum sealed in a bag.
4. A label with the SST logo, lot number, quantity, part number, and packing date is placed on the waffle pack bag.
5. Die do not require cleaning prior to assembly.

General Die Specification

1. Thickness: 330 to 510 µ (13 to 20 mils).
2. X-Y Dimensions: Per each device. Several are provided in the following pages. Please contact SST for devices not shown.
3. Top Glassivation: Varies according to device and wafer fabrication location. Typically 1 µ thick, SiN (silicon nitride) on top PSG.
4. Metallizations: Varies according to device and wafer fabrication location. Typically 1 µ thick Al/Si/Cu (98.9/1.0/0.1)
5. Actual die count variance shall be less than ± 1%.

Suggested Assembly Flow and Conditions

Operation	Condition
Receiving Inspection	Documentation check Visual-1% AOQL
	Mechanism, Functional-2.5% AOQL
Die Attach	Use conductive epoxy with vendor recommended cure profile
Visual	As appropiate
Wire Bond	Gold wire-1.3 mil, Thermosonic Ball bond at 200°C
Visual	As appropiate
Encapsulation	Low Stress Moisture Resistant Molding Compound
Cure	Per vendor recommended cure profile
Final Electrical Test	Timing, Parametric and Functional at Operating Temperatures.

Notes:

1. Final electrical test yields may vary with device data sheet performance limits (e.g., access time, temperature range, V_{CC} range
2. Final electrical test yield expectations do not include yield loss associated with assembly.
3. Correlation includes tester, hardware, test program, and test methods.

Application Information

SST recommends the following power up/power down sequences:

Power up sequence:

1. All addresses and data lines to 0 volts.
2. Output Enable (OE#) to 0 volts.
3. Chip Enable (CE#) and Write Enable (WE#) to 3 volts or TTL high.
4. V_{CC} to Supply Value.
5. Output Enable (OE#) to high.

Power down sequence:

1. All addresses and data lines to 0 volts.
2. Output Enable (OE#) to 0 volts.
3. Chip Enable (CE#) and Write Enable (WE#) to 3 volts or TTL high.
4. V_{CC} to 0 volts.
5. Chip Enable (CE#) and Write Enable (WE#) to 0 volts.

Software Data Protection (SDP)

All SST devices provide a software data protection (SDP) features. When enabled, this feature prevents write operations through software, by accessing an internal register. Software Data Protect can reduce the possibility of inadvertent writes resulting from power up, power down, or momentary power disturbances. Consult the device specification in the SST data book on use of this feature.

Signal lines above V_{CC}

SST. devices incorporate built-in test modes to aid in testing of devices functions. These test modes are accessed by taking one or more device pins above the maximum input level to enable the mode. Although unlikely, a noise "spike" of sufficient duration and amplitude can enable a test mode. If this occurs, device operations mat be changed. The device may be reset by turning power offf, however in some cases a change to the functionality occurs. Consult SST for recommended preventative measures and recovery techniques.

Substrate Grounding

All SST devices require a substrate ground connection for proper operations. If the V_{SS} die attach pad is not grounded or has a high resistance path to ground, the device timing or functionality performance may be affected.

Effects of UV Light or X-Rays

EEPROM cells are used as control fuses to select or modify various internal device functions. If die are exposed to UV (Ultra-Violet) light or X-Rays of sufficient intensity and duration, these cells could be erased. This erasing is the same mechanism as used by UV-EPROMs an is nondestructive, but could cause a change in the functinality of the device. Consult SST for recommended preventative measures and recovery techniques.

29EE512 Pad Coordinates

Die Size: 154" x 152" = 3.91 mm x 3.86 mm

Pin Name	X (Center)	Y (Center)
A15	1296	3502
A12	582	3565
A7	405	3565
A6	193	3552
A5	193	3312
A4	193	3134
A3	152	566
A2	152	352
A1	152	175
A0	483	157
DQ0	743	163
DQ1	1054	163
DQ2	1334	163
VSS	1592	177
VSS	1815	179
DQ3	2154	163
DQ4	2433	163
DQ5	2744	163
DQ6	3024	163
DQ7	3335	163
CE#	3605	228
A10	3605	480
OE#	3605	657
A11	3605	3085
A9	3605	3325
A8	3605	3502
A13	3393	3502
A14	2881	3502
WE#	2407	3502
V_{CC}	2085	3502
V_{CC}	1871	3525

29EE010 Pad Coordinates

Die Size: 154" x 206" = 3.91 mm x 5.23 mm

Pin Name	X (Center)	Y (Center)
A16	1473	4864
A15	1296	4864
A12	582	4927
A7	405	4927
A6	193	4913
A5	193	4673
A4	193	4496
A3	152	566
A2	152	352
A1	152	175
A0	483	157
DQ0	743	163
DQ1	1054	163
DQ2	1334	163
VSS	1592	177
VSS	1815	179
DQ3	2154	163
DQ4	2433	163
DQ5	2744	163
DQ6	3024	163
DQ7	3335	163
CE#	3605	228
A10	3605	480
OE#	3605	657
A11	3605	4446
A9	3605	4687
A8	3605	4864
A13	3393	4864
A14	2881	4864
WE#	2407	4864
V_{CC}	2085	4864
V_{CC}	1871	4887

The coordinates are in microns measured from the bottom left corner of the die edge.
The V_{SS} pin is the double pad on the bottom.

29EE020 Pad Coordinates

Die Size: 151" x 306" = 3.85 mm x 7.78 mm

Pin Name	X (Center)	Y (Center)
A16	1412	7410
A15	1235	7410
A12	521	7473
A7	343	7473
A6	131	7459
A5	131	7219
A4	131	7042
A3	152	563
A2	152	350
A1	152	172
A0	421	154
DQ0	682	160
DQ1	993	160
DQ2	1273	160
VSS	1530	174
VSS	1753	176
DQ3	2092	160
DQ4	2372	160
DQ5	2683	160
DQ6	2963	160
DQ7	3274	160
CE#	3544	225
A10	3544	477
OE#	3544	654
A11	3544	7030
A9	3544	7270
A8	3544	7447
A13	3332	7410
A14	2820	7410
A17	2643	7410
WE#	2345	7410
V_{CC}	2023	7410
V_{CC}	1810	7433

The coordinates are in microns measured from the bottom left corner of the die edge.
The V_{SS} pin is the double pad on the bottom.

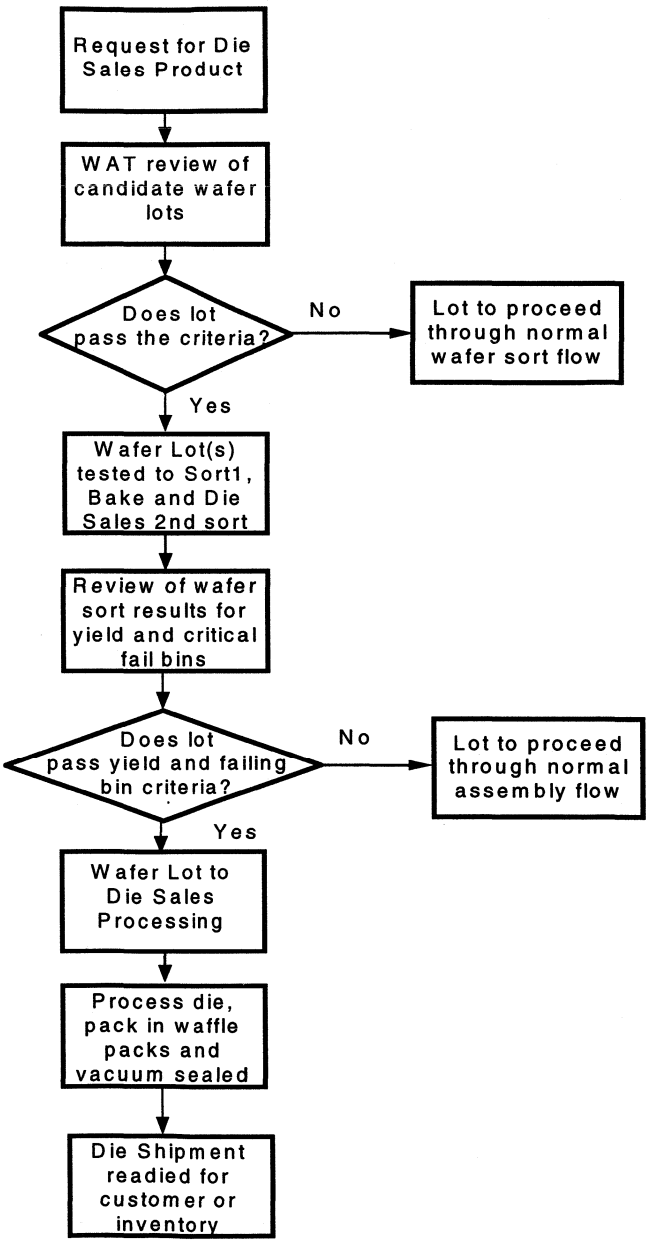
28SF040 Pad Coordinates

Die Size: 250" x 292" = 6.35 mm x 7.41 mm

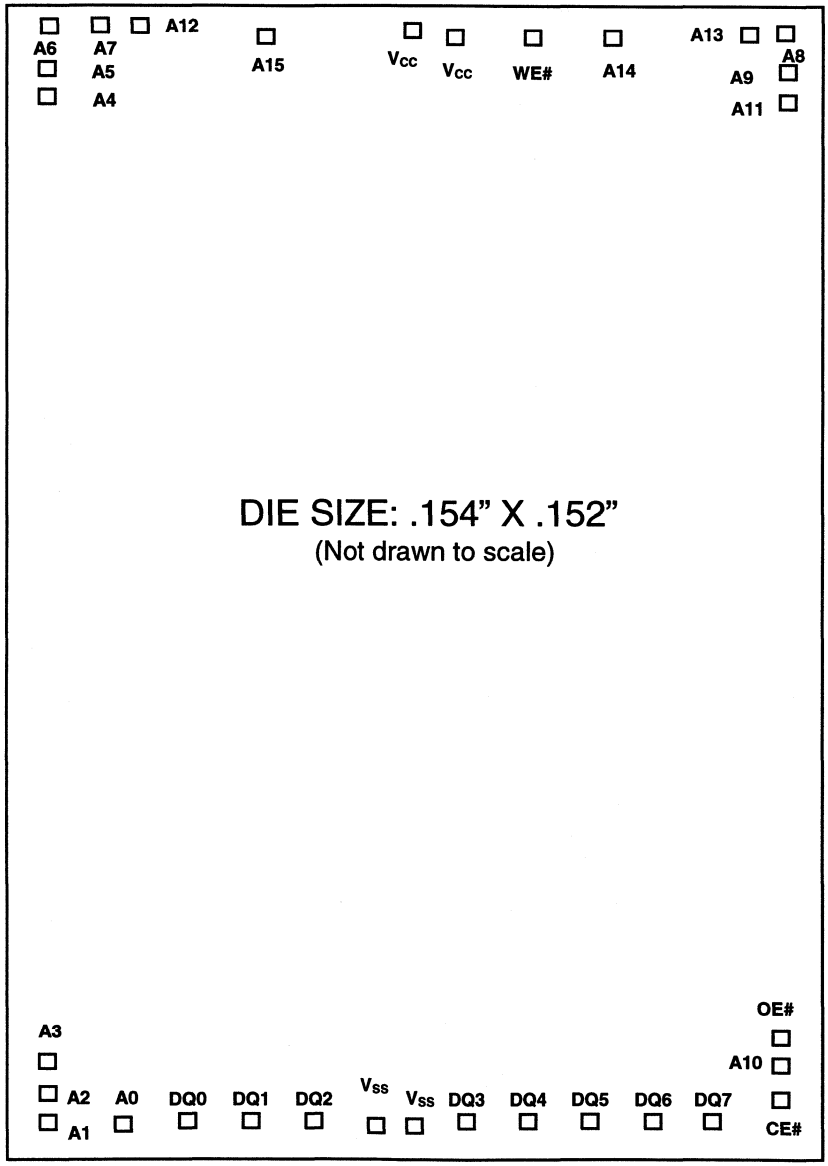
Pin Name	X Coordinate	Y Coordinate	Pin Name	X Coordinate	Y Coordinate
V_{CC}	3212	7078	DQ2	2427	147
V_{CC}	2994	7105	VSS	2862	144
A18	2741	7091	VSS	3120	163
A16	2580	7091	DQ3	3463	147
A15	2377	7091	DQ4	3803	147
A12	2216	7091	DQ5	4105	147
A7	1250	7091	DQ6	4446	147
A6	1089	7091	DQ7	4830	147
A5	886	7091	CE#	5243	142
A4	725	7091	A10	5404	142
N/C	495	7091	OE#	5607	142
N/C	154	7109	N/C	5768	142
A6	141	6922	CE#	6061	204
A5	141	6761	A10	6061	365
A4	141	6550	OE#	6061	580
A3	65	707	A11	6061	741
A2	65	546	A9	6052	6693
A1	65	343	A8	6052	6922
A1	65	182	N/C	5443	7091
N/C	418	142	A11	5201	7091
A3	669	142	A9	4933	7091
A2	837	142	A8	4707	7091
A1	1066	142	A13	4504	7091
A0	1227	142	A14	4203	7091
DQ0	1767	147	A17	4042	7091
DQ1	2069	147	WE#	3803	7091

The coordinates are in microns measured from the bottom left corner of the die edge.

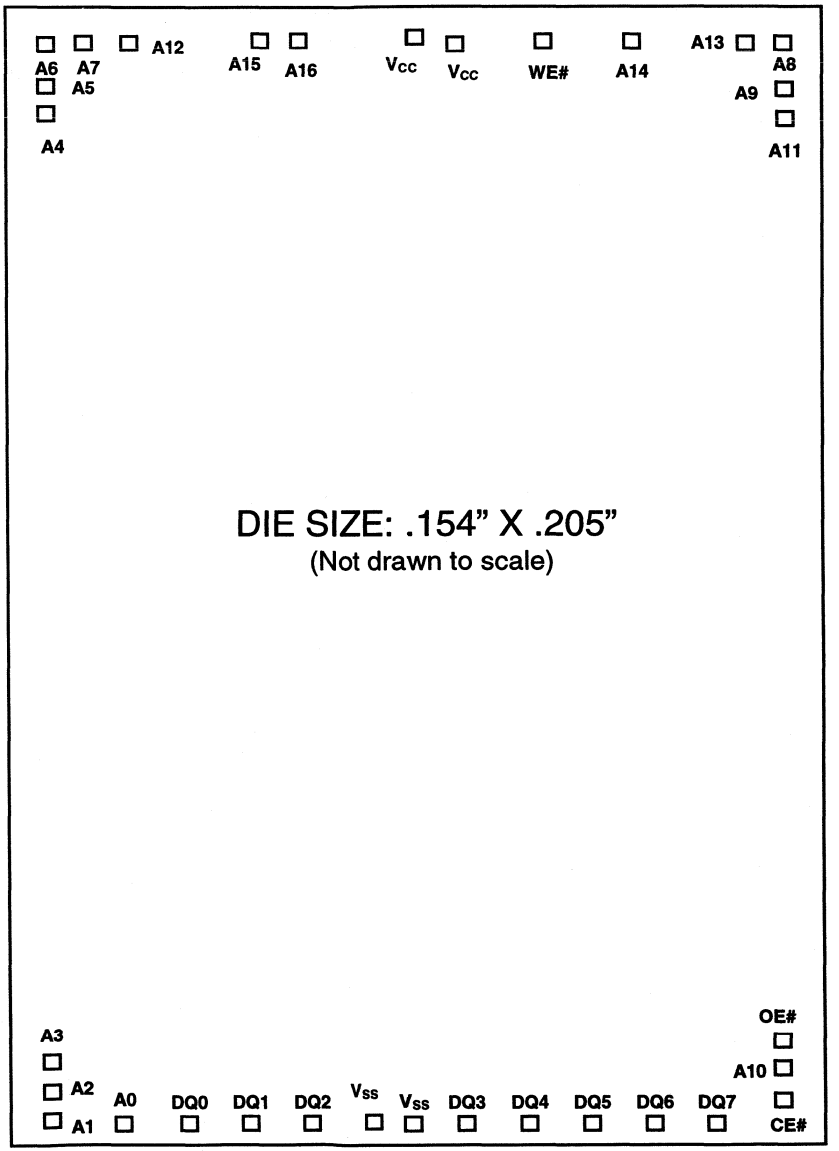
Die Sales Flow



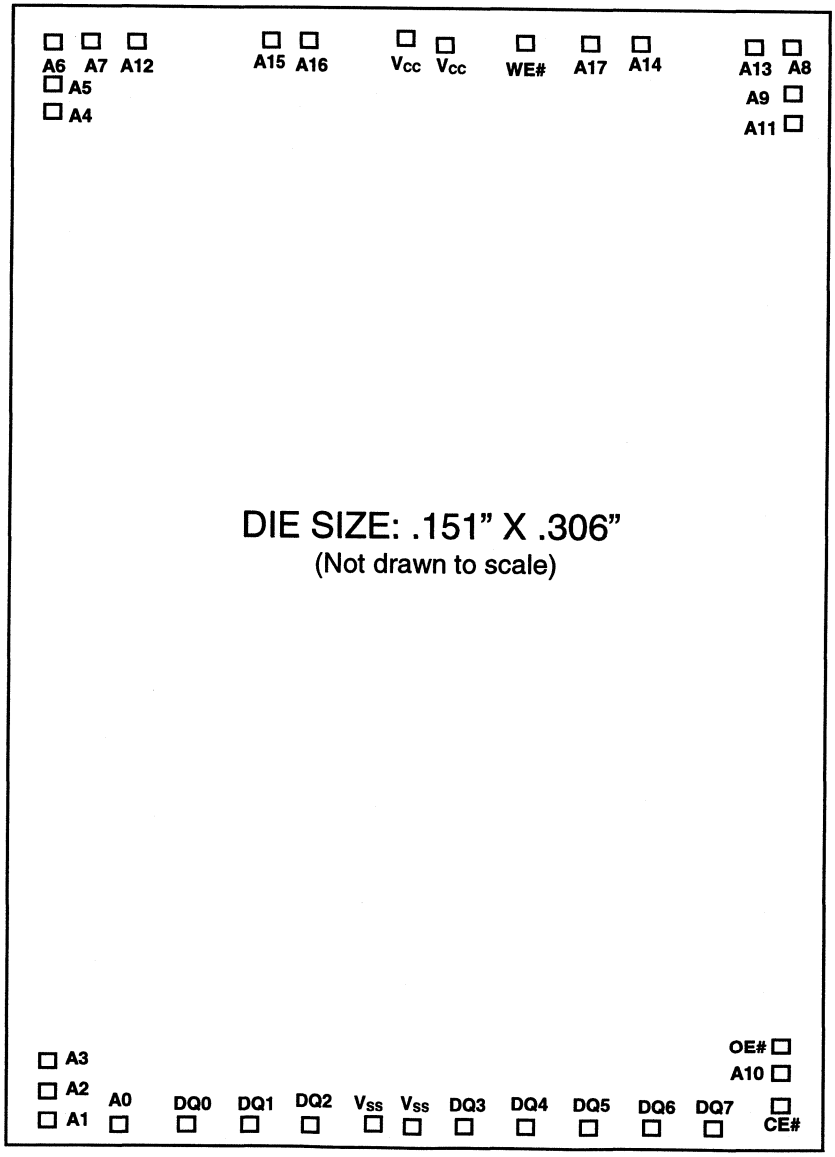
29EE512 Pad Layout Plot



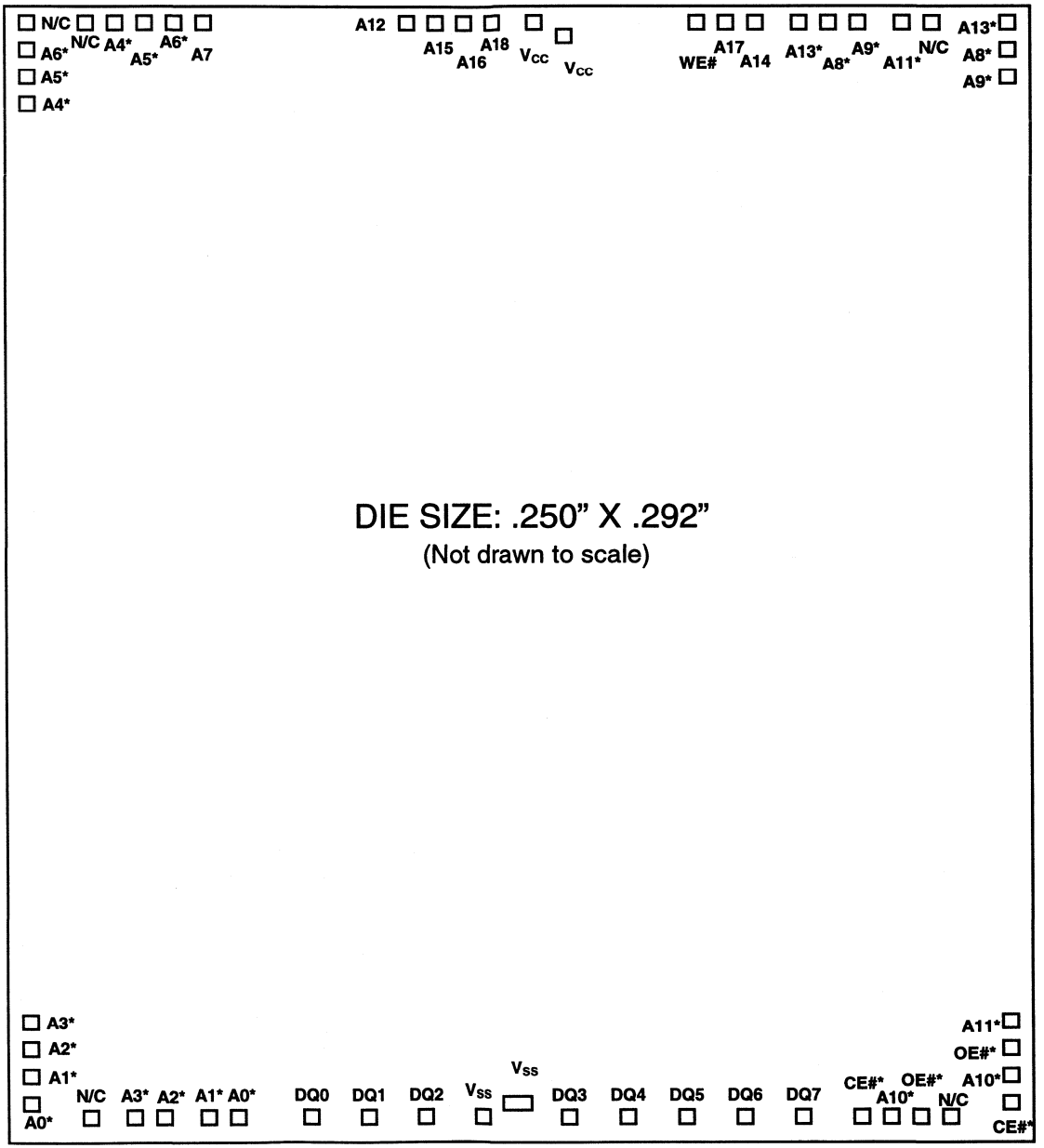
29EE010 Pad Layout Plot



29EE020 Pad Layout Plot



28SF040 Pad Layout Plot



Note * = These pins are duplicate pins, available for efficient assembly configuration.
Wire bond only one of the two pads.

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Software Drivers

29EE512 / 29LE512 / 29VE512
512 Kilobit Page Mode EEPROM

July 1996

29EE512 / 29LE512 / 29VE512
Software Drivers

ABOUT THE SOFTWARE

This application note provides examples software code for controlling page writing by byte SST's 29EE512 512 Kbit Page Mode EEPROM. Two programming languages are provide: high -level "C" for broad platform support and an optimized 8086 assembly language. In many cases, the software driver routines can be inserted "as is" into the main body of code being developed by the system software engineers. Extensive comments are included in each routine to facilitate adapting to code to specific applications. "C" language code can be used with many microprocessors and microcontrollers, while the 8086 assembly language code provides an solution optimized for 8086 assembly language code provides an solution optimized for 8086 microprocessors and embedded processors.

NOTE:

The 29EE512 is for 5.0 volt applications, the 29LE512 is for 3.0 volts application, and the 29VE512 is for 2.7 volt applications. Device functionality is identical for application of this software. For convenience, only the 29EE512 will be referenced in the example codes provided.

ABOUT THE 29EE512

Companion product datasheets for the 29EE512 should be reviewed in conjunction with this application note for a complete understanding of the device.

Writing the 29EE512 can be accomplished with two different algorithms: The first and recommended method employs the JEDEC approved "enable software protection page write" (SDP) algorithm. Using this method, any write operation (128 bytes) requires the inclusion of a series of three byte-load operations, which precede the data loading operation. The three byte-load sequence enables the SDP option during page write operation. SDP provides optimal protection from inadvertent write cycles, e.g., those triggered by noise during the system power-up or power-down. After the initial data byte-load cycle, the host must continue to load a byte into the page buffer within the byte-load cycle time (T_{BLC}) of 100µs for the 29EE512 to stay in the page load cycle. Additional bytes can then be loaded within the same page, in any order, The page load cycle will terminate if no additional byte is loaded into the page buffer within 200 µs (T_{BLCO}) from the last byte-load cycle, i.e. no subsequent WE# high-to-low transition after the last rising edge of WE#.

Both the C and 8086 assembly code in the document contain the following routines, in this order:

Name	Function
Write_29EE512	Alter data
Check_Toggle_Ready	End of write detection using Toggle bit
Check_Data_Polling	End of write detection using Data# polling
Enable_Chip_Data_Protection	Enable JEDEC standard software data protection
Check_SST_29EE512	Check manufacturer and device ID

"C" LANGUAGE DRIVERS

```
/*****************************************************************************************************/
/* Copyright Silicon Storage Technology, Inc. (SST), 1994-1996                                       */
/* Example "C" language Driver of 29EE512 512 Kbit Page Mode EEPROM                                  */
/* Chi Chung Yin, Silicon Storage Technology                                                         */
/*                                                                                                   */
/* Revision 2.0, May 1, 1996                                                                         */
/*                                                                                                   */
/* This file requires these external "timing"  routines:                                             */
/*                                                                                                   */
/*       1.) Delay_1_Milli_Second                                                                    */
/*       2.) Delay_10_Milli_Second                                                                   */
/*       3.) Delay_10_Micro_Second                                                                   */
/*****************************************************************************************************/

#define FALSE                   0
#define TRUE                    (~FALSE)

#define ROW_SIZE                128             /* Must be 128 bytes for 29EE512  */

#define SST_ID                  0xBF            /* SST Manufacture's ID code */
#define SST_29EE512             0x5D            /* SST 29EE512 device code */

typedef unsigned char           BYTE;

/*-------------------------------------------------------------------------------*/
/*                      EXERNAL ROUTINES                                         */
/*-------------------------------------------------------------------------------*/

extern void     Delay_1_Milli_Second();
extern void     Delay_10_Milli_Second();
extern void     Delay_10_Micro_Second();
extern void     Check_Toggle_Read(BYTE far *);
extern void     Check_Data_Polling(BYTE far *, BYTE);
```

```
/*****************************************************************************************************/
/* PROCEDURE:                Write_29EE512                                                           */
/*                                                                                                   */
/* This procedure can be used to write a total of 128 bytes at one write cycle to the                */
/* SST's 29EE512.                                                                                    */
/*                                                                                                   */
/* Input:                                                                                            */
/*        SRC    SOURCE address containing the data which will be                                    */
/*               written into the 29EE512.                                                           */
/*        Dst    DESTINATION address which will be written with the                                  */
/*               data passed in from ds:si                                                           */
/*                                                                                                   */
/* Out put:                                                                                          */
/*         None                                                                                      */
/*****************************************************************************************************/

void Write_29EE512 (BYTE far *Src,   BYTE far *Dst)
{
        BYTE far *Temp;
        BYTE far *SourceBuf;
        BYTE far *DestBuf;
        int Index;

        SourceBuf = Src;
        DestBuf = Dst;

        /*************************************************************************************/
        /*                          WRITTEN OPERATION                                        */
        /*                                                                                   */
        /* Issue the 3-byte "enable protection" sequence followed by 128 bytes               */
        /* of data written to the 29EE512.                                                   */
        /*************************************************************************************/

        Temp =  (BYTE far *)0xE0005555;      /* set up address to be E000:555h      */
         *Temp = 0xAA;                       /* write data 0xAA to the address      */
        Temp =  (BYTE far *)0xE0002AAA;      /* set up address to be E000:2AAAh     */
         *Temp = 0x55;                       /* write data 0x55 to the address      */
        Temp =  (BYTE far *)0xE0005555;      /* set up address to be E000:5555h     */
         *Temp = 0xA0;                       /* write data 0xA0 to the address      */

         for (Index = 0; Index < ROW_SIZE; Index++)
         {
                 *DestBuf++ = *SourceBuf++;    /* transfer data from source to destination */

         }
         Delay_1_Milli_Second();          /* wait 1ms to start writing              */

         Check_Toggle_Ready(Dst);     /* wait for TOGGLE bit to get ready       */
}
```

```
/*****************************************************************************************************/
/* PROCEDURE:                Check_Toggle_Ready                                                      */
/*                                                                                                   */
/* During the internal write cycle, any consecutive read operation                                   */
/* on DQ6 will produce alternating 0's and 1's i.e. toggling between                                 */
/* 0 and 1.  When the write cycle is completed, DQ6 of the data will                                 */
/* stop toggling.  After the DQ6 data bit stops toggling, the device is ready                        */
/* for next operation.                                                                               */
/*                                                                                                   */
/* Input:                                                                                            */
/*        Dst             must already set-up by the caller                                          */
/*                                                                                                   */
/* Output:                                                                                           */
/*        None                                                                                       */
/*****************************************************************************************************/

void Check_Toggle_Ready (BYTE far  *Dst)
{
        BYTE Loop = TRUE;
        BYTE PreData;
        BYTE CurrData;
        unsigned long TimeOut = 0;

        PreData = *Dst;
        PreData = PreData & 0x40;
        while ((Timeout< 0x07FFFFFF) && (Loop))
        {
                CurrData = *Dst;
                CurrData = CurrData & 0x40;
                if (PreData == CurrData)
                        Loop = FALSE;           /* ready to exit the while loop */
                PreData = CurrData;
                TimeOut++;
        }
}
```

```
/*****************************************************************************************************/
/* PROCEDURE:                Check_Data_Polling                                                      */
/*                                                                                                   */
/* During the internal write cycle, any attempt to read DQ7 of the last byte loaded during           */
/* the page/byte-load cycle will receive the complement of the true data.  Once the                  */
/* write cycle is completed, DQ7 will show true data.                                                */
/*                                                                                                   */
/* Input:                                                                                            */
/*       Dst             must already set-up by the caller                                           */
/*       TrueData        this is the original (true) data                                            */
/*                                                                                                   */
/* Output:                                                                                           */
/*       None                                                                                        */
/*****************************************************************************************************/

void Check_Data_Polling (BYTE FAR  *Dst,        BYTE TrueData)
{
        BYTE Loop = TRUE;
        BYTE CurrData;
        unsigned long TimeOut = 0;

        TrueData = TrueData &  0x80;
        while ((Timeout< 0x07FFFFFF) && (Loop))
        {
                CurrData = *Dst;
                CurrData = CurrData & 0x80;
                if (TrueData == CurrData)
                        Loop = FALSE;           /* ready to exit the while loop  */
                TimeOut++;
        }
}
```

```
/*****************************************************************************************************/
/* PROCEDURE:                Enable_Chip_Data_Protection                                             */
/*                                                                                                   */
/* This procedure ENABLES the data  protection feature on the 29EE512                                */
/* 512 Kbit Page Mode EEPROM.  After calling this routine, the chip cannot be written                */
/* unless preceded by the three Byte-Load sequence.                                                  */
/*                                                                                                   */
/* Input:                                                                                            */
/*        None                                                                                       */
/*                                                                                                   */
/* Output:                                                                                           */
/*        None                                                                                       */
/*****************************************************************************************************/

void Enable_Chip_Data_Protection()
{
        BYTE  far  *Temp;

        Temp  = (BYTE far *)0xE0005555;      /* set up address to be E000:5555h     */
        *Temp = 0xAA;                        /* write data 0xAA to the address      */
        Temp  = (BYTE far *)0xE0002AAA;      /* set up address to be E000:2AAAh     */
        *Temp = 0x55;                        /* write data ox55 to the address      */
        Temp  = (BYTE far *)0xE0005555;      /* set up address to be E000:5555h     */
        *Temp = 0xA0;                        /* write data 0xA0 to the address      */

        Delay_10_Milli Second();
}
```

```
/*****************************************************************************************************/
/* PROCEDURE:                    Check_SST_29EE512                                                   */
/*                                                                                                   */
/* This procedure  decides whether a  physical hardware device has a SST                             */
/* 29EE512 512 Kbit Page Mode EEPROM installed or not.                                               */
/* without using the three Byte-Load sequence.                                                       */
/*                                                                                                   */
/* Input:                                                                                            */
/*        None                                                                                       */
/*                                                                                                   */
/* Output:                                                                                           */
/*        return -1:  indicates not a SST 29EE512                                                    */
/*        return 0:   indicates is    a SST 29EE512                                                  */
/*****************************************************************************************************/

int Check_SST_29EE512()
{
        BYTE far  *Temp;
        BYTE SST_id1;
        BYTE SST_id2;
        int   ReturnStatus;

        /*  Issue the Software Product ID code to 29EE512  */

        Temp  = (BYTE far *)0xE0005555;         /* set up address to be E000:5555h    */
        *Temp = 0xAA;                           /* write data 0xAA to the address     */
        Temp  = (BYTE far *)0xE0002AAA;         /* set up address to be E000:2AAAh    */
        *Temp = 0x55;                           /* write data ox55 to the address     */
        Temp  = (BYTE far *)0xE0005555;         /* set up address to be E000:5555h    */
        *Temp = 0x90;                           /* write data 0x80 to the address     */

        Delay_10_Milli Second();

        /* Read the product ID from 29EE512 */

        Temp  = (BYTE far *)0xE0000000;         /* set up address to be E000:0000h    */
        SST_id1  =  *Temp;                      /* get first ID byte                  */
        Temp  =  (BYTE far *)0xE0000001;        /* set up address to be E000:0001h    */

        if ((SST_id1 == SST_ID) && (SST_id2 ==SST_29EE512))
                ReturnStatus = 0;
        else
                ReturnStatus = -1;
```

```
        /* Issue the Soffware Product ID Exit code thus returning the 29EE512      */
        /* to the read operating mode                                              */

        Temp  = (BYTE far *)0xE0005555;     /* set up address to be E000:5555h     */
        *Temp = 0xAA;                       /* write data 0xAA to the address      */
        Temp  = (BYTE far *)0xE0002AAA;     /* set up address to be E000:2AAAh     */
        *Temp = 0x55;                       /* write data 0x55 to the address      */
        Temp  = (BYTE far *)0xE0005555;     /* set up address to be E000:5555h     */
        *Temp =0xF0;                        /* write data 0xF0 to the address      */

        Delay_10_Milli Second();

        return(ReturnStatus);
}
```

8086 ASSEMBLY LANGUAGE DRIVERS

```
; ========================================================================
; Copyright Silicon Storage Technology, Inc. (SST), 1994-1996
; EXAMPLE 8086 assembly Drivers for 29EE512 512 Kbit Page Mode EEPROM
; Chi Chung Yin,  Silicon Storage Technology
;
; Revision 2.0, Mayt 1, 1996
;
; This file requires these external "timing" routines:
;
;       1.) Delay_1_Milli_Second
;       2.) Delay_10_Milli_ Second
;       3.) Delay_10_Micro_Second
; ========================================================================

ROW_SIZE            EQU   128               ;Must be 128 bytes for 29EE512

SST_ID              EQU   0BFh              ;SST Manufacture's ID code
SST_29EE512         EQU   05Dh              ;SST 29EE512 internal code

ABS_SEGMENT         EQU   0E000h

extrn   Delay_1_Milli_Second:near
extrn   Delay_10_Milli_Second:near
extrn   Delay_10_Micro_Second:near
```

```
; ============================================================================
; PROCEDURE:                    Write_29EE512
;
; This procedure can be used to write a total of 128 bytes at one write cycle to the
; SST's 29EE512.
;
; Input:
;       ds:si   SOURCE address containing the data which will be
;               written into the 29EE512.
;       es:di   DESTINATION address which will be written with the
;               data passed in for ds;si
;
; Output:
;       None
;       SI, DI:  Contains the original values
; ============================================================================

Write_29EE512          proc    near

        push    ax
        push    bx
        push    cx
        push    di
        push    si
        push                    ; preserve the "Direction" flag in the FLAG
                                ; register

        cld                     ; clear "Direction" flag in the FLAG register
                                ; auto-increment SI, and DI

; ============================================================================
;                               WRITE OPERATION
; Let's issue the 3-byte "Enable Protection" sequence to the 29EE512
; chip followed by the 128 bytes of data.
; ============================================================================

        push    ax
        push    ds

        mov     as, ABS_SEGMENT
        mov     ds, ax
        mov     ds:byte ptr [5555h], 0aah; 3 bytes of  "enable protection"
        mov     ds:byte ptr [2AAAh], 055h       ; sequence to the chip
        mov     ds:byte ptr [5555h], 0A0h

        pop     ds
        pop     ax

        mov     cx,  ROW_SIZE           ; we will write 128 bytes
        push    si                      ; save original values
        push    di
```

```
        cli                             ; no disturb allowed while in the process
                                        ; of writing the 29EE512.
DRP1:
        lodsb                           ; do not use " rep movsb" instruction
        stosb                           ;
        loop    DRP1                    ; write 128 bytes

        call    Delay_1_Milli Second    ; wait 1ms to start writing
        pop     di                      ; restore original values
        pop     si
        call    check_Toggle_Ready      ; wait for TOGGLE bit to get ready

        popf
        pop     si
        pop     di
        pop     cx
        pop     bx
        pop     ax

        ret

Wrtie_29EE512           endp
```

```
;=============================================================================
; PROCEDURE:                    Check_Toggle_Ready
;
; During the internal write cycle, any consecutive read operation
; on DQ6 will produce alternating O's and 1's, i.e. toggling between
; 0 and 1. When the write cycle is completed, the DQ6 data will
; stop toggling. After the DQ6 data stops toggling, the device is ready
; for the next operation.
;
; Input::
;       es:di    must already set-up by the calller
;
; Output:
;       None
;=============================================================================

Check_Toggle_Ready   proc    near

        push    ax

        mov     al, es:[di]             ; read a byte form the chip
        and     al,40h                  ; mask out the TOGGLE bit (DQ6)
CTR_Tog2:
        mov     ah, es:[di]             ; read the same byte from the chip again
        and     ah, 40h                 ; mask out the TOGGLE bit (DQ6)
        cmp     al, ah                  ; is DQ6 still toggling?
        je      CTR_T0g3                ; No, then the write operation is done
        xchg    ah, al                  ; YES, then continue chicking...
        jmp     short CTR_Tog2
CTR_Tog3:
        pop     ax

        ret

Check_Toggle_Ready   endp
```

```
;=============================================================================
; PROCEDURE:                    Check_Data_Polling
;
; During the internal write cycle, any attemp to read DQ7 of the last byte loaded during
; the page/byte-load cycle will receive the complement of the true data.  Once the
; write cycle is completed, DQ7 will show  true data.
;
; Input:
;       es:di    must  already set-up by the caller
;       bl       contains the original (true) data
;
; Output:
;       None
;
;=============================================================================

Check_Data_Polling      proc    near

        push    ax

        an      bl, 80h                 ; mask out the DQ7 bit
CDP_Tog2:
        mov     al, es:[di]             ; read a byte from the chip
        and     al,80h                  ; mask out the DQ7 bit
        camp    al,bl                   ; is DQ7 still complementing?
        jne     CDP Tog2

        pop     ax

        ret

Check_Data_Polling      endp
```

```
;=============================================================================
; PROCEDURE:                    Enable_Chip_Data_Protection
;
; This procedure ENABLES the data protection feature on the 29EE512
; 512 Kbit Page Mode EEPROM.  After calling the routine, the chip can be written
; without using the three Byte-Load sequence.
;
; Input::
:       None
;
; Output:
;       None
;=============================================================================

Disable_Chip_Data_Protection   proc    near

        push    ax                          ; preserve registers' value
        push    ds

        cli
        mov     ax, ABS_SEGMENT
        mov     ds, ax

        mov     ds:byte ptr [5555h], 0AAh   ; issue the 3-byte protect
        mov     ds:byte ptr [2AAAh], 055h   ; sequence to the 29EE512
        mov     ds:byte ptr [5555h], 0A0h

        call    Delay_10_Milli_Second

        pop     ds
        pop     ax

        ret

Enable_Chip_Data_Protection endp
```

```
;=============================================================================
; PROCEDURE:                    Check_SST_29EE512
;
; This procedure decides whether a physical hardware device has a SST's
; 29EE512 512 Kbit Page Mode EEPROM installed or not.
;
; Input:
;       None
;
; Output:
;       carry bit:  SET means not a SST 29EE512
;       carry bit:  CLEARED means a SST 29EE512
;
;=============================================================================

Check_SST_29EE512  proc    near

        push    ax                          ; preserve registers' value
        push ds

        cli
        mov     ax, ABS_SEGMENT
        mov     ds, ax

        mov     ds:byte ptr [5555h], 0AAh   ; issue the 6-byte product ID
        mov     ds:byte ptr [2AAAh], 055h   ; command to the 29EE512
        mov     ds:byte ptr [5555h], 090h

        call    Delay_10_Micro_Second       ; wait until Tww expires

        mov     al, ds:[0]
        cmp     al, SST_ID                  ; is this a SST part?
        jne     CSC5                        ; NO, then return Carry set
        mov     al,ds:[1]
        cmp     al, SST_29EE512             ; Is it 29EE512?
        jne     CSC5                        ; NO, then Non-SST part
CSC4:
        clc
        pushf                               ; save the result on the STACK
        jmp     short CSC6
CSC5:
        stc                                 ; save the result on the STACK
        pushf
```

```
CSC6:
;
; Issue the Software Product ID Exit code thus returning the 29EE512
; to the read operation mode.
;
        mov     ds:byte ptr [5555h], 0AAh       ; issue the 3-byte product ID
        mov     ds:byte ptr [2AAAh], 055h       ; exit command to the 29EE512
        mov     ds:byte ptr [5555h], 0F0h

        call    Delay_10_Micro_Second           ; wait until Tww expires

        popf                                    ; restore result from the stack
        pop     ds                              ; restore original values
        pop     ax

        ret

Check_SST_29EE512 endp
```

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Software Drivers

29EE010 / 29LE010 / 29VE010
1 Megabit Page Mode EEPROM

July 1996

29EE010 / 29LE010 / 29VE010
Software Drivers

ABOUT THE SOFTWARE

This application note provides examples software code for controlling page writing by byte SST's 29EE010 1 Mbit Page Mode EEPROM. Two programming languages are provide: high -level "C" for broad platform support and an optimized 8086 assembly language. In many cases, the software driver routines can be inserted "as is" into the main body of code being developed by the system software engineers. Extensive comments are included in each routine to facilitate adapting to code to specific applications. "C" language code can be used with many microprocessors and microcontrollers, while the 8086 assembly language code provides an solution optimized for 8086 assembly language code provides an solution optimized for 8086 microprocessors and embedded processors.

NOTE:

The 29EE010 is for 5.0 volt applications, the 29LE010 is for 3.0 volts application, and the 29VE010 is for 2.7 volt applications. Device functionality is identical for application of this software. For convenience, only the 29EE010 will be referenced in the example codes provided.

ABOUT THE 29EE010

Companion product datasheets for the 29EE010 should be reviewed in conjunction with this application note for a complete understanding of the device.

Writing the 29EE010 can be accomplished with two different algorithms: The first and recommended method employs the JEDEC approved "enable software protection page write" (SDP) algorithm. Using this method, any write operation (128 bytes) requires the inclusion of a series of three byte-load operations, which precede the data loading operation. The three byte-load sequence enables the SDP option during page write operation. SDP provides optimal protection from inadvertent write cycles, e.g., those triggered by noise during the system power-up or power-down. After the initial data byte-load cycle, the host must continue to load a byte into the page buffer within the byte-load cycle time (T_{BLC}) of 100µs for the 29EE010 to stay in the page load cycle. Additional bytes can then be loaded within the same page, in any order, The page load cycle will terminate if no additional byte is loaded into the page buffer within 200 µs (T_{BLCO}) from the last byte-load cycle, i.e. no subsequent WE# high-to-low transition after the last rising edge of WE#.

Both the C and 8086 assembly code in the document contain the following routines, in this order:

Name	Function
Write_29EE010	Alter data
Check_Toggle_Ready	End of write detection using Toggle bit
Check_Data_Polling	End of write detection using Data# polling
Enable_Chip_Data_Protection	Enable JEDEC standard software data protection
Check_SST_29EE010	Check manufacturer and device ID

"C" LANGUAGE DRIVERS

```
/*****************************************************************************************************/
/* Copyright Silicon Storage Technology, Inc. (SST), 1994-1996                                       */
/* Example "C" language Driver of 29EE010 1 Mbit Page Mode EEPROM                                    */
/* Chi Chung Yin, Silicon Storage Technology                                                         */
/*                                                                                                   */
/* Revision 2.0, May 1, 1996                                                                         */
/*                                                                                                   */
/* This file requires these external "timing"  routines:                                             */
/*                                                                                                   */
/*       1.) Delay_1_Milli_Second                                                                    */
/*       2.) Delay_10_Milli_Second                                                                   */
/*       3.) Delay_10_Micro_Second                                                                   */
/*****************************************************************************************************/

#define FALSE                   0
#define TRUE                    (~FALSE)

#define ROW_SIZE                128             /* Must be 128 bytes for 29EE010  */

#define SST_ID                  0xBF            /* SST Manufacture's ID code */
#define SST_29EE010             0x07            /* SST 29EE010 device code */

typedef unsigned char           BYTE;

/*-------------------------------------------------------------------------*/
/*                      EXERNAL ROUTINES                                   */
/*-------------------------------------------------------------------------*/

extern void     Delay_1_Milli_Second();
extern void     Delay_10_Milli_Second();
extern void     Delay_10_Micro_Second();
extern void     Check_Toggle_Read(BYTE far *);
extern void     Check_Data_Polling(BYTE far *, BYTE);
```

```
/*****************************************************************************************************/
/* PROCEDURE:                Write_29EE010                                                           */
/*                                                                                                   */
/* This procedure can be used to write a total of 128 bytes at one write cycle to the                */
/* SST's 29EE010.                                                                                    */
/*                                                                                                   */
/* Input:                                                                                            */
/*        SRC    SOURCE address containing the data which will be                                    */
/*               written into the 29EE010.                                                           */
/*        Dst    DESTINATION address which will be written with the                                  */
/*               data passed in from ds:si                                                           */
/*                                                                                                   */
/* Out put:                                                                                          */
/*         None                                                                                      */
/*****************************************************************************************************/

void Write_29EE010 (BYTE far *Src,   BYTE far *Dst)
{
        BYTE far *Temp;
        BYTE far *SourceBuf;
        BYTE far *DestBuf;
        int Index;

        SourceBuf = Src;
        DestBuf = Dst;

        /*************************************************************************************/
        /*                              WRITTEN OPERATION                                    */
        /*                                                                                   */
        /* Issue the 3-byte "enable protection" sequence followed by 128 bytes               */
        /* of data written to the 29EE010.                                                   */
        /*************************************************************************************/

        Temp =  (BYTE far *)0xE0005555;      /* set up address to be E000:555h      */
         *Temp = 0xAA;                       /* write data 0xAA to the address      */
        Temp =  (BYTE far *)0xE0002AAA;      /* set up address to be E000:2AAAh     */
         *Temp = 0x55;                       /* write data 0x55 to the address      */
        Temp =  (BYTE far *)0xE0005555;      /* set up address to be E000:5555h     */
         *Temp = 0xA0;                       /* write data 0xA0 to the address      */

         for (Index = 0; Index < ROW_SIZE; Index++)
         {
                 *DestBuf++ = *SourceBuf++;    /* transfer data from source to destination */

         }
         Delay_1_Milli_Second();          /* wait 1ms to start writing              */

         Check_Toggle_Ready(Dst);     /* wait for TOGGLE bit to get ready       */
}
```

```
/*****************************************************************************************************/
/* PROCEDURE:                Check_Toggle_Ready                                                      */
/*                                                                                                   */
/* During the internal write cycle, any consecutive read operation                                   */
/* on DQ6 will produce alternating 0's and 1's i.e. toggling between                                 */
/* 0 and 1.  When the write cycle is completed, DQ6 of the data will                                 */
/* stop toggling.  After the DQ6 data bit stops toggling, the device is ready                        */
/* for next operation.                                                                               */
/*                                                                                                   */
/* Input:                                                                                            */
/*        Dst             must already set-up by the caller                                          */
/*                                                                                                   */
/* Output:                                                                                           */
/*        None                                                                                       */
/*****************************************************************************************************/

void Check_Toggle_Ready (BYTE far  *Dst)
{
        BYTE Loop = TRUE;
        BYTE PreData;
        BYTE CurrData;
        unsigned long TimeOut = 0;

        PreData = *Dst;
        PreData = PreData & 0x40;
        while ((Timeout< 0x07FFFFFF) && (Loop))
        {
                CurrData = *Dst;
                CurrData = CurrData & 0x40;
                if (PreData == CurrData)
                        Loop = FALSE;           /* ready to exit the while loop */
                PreData = CurrData;
                TimeOut++;
        }
}
```

```
/*****************************************************************************************************/
/* PROCEDURE:                Check_Data_Polling                                                      */
/*                                                                                                   */
/* During the internal write cycle, any attempt to read DQ7 of the last byte loaded during           */
/* the page/byte-load cycle will receive the complement of the true data.  Once the                  */
/* write cycle is completed, DQ7 will show true data.                                                */
/*                                                                                                   */
/* Input:                                                                                            */
/*       Dst             must already set-up by the caller                                           */
/*       TrueData        this is the original (true) data                                            */
/*                                                                                                   */
/* Output:                                                                                           */
/*       None                                                                                        */
/*****************************************************************************************************/

void Check_Data_Polling (BYTE FAR  *Dst,        BYTE TrueData)
{
        BYTE Loop = TRUE;
        BYTE CurrData;
        unsigned long TimeOut = 0;

        TrueData = TrueData &  0x80;
        while ((Timeout< 0x07FFFFFF) && (Loop))
        {
                CurrData = *Dst;
                CurrData = CurrData & 0x80;
                if (TrueData == CurrData)
                        Loop = FALSE;           /* ready to exit the while loop  */
                TimeOut++;
        }
}
```

```
/*****************************************************************************************************/
/* PROCEDURE:                Enable_Chip_Data_Protection                                             */
/*                                                                                                   */
/* This procedure ENABLES the data  protection feature on the 29EE010                                */
/* 1 Mbit Page Mode EEPROM.  After calling this routine, the chip cannot be written                  */
/* unless preceded by the three Byte-Load sequence.                                                  */
/*                                                                                                   */
/* Input:                                                                                            */
/*        None                                                                                       */
/*                                                                                                   */
/* Output:                                                                                           */
/*        None                                                                                       */
/*****************************************************************************************************/

void Enable_Chip_Data_Protection()
{
        BYTE  far  *Temp;

        Temp  = (BYTE far *)0xE0005555;      /* set up address to be E000:5555h     */
        *Temp = 0xAA;                        /* write data 0xAA to the address      */
        Temp  = (BYTE far *)0xE0002AAA;      /* set up address to be E000:2AAAh     */
        *Temp = 0x55;                        /* write data ox55 to the address      */
        Temp  = (BYTE far *)0xE0005555;      /* set up address to be E000:5555h     */
        *Temp = 0xA0;                        /* write data 0xA0 to the address      */

        Delay_10_Milli Second();
}
```

```
/*****************************************************************************************************/
/* PROCEDURE:                Check_SST_29EE010                                                       */
/*                                                                                                   */
/* This procedure  decides whether a  physical hardware device has a SST                             */
/* 29EE010 1 Mbit Page Mode EEPROM installed or not.                                                 */
/* without using the three Byte-Load sequence.                                                       */
/*                                                                                                   */
/* Input:                                                                                            */
/*        None                                                                                       */
/*                                                                                                   */
/* Output:                                                                                           */
/*        return -1:  indicates not a SST 29EE010                                                    */
/*        return 0:   indicates is    a SST 29EE010                                                  */
/*****************************************************************************************************/

int Check_SST_29EE010()
{
        BYTE far  *Temp;
        BYTE SST_id1;
        BYTE SST_id2;
        int    ReturnStatus;

        /*  Issue the Software Product ID code to 29EE010  */

        Temp  = (BYTE far *)0xE0005555;      /* set up address to be E000:5555h    */
        *Temp = 0xAA;                        /* write data 0xAA to the address     */
        Temp  = (BYTE far *)0xE0002AAA;      /* set up address to be E000:2AAAh    */
        *Temp = 0x55;                        /* write data ox55 to the address     */
        Temp  = (BYTE far *)0xE0005555;      /* set up address to be E000:5555h    */
        *Temp = 0x80;                        /* write data 0x80 to the address     */
        Temp  = (BYTE far *)0xE0005555;      /* set up address to be E000:5555h    */
        *Temp = 0xAA;                        /* write data 0xAA to the address     */
        Temp  = (BYTE far *)0xE0002AAA;      /* set up address to be E000:2AAAh    */
        *Temp = 0x55;                        /* write data 0x55 to the address     */
        Temp  = (BYTE far *)0xE0005555;      /* set up address to be E000:5555h    */
        *Temp =0x60;                         /* write data 0x60 to the address     */

        Delay_10_Milli Second();

        /* Read the product ID from 29EE010 */

        Temp  = (BYTE far *)0xE0000000;      /* set up address to be E000:0000h    */
        SST_id1  =  *Temp;                   /* get first ID byte                  */
        Temp  =  (BYTE far *)0xE0000001;     /* set up address to be E000:0001h    */

        if ((SST_id1 == SST_ID) && (SST_id2 ==SST_29EE010))
                ReturnStatus = 0;
        else
                ReturnStatus = -1;
```

```
    /* Issue the Soffware Product ID Exit code thus returning the 29EE010      */
    /* to the read operating mode                                              */

    Temp  = (BYTE far *)0xE0005555;     /* set up address to be E000:5555h     */
    *Temp = 0xAA;                       /* write data 0xAA to the address      */
    Temp  = (BYTE far *)0xE0002AAA;     /* set up address to be E000:2AAAh     */
    *Temp = 0x55;                       /* write data 0x55 to the address      */
    Temp  = (BYTE far *)0xE0005555;     /* set up address to be E000:5555h     */
    *Temp =0xF0;                        /* write data 0xF0 to the address      */

    Delay_10_Milli Second();

    return(ReturnStatus);
}
```

8086 ASSEMBLY LANGUAGE DRIVERS

```
; ============================================================================
; Copyright Silicon Storage Technology, Inc. (SST), 1994-1996
; EXAMPLE 8086 assembly Drivers for 29EE010 1 Mbit Page Mode EEPROM
; Chi Chung Yin,  Silicon Storage Technology
;
; Revision 2.0, Mayt 1, 1996
;
; This file requires these external "timing" routines:
;
;       1.) Delay_1_Milli_Second
;       2.) Delay_10_Milli_ Second
;       3.) Delay_10_Micro_Second
; ============================================================================

ROW_SIZE            EQU   128               ;Must be 128 bytes for 29EE010

SST_ID              EQU   0BFh              ;SST Manufacture's ID code
SST_29EE010         EQU   007h              ;SST 29EE010 internal code

ABS_SEGMENT         EQU   0E000h

extrn   Delay_1_Milli_Second:near
extrn   Delay_10_Milli_Second:near
extrn   Delay_10_Micro_Second:near
```

```
; ============================================================================
; PROCEDURE:                    Write_29EE010
;
; This procedure can be used to write a total of 128 bytes at one write cycle to the
; SST's 29EE010.
;
; Input:
;       ds:si   SOURCE address containing the data which will be
;               written into the 29EE010.
;       es:di   DESTINATION address which will be written with the
;               data passed in for ds;si
;
; Output:
;       None
;       SI, DI:  Contains the original values
; ============================================================================

Write_29EE010           proc    near

        push    ax
        push    bx
        push    cx
        push    di
        push    si
        push                    ; preserve the "Direction" flag in the FLAG
                                ; register

        cld                     ; clear "Direction" flag in the FLAG register
                                ; auto-increment SI, and DI

; ============================================================================
;                               WRITE OPERATION
; Let's issue the 3-byte "Enable Protection" sequence to the 29EE010
; chip followed by the 128 bytes of data.
; ============================================================================

        push    ax
        push    ds

        mov     as, ABS_SEGMENT
        mov     ds, ax
        mov     ds:byte ptr [5555h], 0aah; 3 bytes of  "enable protection"
        mov     ds:byte ptr [2AAAh], 055h       ; sequence to the chip
        mov     ds:byte ptr [5555h], 0A0h

        pop     ds
        pop     ax

        mov     cx,  ROW_SIZE           ; we will write 128 bytes
        push    si                      ; save original values
        push    di
```

```
        cli                             ; no disturb allowed while in the process
                                        ; of writing the 29EE010.
DRP1:
        lodsb                           ; do not use " rep movsb" instruction
        stosb                           ;
        loop    DRP1                    ; write 128 bytes

        call    Delay_1_Milli Second    ; wait 1ms to start writing
        pop     di                      ; restore original values
        pop     si
        call    check_Toggle_Ready      ; wait for TOGGLE bit to get ready

        popf
        pop     si
        pop     di
        pop     cx
        pop     bx
        pop     ax

        ret

Wrtie_29EE010           endp
```

```
;=============================================================================
; PROCEDURE:                    Check_Toggle_Ready
;
; During the internal write cycle, any consecutive read operation
; on DQ6 will produce alternating O's and 1's, i.e. toggling between
; 0 and 1. When the write cycle is completed, the DQ6 data will
; stop toggling. After the DQ6 data stops toggling, the device is ready
; for the next operation.
;
; Input::
;       es:di    must already set-up by the calller
;
; Output:
;       None
;=============================================================================

Check_Toggle_Ready   proc    near

        push    ax

        mov     al, es:[di]             ; read a byte form the chip
        and     al,40h                  ; mask out the TOGGLE bit (DQ6)
CTR_Tog2:
        mov     ah, es:[di]             ; read the same byte from the chip again
        and     ah, 40h                 ; mask out the TOGGLE bit (DQ6)
        cmp     al, ah                  ; is DQ6 still toggling?
        je      CTR_T0g3                ; No, then the write operation is done
        xchg    ah, al                  ; YES, then continue chicking...
        jmp     short CTR_Tog2
CTR_Tog3:
        pop     ax

        ret

Check_Toggle_Ready   endp
```

```
;=============================================================================
; PROCEDURE:                    Check_Data_Polling
;
; During the internal write cycle, any attemp to read DQ7 of the last byte loaded during
; the page/byte-load cycle will receive the complement of the true data.  Once the
; write cycle is completed, DQ7 will show  true data.
;
; Input:
;       es:di    must  already set-up by the caller
;       bl       contains the original (true) data
;
; Output:
;       None
;
;=============================================================================

Check_Data_Polling      proc    near

        push    ax

        an      bl, 80h                 ; mask out the DQ7 bit
CDP_Tog2:
        mov     al, es:[di]             ; read a byte from the chip
        and     al,80h                  ; mask out the DQ7 bit
        camp    al,bl                   ; is DQ7 still complementing?
        jne     CDP Tog2

        pop     ax

        ret

Check_Data_Polling      endp
```

```
;=============================================================================
; PROCEDURE:                    Enable_Chip_Data_Protection
;
; This procedure ENABLES the data protection feature on the 29EE010
; 1 Mbit Page Mode EEPROM.  After calling the routine, the chip can be written
; without using the three Byte-Load sequence.
;
; Input::
:       None
;
; Output:
;       None
;=============================================================================

Disable_Chip_Data_Protection   proc    near

        push    ax                          ; preserve registers' value
        push    ds

        cli
        mov     ax, ABS_SEGMENT
        mov     ds, ax

        mov     ds:byte ptr [5555h], 0AAh   ; issue the 3-byte protect
        mov     ds:byte ptr [2AAAh], 055h   ; sequence to the 29EE010
        mov     ds:byte ptr [5555h], 0A0h

        call    Delay_10_Milli_Second

        pop     ds
        pop     ax

        ret

Enable_Chip_Data_Protection endp
```

```
;=============================================================================
; PROCEDURE:                    Check_SST_29EE010
;
; This procedure decides whether a physical hardware device has a SST's
; 29EE010 1 Mbit Page Mode EEPROM installed or not.
;
; Input:
;       None
;
; Output:
;       carry bit:  SET means not a SST 29EE010
;       carry bit:  CLEARED means a SST 29EE010
;
;=============================================================================

Check_SST_29EE010   proc    near

        push    ax                          ; preserve registers' value
        push ds

        cli
        mov     ax, ABS_SEGMENT
        mov     ds, ax

        mov     ds:byte ptr [5555h], 0AAh   ; issue the 6-byte product ID
        mov     ds:byte ptr [2AAAh], 055h   ; command to the 29EE010
        mov     ds:byte ptr [5555h], 080h
        mov     ds:byte ptr [5555h], 0AAh
        mov     ds:byte ptr [2AAAh],055h
        mov     ds:byte ptr [5555h], 060h

        call    Delay_10_Micro_Second       ; wait until Tww expires

        mov     al, ds:[0]
        cmp     al, SST_ID                  ; is this a SST part?
        jne     CSC5                        ; NO, then return Carry set
        mov     al,ds:[1]
        cmp     al, SST_29EE010             ; Is it 29EE010?
        jne     CSC5                        ; NO, then Non-SST part
CSC4:
        clc
        pushf                               ; save the result on the STACK
        jmp     short CSC6
CSC5:
        stc                                 ; save the result on the STACK
        pushf
```

```
CSC6:
;
; Issue the Software Product ID Exit code thus returning the 29EE010
; to the read operation mode.
;
        mov     ds:byte ptr [5555h], 0AAh       ; issue the 3-byte product ID
        mov     ds:byte ptr [2AAAh], 055h       ; exit command to the 29EE010
        mov     ds:byte ptr [5555h], 0F0h

        call    Delay_10_Micro_Second           ; wait until Tww expires

        popf                                    ; restore result from the stack
        pop     ds                              ; restore original values
        pop     ax

        ret

Check_SST_29EE010 endp
```

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Software
Drivers

29EE020 / 29LE020 / 29VE020
2 Megabit Page Mode EEPROM

July 1996

29EE020 / 29LE020 / 29VE020
Software Drivers

ABOUT THE SOFTWARE

This application note provides examples software code for controlling page writing by byte SST's 29EE020 2 Mbit Page Mode EEPROM. Two programming languages are provide: high -level "C" for broad platform support and an optimized 8086 assembly language. In many cases, the software driver routines can be inserted "as is" into the main body of code being developed by the system software engineers. Extensive comments are included in each routine to facilitate adapting to code to specific applications. "C" language code can be used with many microprocessors and microcontrollers, while the 8086 assembly language code provides an solution optimized for 8086 assembly language code provides an solution optimized for 8086 microprocessors and embedded processors.

NOTE:

The 29EE020 is for 5.0 volt applications, the 29LE020 is for 3.0 volts application, and the 29VE020 is for 2.7 volt applications. Device functionality is identical for application of this software. For convenience, only the 29EE020 will be referenced in the example codes provided.

ABOUT THE 29EE010

Companion product datasheets for the 29EE020 should be reviewed in conjunction with this application note for a complete understanding of the device.

Writing the 29EE020 can be accomplished with two different algorithms: The first and recommended method employs the JEDEC approved "enable software protection page write" (SDP) algorithm. Using this method, any write operation (128 bytes) requires the inclusion of a series of three byte-load operations, which precede the data loading operation. The three byte-load sequence enables the SDP option during page write operation. SDP provides optimal protection from inadvertent write cycles, e.g., those triggered by noise during the system power-up or power-down. After the initial data byte-load cycle, the host must continue to load a byte into the page buffer within the byte-load cycle time (T_{BLC}) of 100µs for the 29EE020 to stay in the page load cycle. Additional bytes can then be loaded within the same page, in any order, The page load cycle will terminate if no additional byte is loaded into the page buffer within 200 µs (T_{BLCO}) from the last byte-load cycle, i.e. no subsequent WE# high-to-low transition after the last rising edge of WE#.

Both the C and 8086 assembly code in the document contain the following routines, in this order:

Name	Function
Write_29EE020	Alter data
Check_Toggle_Ready	End of write detection using Toggle bit
Check_Data_Polling	End of write detection using Data# polling
Enable_Chip_Data_Protection	Enable JEDEC standard software data protection
Check_SST_29EE020	Check manufacturer and device ID

"C" LANGUAGE DRIVERS

```
/*****************************************************************************************************/
/* Copyright Silicon Storage Technology, Inc. (SST), 1994-1996                                       */
/* Example "C" language Driver of 29EE020 2 Mbit Page Mode EEPROM                                    */
/* Chi Chung Yin, Silicon Storage Technology                                                         */
/*                                                                                                   */
/* Revision 1.0, May 1, 1996                                                                         */
/*                                                                                                   */
/* This file requires these external "timing"  routines:                                             */
/*                                                                                                   */
/*       1.) Delay_1_Milli_Second                                                                    */
/*       2.) Delay_10_Milli_Second                                                                   */
/*       3.) Delay_10_Micro_Second                                                                   */
/*****************************************************************************************************/

#define FALSE                   0
#define TRUE                    (~FALSE)

#define ROW_SIZE                128             /* Must be 128 bytes for 29EE020  */

#define SST_ID                  0xBF            /* SST Manufacture's ID code */
#define SST_29EE020             0x10            /* SST 29EE020 device code */

typedef unsigned char           BYTE;

/*-------------------------------------------------------------------------*/
/*                  EXERNAL ROUTINES                                       */
/*-------------------------------------------------------------------------*/

extern void     Delay_1_Milli_Second();
extern void     Delay_10_Milli_Second();
extern void     Delay_10_Micro_Second();
extern void     Check_Toggle_Read(BYTE far *);
extern void     Check_Data_Polling(BYTE far *, BYTE);
```

```
/*****************************************************************************************************/
/* PROCEDURE:                    Write_29EE020                                                       */
/*                                                                                                   */
/* This procedure can be used to write a total of 128 bytes at one write cycle to the                */
/* SST's 29EE020.                                                                                    */
/*                                                                                                   */
/* Input:                                                                                            */
/*        SRC    SOURCE address containing the data which will be                                    */
/*               written into the 29EE020.                                                           */
/*        Dst     DESTINATION address which will be written with the                                 */
/*                data passed in from ds:si                                                          */
/*                                                                                                   */
/* Out put:                                                                                          */
/*          None                                                                                     */
/*****************************************************************************************************/

void Write_29EE020 (BYTE far *Src,    BYTE far *Dst)
{
        BYTE far *Temp;
        BYTE far *SourceBuf;
        BYTE far *DestBuf;
        int Index;

        SourceBuf = Src;
        DestBuf = Dst;

        /*************************************************************************************/
        /*                              WRITTEN OPERATION                                    */
        /*                                                                                   */
        /* Issue the 3-byte "enable protection" sequence followed by 128 bytes               */
        /* of data written to the 29EE020.                                                   */
        /*************************************************************************************/

        Temp =  (BYTE far *)0xC0005555;      /* set up address to be C000:555h      */
         *Temp = 0xAA;                       /* write data 0xAA to the address      */
        Temp =  (BYTE far *)0xC0002AAA;      /* set up address to be C000:2AAAh     */
         *Temp = 0x55;                       /* write data 0x55 to the address      */
        Temp =  (BYTE far *)0xC0005555;      /* set up address to be C000:5555h     */
         *Temp = 0xA0;                       /* write data 0xA0 to the address      */

         for (Index = 0; Index < ROW_SIZE; Index++)
         {
                 *DestBuf++ = *SourceBuf++;    /* transfer data from source to destination */

         }
         Delay_1_Milli_Second();         /* wait 1ms to start writing                */

         Check_Toggle_Ready(Dst);    /* wait for TOGGLE bit to get ready       */
}
```

```
/*****************************************************************************************************/
/* PROCEDURE:                    Check_Toggle_Ready                                                  */
/*                                                                                                   */
/* During the internal write cycle, any consecutive read operation                                   */
/* on DQ6 will produce alternating 0's and 1's i.e. toggling between                                 */
/* 0 and 1.  When the write cycle is completed, DQ6 of the data will                                 */
/* stop toggling.  After the DQ6 data bit stops toggling, the device is ready                        */
/* for next operation.                                                                               */
/*                                                                                                   */
/* Input:                                                                                            */
/*        Dst             must already set-up by the caller                                          */
/*                                                                                                   */
/* Output:                                                                                           */
/*        None                                                                                       */
/*****************************************************************************************************/

void Check_Toggle_Ready (BYTE far  *Dst)
{
        BYTE Loop = TRUE;
        BYTE PreData;
        BYTE CurrData;
        unsigned long TimeOut = 0;

        PreData = *Dst;
        PreData = PreData & 0x40;
        while ((Timeout< 0x07FFFFFF) && (Loop))
        {
                CurrData = *Dst;
                CurrData = CurrData & 0x40;
                if (PreData == CurrData)
                        Loop = FALSE;           /* ready to exit the while loop */
                PreData = CurrData;
                TimeOut++;
        }
}
```

```
/*****************************************************************************************************/
/* PROCEDURE:                    Check_Data_Polling                                                  */
/*                                                                                                   */
/* During the internal write cycle, any attempt to read DQ7 of the last byte loaded during           */
/* the page/byte-load cycle will receive the complement of the true data.  Once the                  */
/* write cycle is completed, DQ7 will show true data.                                                */
/*                                                                                                   */
/* Input:                                                                                            */
/*        Dst             must already set-up by the caller                                          */
/*        TrueData        this is the original (true) data                                           */
/*                                                                                                   */
/* Output:                                                                                           */
/*        None                                                                                       */
/*****************************************************************************************************/

void Check_Data_Polling (BYTE FAR  *Dst,        BYTE TrueData)
{
        BYTE Loop = TRUE;
        BYTE CurrData;
        unsigned long TimeOut = 0;

        TrueData = TrueData &  0x80;
        while ((Timeout< 0x07FFFFFF) && (Loop))
        {
                CurrData = *Dst;
                CurrData = CurrData & 0x80;
                if (TrueData == CurrData)
                        Loop = FALSE;           /* ready to exit the while loop  */
                TimeOut++;
        }
}
```

```
/*****************************************************************************************************/
/* PROCEDURE:                Enable_Chip_Data_Protection                                             */
/*                                                                                                   */
/* This procedure ENABLES the data  protection feature on the 29EE020                                */
/* 2 Mbit Page Mode EEPROM.  After calling this routine, the chip cannot be written                  */
/* unless preceded by the three Byte-Load sequence.                                                  */
/*                                                                                                   */
/* Input:                                                                                            */
/*        None                                                                                       */
/*                                                                                                   */
/* Output:                                                                                           */
/*        None                                                                                       */
/*****************************************************************************************************/

void Enable_Chip_Data_Protection()
{
        BYTE  far  *Temp;

        Temp  = (BYTE far *)0xC0005555;      /* set up address to be C000:5555h     */
        *Temp = 0xAA;                        /* write data 0xAA to the address      */
        Temp  = (BYTE far *)0xC0002AAA;      /* set up address to be C000:2AAAh     */
        *Temp = 0x55;                        /* write data ox55 to the address      */
        Temp  = (BYTE far *)0xC0005555;      /* set up address to be C000:5555h     */
        *Temp = 0xA0;                        /* write data 0xA0 to the address      */

        Delay_10_Milli Second();
}
```

```
/*****************************************************************************************************/
/* PROCEDURE:                    Check_SST_29EE020                                                   */
/*                                                                                                   */
/* This procedure  decides whether a  physical hardware device has a SST                             */
/* 29EE020 2 Mbit Page Mode EEPROM installed or not.                                                 */
/* without using the three Byte-Load sequence.                                                       */
/*                                                                                                   */
/* Input:                                                                                            */
/*        None                                                                                       */
/*                                                                                                   */
/* Output:                                                                                           */
/*        return -1:  indicates not a SST 29EE020                                                    */
/*        return 0:   indicates is    a SST 29EE020                                                  */
/*****************************************************************************************************/

int Check_SST_29EE020()
{
        BYTE far  *Temp;
        BYTE SST_id1;
        BYTE SST_id2;
        int    ReturnStatus;

        /*  Issue the Software Product ID code to 29EE020   */

        Temp  = (BYTE far *)0xC0005555;       /* set up address to be C000:5555h     */
        *Temp = 0xAA;                         /* write data 0xAA to the address      */
        Temp  = (BYTE far *)0xC0002AAA;       /* set up address to be C000:2AAAh     */
        *Temp = 0x55;                         /* write data ox55 to the address      */
        Temp  = (BYTE far *)0xC0005555;       /* set up address to be C000:5555h     */
        *Temp = 0x90;                         /* write data 0x80 to the address      */

        Delay_10_Milli Second();

        /* Read the product ID from 29EE020 */

        Temp  = (BYTE far *)0xC0000000;       /* set up address to be C000:0000h     */
        SST_id1  =  *Temp;                    /* get first ID byte                   */
        Temp  =  (BYTE far *)0xC0000001;      /* set up address to be C000:0001h     */

        if ((SST_id1 == SST_ID) && (SST_id2 ==SST_29EE020))
                ReturnStatus = 0;
        else
                ReturnStatus = -1;
```

```
        /* Issue the Soffware Product ID Exit code thus returning the 29EE020      */
        /* to the read operating mode                                              */

        Temp  = (BYTE far *)0xC0005555;     /* set up address to be C000:5555h     */
        *Temp = 0xAA;                       /* write data 0xAA to the address      */
        Temp  = (BYTE far *)0xC0002AAA;     /* set up address to be C000:2AAAh     */
        *Temp = 0x55;                       /* write data 0x55 to the address      */
        Temp  = (BYTE far *)0xC0005555;     /* set up address to be C000:5555h     */
        *Temp =0xF0;                        /* write data 0xF0 to the address      */

        Delay_10_Milli Second();

        return(ReturnStatus);
}
```

8086 ASSEMBLY LANGUAGE DRIVERS

```
; ============================================================================
; Copyright Silicon Storage Technology, Inc. (SST), 1994-1996
; EXAMPLE 8086 assembly Drivers for 29EE020 2 Mbit Page Mode EEPROM
; Chi Chung Yin,  Silicon Storage Technology
;
; Revision 1.0, Mayt 1, 1996
;
; This file requires these external "timing" routines:
;
;       1.) Delay_1_Milli_Second
;       2.) Delay_10_Milli_ Second
;       3.) Delay_10_Micro_Second
; ============================================================================

ROW_SIZE            EQU   128               ;Must be 128 bytes for 29EE020

SST_ID              EQU   0BFh              ;SST Manufacture's ID code
SST_29EE020         EQU   010h              ;SST 29EE020 internal code

ABS_SEGMENT         EQU   0E000h

extrn   Delay_1_Milli_Second:near
extrn   Delay_10_Milli_Second:near
extrn   Delay_10_Micro_Second:near
```

```
; ============================================================================
; PROCEDURE:                    Write_29EE020
;
; This procedure can be used to write a total of 128 bytes at one write cycle to the
; SST's 29EE020.
;
; Input:
;       ds:si   SOURCE address containing the data which will be
;               written into the 29EE020.
;       es:di   DESTINATION address which will be written with the
;               data passed in for ds;si
;
; Output:
;       None
;       SI, DI:  Contains the original values
; ============================================================================

Write_29EE020           proc    near

        push    ax
        push    bx
        push    cx
        push    di
        push    si
        push                    ; preserve the "Direction" flag in the FLAG
                                ; register

        cld                     ; clear "Direction" flag in the FLAG register
                                ; auto-increment SI, and DI

; ============================================================================
;                               WRITE OPERATION
; Let's issue the 3-byte "Enable Protection" sequence to the 29EE020
; chip followed by the 128 bytes of data.
; ============================================================================

        push    ax
        push    ds

        mov     as, ABS_SEGMENT
        mov     ds, ax
        mov     ds:byte ptr [5555h], 0aah; 3 bytes of  "enable protection"
        mov     ds:byte ptr [2AAAh], 055h       ; sequence to the chip
        mov     ds:byte ptr [5555h], 0A0h

        pop     ds
        pop     ax

        mov     cx,  ROW_SIZE           ; we will write 128 bytes
        push    si                      ; save original values
        push    di
```

```
        cli                             ; no disturb allowed while in the process
                                        ; of writing the 29EE020.
DRP1:
        lodsb                           ; do not use " rep movsb" instruction
        stosb                           ;
        loop    DRP1                    ; write 128 bytes

        call    Delay_1_Milli Second    ; wait 1ms to start writing
        pop     di                      ; restore original values
        pop     si
        call    check_Toggle_Ready      ; wait for TOGGLE bit to get ready

        popf
        pop     si
        pop     di
        pop     cx
        pop     bx
        pop     ax

        ret

Wrtie_29EE020           endp
```

```
;=============================================================================
; PROCEDURE:                    Check_Toggle_Ready
;
; During the internal write cycle, any consecutive read operation
; on DQ6 will produce alternating 0's and 1's, i.e. toggling between
; 0 and 1. When the write cycle is completed, the DQ6 data will
; stop toggling. After the DQ6 data stops toggling, the device is ready
; for the next operation.
;
; Input::
;       es:di    must already set-up by the calller
;
; Output:
;       None
;=============================================================================

Check_Toggle_Ready   proc    near

        push    ax

        mov     al, es:[di]             ; read a byte form the chip
        and     al,40h                  ; mask out the TOGGLE bit (DQ6)
CTR_Tog2:
        mov     ah, es:[di]             ; read the same byte from the chip again
        and     ah, 40h                 ; mask out the TOGGLE bit (DQ6)
        cmp     al, ah                  ; is DQ6 still toggling?
        je      CTR_T0g3                ; No, then the write operation is done
        xchg    ah, al                  ; YES, then continue chicking...
        jmp     short CTR_Tog2
CTR_Tog3:
        pop     ax

        ret

Check_Toggle_Ready   endp
```

```
;===============================================================================
; PROCEDURE:                    Check_Data_Polling
;
; During the internal write cycle, any attemp to read DQ7 of the last byte loaded during
; the page/byte-load cycle will receive the complement of the true data.  Once the
; write cycle is completed, DQ7 will show  true data.
;
; Input:
;       es:di    must already set-up by the caller
;       bl       contains the original (true) data
;
; Output:
;       None
;
;===============================================================================

Check_Data_Polling      proc    near

        push    ax

        an      bl, 80h                 ; mask out the DQ7 bit
CDP_Tog2:
        mov     al, es:[di]             ; read a byte from the chip
        and     al,80h                  ; mask out the DQ7 bit
        camp    al,bl                   ; is DQ7 still complementing?
        jne     CDP Tog2

        pop     ax

        ret

Check_Data_Polling      endp
```

```
;=============================================================================
; PROCEDURE:                    Enable_Chip_Data_Protection
;
; This procedure ENABLES the data protection feature on the 29EE020
; 2 Mbit Page Mode EEPROM.  After calling the routine, the chip can be written
; without using the three Byte-Load sequence.
;
; Input::
;       None
;
; Output:
;       None
;=============================================================================

Disable_Chip_Data_Protection   proc    near

        push    ax                              ; preserve registers' value
        push    ds

        cli
        mov     ax, ABS_SEGMENT
        mov     ds, ax

        mov     ds:byte ptr [5555h], 0AAh       ; issue the 3-byte protect
        mov     ds:byte ptr [2AAAh], 055h       ; sequence to the 29EE020
        mov     ds:byte ptr [5555h], 0A0h

        call    Delay_10_Milli_Second

        pop     ds
        pop     ax

        ret

Enable_Chip_Data_Protection endp
```

```
;=============================================================================
; PROCEDURE:                    Check_SST_29EE020
;
; This procedure decides whether a physical hardware device has a SST's
; 29EE020 2 Mbit Page Mode EEPROM installed or not.
;
; Input:
;       None
;
; Output:
;       carry bit:  SET means not a SST 29EE020
;       carry bit:  CLEARED means a SST 29EE020
;
;=============================================================================

Check_SST_29EE020   proc    near

        push    ax                          ; preserve registers' value
        push ds

        cli
        mov     ax, ABS_SEGMENT
        mov     ds, ax

        mov     ds:byte ptr [5555h], 0AAh   ; issue the 6-byte product ID
        mov     ds:byte ptr [2AAAh], 055h   ; command to the 29EE020
        mov     ds:byte ptr [5555h], 090h

        call    Delay_10_Micro_Second       ; wait until Tww expires

        mov     al, ds:[0]
        cmp     al, SST_ID                  ; is this a SST part?
        jne     CSC5                        ; NO, then return Carry set
        mov     al,ds:[1]
        cmp     al, SST_29EE020             ; Is it 29EE020?
        jne     CSC5                        ; NO, then Non-SST part
CSC4:
        clc
        pushf                               ; save the result on the STACK
        jmp     short CSC6
CSC5:
        stc                                 ; save the result on the STACK
        pushf
```

```
CSC6:
;
; Issue the Software Product ID Exit code thus returning the 29EE020
; to the read operation mode.
;
        mov     ds:byte ptr [5555h], 0AAh       ; issue the 3-byte product ID
        mov     ds:byte ptr [2AAAh], 055h       ; exit command to the 29EE020
        mov     ds:byte ptr [5555h], 0F0h

        call    Delay_10_Micro_Second           ; wait until Tww expires

        popf                                    ; restore result from the stack
        pop     ds                              ; restore original values
        pop     ax

        ret

Check_SST_29EE020 endp
```

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Software
Drivers

28SF040 / 28LF040 / 28VF040
4 Megabit SuperFlash EEPROM

July 1996

28SF040 / 28LF040 / 28VF040
Software Drivers

ABOUT THE SOFTWARE

This application note provides examples software code for controlling sector erasing and byte writing SST's 28SF040 4 Mbit SuperFlash EEPROM. Two programming languages are provide: high-level "C" for broad platform support and an optimized 8086 assembly language. In many cases, the software driver routines can be inserted "as is " into the main body of code being developed by the system software engineers. Extensive comments are included in each routine to facilitate adapting to code to specific applications. "C" language code can be used with many microprocessors and microcontrollers, while the 8086 assembly language code provides an solution optimized for 8086 microprocessors and embedded processors.

NOTE:

The 28SF040 is for 5 volt applications, the 28LF040 is for 3.0 volt applications, and the 28VF040 is for 2.7 volt applications. Device functionality is identical for application of this software. For convenience, only the 28SF040 will be referenced in the example codes provided.

ABOUT THE 28SF040

Companion product datasheets for the 28SF040 should be reviewed in conjunction with this application note for a complete understanding of the device.

The 28SF040 features high performance program and sector (256 bytes) erase capability. A command register is incorporated on chip to facilitate interface and control of the 28SF040. Device Read, Erase, Program, and other essential operations are accomplished via the command register. Commands are written to the command register using standard microprocessor write timings. The register contents serve as input to an internal state machine, which controls the erase and program circuitry. Address and data are latched for program and erase operations. The command register does not occupy an addressable memory location. It is a latch used to store the command, along with address and data information needed to execute the command.

Provisions are made to prevent inadvertent writes through a software approach. In order to perform the functions of page erase or program, users must issue a series of seven byte-read sequence to the 28SF040 to unprotect the chip. After the device is unprotected, users can then erase and program the device. Prior to programming the sector (256 bytes), it must be erased first. After the erase operation, programming are done on a byte-by-byte basis for a total of 256 bytes. The end of each byte program cycle can be detected by two means, namely by monitoring either DATA# Polling or Toggle Bit.

Both the C and 8086 assembly code in the document contain the following routines, in this order:

Name	Function
Write_28SF040	Alter data
Check_Toggle_Ready	End of write detection using Toggle bit
Check_Data_Polling	End of write detection using Data# polling
Disable_Chip_Data_Protection	Diables software data protection
Enable_Chip_Data_Protection	Enable software data protection
Check_SST_28SF040	Check manufacturer and device ID

"C" LANGUAGE DRIVERS

```
/*****************************************************************************************************/
/* Copyright Silicon Storage Technology, Inc. (SST), 1994, 1995                                      */
/* Example "C" language Driver of 28SF040 4 Mbit SuperFlash EEPROM                                   */
/* Chi Chung Yin, Silicon Storage Technology                                                         */
/*                                                                                                   */
/* Revision 1.0, August 1, 1994                                                                      */
/*                                                                                                   */
/*****************************************************************************************************/

#define FALSE           0
#define TRUE            (~FALSE)

#define ROW_SIZE        256         /* Must be 256 bytes for 28SF040  */

#define SST_ID          0xBF        /* SST Manufacture's ID code */
#define SST_28SF040     0x04        /* SST 28SF040 device code */

#define AUTO_PG_ERASE1  0x20
#define AUTO_PG_ERASE2  0xD0
#define AUTO_PGRM       0x10
#define RESET           0xFF
#define READ_ID         0x90

typedef unsigned char   BYT


void    Check_Toggle_Read(BYTE far *);
void    Check_Data_Polling(BYTE far *, BYTE);
```

```
/*****************************************************************************************************/
/* PROCEDURE:                          Program_28SF040                                               */
/*                                                                                                   */
/* This procedure can be used to write a total of 256 bytes at one write cycle to the                */
/* SST's 28SF040 4 Mbit SuperFlash EEPROM.                                                           */
/*                                                                                                   */
/* Input:                                                                                            */
/*        SRC    SOURCE address containing the data which will be                                    */
/*               written into the 28SF040.                                                           */
/*        Dst    DESTINATION address which will be written with the                                  */
/*               data passed in from ds:si                                                           */
/*                                                                                                   */
/* Output:                                                                                           */
/*        return - 1 : indicates an error in programming the 28SF040                                 */
/*        return - 0 : indicates no error in programming the 28SF040                                 */
/*****************************************************************************************************/

int Program_28SF040 (BYTE far *Src,   BYTE far *Dst)
{
        BYTE far *Temp;
        BYTE far *SourceBuf;
        BYTE far *DestBuf;
        int Index;
        int Count;
        BYTE SourceByte;
        BYTE ProgrammedBYTE;
        BYTE Continue

        SourceBuf = Src;
        DestBuf = Dst;

        /*************************************************************************************/
        /*                          ERASE OPERATION                                          */
        /*                                                                                   */
        /*************************************************************************************/

        *DestBuf = AUTO_PG_ERASE1;          /* erase the page before programming */
        *DestBuf = AUTO_PG_ERASE2;
        Check_Toggle_Ready(Dst);            /* wait for Toggle bit ready */

        Count = 0;
        Continue = TRUE;
         while ((Count < ROW_SIZE) && (Continue))
        {
                SourceByte = * DestBuf++;
                 if (SourceByte == 0xFF)
                        Count++;
                 else
                        Continue =  FALSE;
        }
        if (!Continue)
           return(TRUE);                    /* return with error */
```

```
/*****************************************************************************************************/
/*                              PROGRAM  OPERATION                                                   */
/*                                                                                                   */
/*****************************************************************************************************/

SourceBuf = Src;
DestBuf = Dst;

for (Index = 0; Index < ROW_SIZE; Index++)
{
        SourceByte = *SourceBuf++;
        if (SourceByte != 0xFF)             /* If the data is 0xFF, don't program it*/
        {

                *DestBuf = AUTO_PGRM;       /*issue AUTO PROGRAM command*/
                *DestBuf = SourceByte;       /* program the data */
                Check_Toggle_Ready(Dst);     /* wait for Toggle bit ready */
                 ProgrammedByte = *DestBuff++; /* read back the data pragrammed */
                 if (SourceByte != ProgrammedByte)
                 {
                         Continue = FALSE;
                          Break;
                 }
        }
}
if (!Continue)
        return(TRUE);                       /* return with error */
else
        return(TURE);                       /* return with NO error */
}
```

```
/*****************************************************************************************************/
/*PROCEDURE:                    Check_Toggle_Ready                                                   */
/*                                                                                                   */
/*During the internal write cycle, any consecutive read operation                                    */
/*on DQ6 will produce alternating 0's and 1's i.e. toggling between                                  */
/* 0 and 1.  When the write cycle is completed, DQ6 of the data  will                                */
/* stop toggling.  After the DQ6 data bit  stops toggling, the device is ready                       */
/* for next operation.                                                                               */
/*                                                                                                   */
/* Input:                                                                                            */
/*        Dst      must  already set-up by the caller                                                */
/*                                                                                                   */
/* Output:                                                                                           */
/*        None                                                                                       */
/*****************************************************************************************************/

void Check_Toggle_Ready (BYTE far *Dst)
{
        BYTE Loop = TRUE;
        BYTE PreData;
        BYTE CurrData;
        unsigned long TimeOut = 0;

        PreData = *Dst;
        PreData = PreData & 0x40;
        while ((Timeout< 0x07FFFFFF) && (Loop))
        {
                CurrData = *Dst;
                CurrData = CurrData & 0x40;
                if (PreData == CurrData)
                        Loop = FALSE;           /* ready to exit the while loop */
                PreData = CurrData;
                TimeOut++;
        }
}
```

```
/*****************************************************************************************************/
/* PROCEDURE:                    Check_Data_Polling                                                  */
/*                                                                                                   */
/* During the internal write cycle, any attempt to read DQ7 of the byte loaded during                */
/* the byte-load cycle will receive the complement of the true data. Once the write                  */
/* cycle is completed, DQ7 will show true data.                                                      */
/*                                                                                                   */
/* Input:                                                                                            */
/*       Dst             must already set-up by the caller                                           */
/*       TrueData        this is the original (true) data                                            */
/*                                                                                                   */
/* Output:                                                                                           */
/*       None                                                                                        */
/*****************************************************************************************************/

void Check_Data_Polling (BYTE FAR  *Dst,        BYTE TrueData)
{
        BYTE Loop = TRUE;
        BYTE PreData;
        BYTE CurrData;
        unsigned long TimeOut = 0;

        TrueData = TrueData &  0x80;
        while ((Timeout< 0x07FFFFFF) && (Loop))
        {
                CurrData = *Dst;
                CurrData = CurrData & 0x80;     /* mask out the DQ7 bit */
                if (TrueData == CurrData)
                        Loop = FALSE;           /* ready to exit the while loop  */
                TimeOut++;
        }
}
```

```
/*****************************************************************************************************/
/*PROCEDURE:                Disable_Chip_Data_Protection                                             */
/*                                                                                                   */
/* This procedure DISABLES the data  protection feature on the 28SF040                               */
/* 4 Mbit SuperFlash EEPROM.  After calling this routine, the chip can be written                    */
/*  without any additional commands.                                                                 */
/*                                                                                                   */
/* Input:                                                                                            */
/*        None                                                                                       */
/*                                                                                                   */
/* Output:                                                                                           */
/*        None                                                                                       */
/*****************************************************************************************************/

void Disable_Chip_Data_Protection()
{
        BYTE  far  *Temp;
        BYTE    TempByte;

        Temp  = (BYTE far *)0xE0001823;      /* set up address to be E000:1823h    */
        TempByte = *Temp;                    /* read data from the address         */
        Temp  = (BYTE far *)0xE0001820;      /* set up address to be E000:1820h    */
        TempByte = *Temp;                    /* read data from the address         */
        Temp  = (BYTE far *)0xE0001822;      /* set up address to be E000:1822h    */
        TempByte = *Temp;                    /* read data from the address         */
        Temp  = (BYTE far *)0xE0000418;      /* set up address to be E000:0418h    */
        TempByte = *Temp;                    /* read data from the address         */
        Temp  = (BYTE far *)0xE000041B;      /* set up address to be E000:041Bh    */
        TempByte = *Temp;                    /* read data from the address         */
        Temp  = (BYTE far *)0xE0000419;      /* set up address to be E000:0419h    */
        TempByte = *Temp;                    /* read data from the address         */
        Temp =  (BYTE far *)0xE000041A;      /* set up address to be E000:041Ah    */
        TempByte = *Temp;                    /* read data from the address         */

}
```

```
/*****************************************************************************************************/
/*PROCEDURE:                Enable_Chip_Data_Protection                                              */
/*                                                                                                   */
/* This procedure ENABLES the data  protection feature on the 28SF040                                */
/* 4 Mbit SuperFlash EEPROM. After calling this routine, the chip cannot be written                  */
/*  without disabling SDP first. Disabling the SDP can be done by calling the                        */
/*  "Disable_Chip_Data_Protection" routine.                                                          */
/*                                                                                                   */
/* Input:                                                                                            */
/*       None                                                                                        */
/*                                                                                                   */
/* Output:                                                                                           */
/*       None                                                                                        */
/*****************************************************************************************************/

void Enable_Chip_Data_Protection()
{
        BYTE  far  *Temp;
        BYTE TempByte;

        Temp  = (BYTE far *)0xE0001823;      /* set up address to be E000:1823h    */
        TempByte = *Temp;                    /* read data from the address         */
        Temp  = (BYTE far *)0xE0001820;      /* set up address to be E000:1820h    */
        TempByte = *Temp;                    /* read data from the address         */
        Temp  = (BYTE far *)0xE0001822;      /* set up address to be E000:1822h    */
        TempByte = *Temp;                    /* read data from the address         */
        Temp = (BYTE far *)0xE0000418;       /* set up address to be E000:0418h    */
        TempByte = *Temp;                    /* read data from the address         */
        Temp = (BYTE far *)0xE000041B;       /* set up address to be E000:041Bh    */
        TempByte = *Temp;                    /* read data from the address         */
        Temp = (BYTE far *)0xE0000419;       /* set up address to be E000:0419h    */
        TempByte = *Temp;                    /* read data from the address         */
        Temp = (BYTE far *)0xE000040A;       /* set up address to be E000:040h     */
        TempByte = *Temp;                    /* read data from the address         */
}
```

```
/*****************************************************************************************************/
/*PROCEDURE:                    Check_SST_28SF040                                                    */
/*                                                                                                   */
/* This procedure  decides whether a  physical hardware device has a SST                             */
/* 28SF040 4 Mbit SuperFlash EEPROM installed or not..                                               */
/*                                                                                                   */
/* Input:                                                                                            */
/*       None                                                                                        */
/*                                                                                                   */
/* Output:                                                                                           */
/*       return -1:  indicates no SST 28SF040 installed                                              */
/*       return 0:   indicates a SST 28SF040 is installed                                            */
/*****************************************************************************************************/

int Check_SST_28SF040()
{
        BYTE far  *Temp;
        BYTE SST_id1;
        BYTE SST_id2;
        int   ReturnStatus;
        BYTE OriginalByte;

        Temp  = (BYTE far *)0xE0000000;
        OriginalByte = *Temp;                   /* save the original memory contents   */
        *Temp = RESET;                          /* reset tje 28SF040 chip first        */
        *Temp = READ_ID;                        /* issue the READ_ID command           */

        Temp  = (BYTE far *)0xE0000000;         /* set up address to be E000:0000h     */
        SST_id1 = *Temp                         /* get first ID byte                   */
        Temp  = (BYTE far *)0xE0000001;         /* set up address to be E000:0001h     */
        SST_id2 = *Temp;                        /* get second ID byte                  */

        If ((SST_id1 == SST_ID) && (SST_id2 == SST_28SF040))
                ReturnStatus = 0;
        else
                ReturnStatus = -1;
        Temp  = (BYTE far *)0xE0000000;
        *Temp = RESET;                          /* issue RESET command to 28SF040   */
        if (ReturnStatus ==-1)
                *Temp = OriginalByte;           /* if not 28SF040, restore original contents  */

        return(ReturnStatus);

}
```

8086 ASSEMBLY LANGUAGE DRIVERS

```
; ======================================================================
 ; Copyright Silicon Storage Technology, Inc. (SST), 1994, 1995
; EXAMPLE 8086 assembly Drivers for 28SF040 4 Mbit SuperFlash EEPROM
;  Chi Chung Yin,  Silicon Storage Technology
;
; Revision 1.0, August 1, 1994
;======================================================================

ROW_SIZE          EQU   256          ;Must be 256bytes for 28SF040

SST_ID            EQU   0BFh         ;SST Manufacture's ID code
SST_28SF040       EQU   004h         ;SST 28SF040 internal code

AUTO_PG_ERASE1    EQU   020h
AUTO_PG_ERASE2    EQU   0D0h
AUTO_PGRM         EQU   010h
RESET             EQU   0FFh
READ_ID           EQU   090h

ABS_SEGMENT       EQU   0E000h
```

```
; ============================================================================
; PROCEDURE:                    Program_28SF040
;
; This procedure can be used to write a total of 256 bytes at one write cycle to the
;  28SF040 4 Mbit SuperFlash EEPROM.
;
; Input:
;       ds:si   SOURCE address containing the data which will be
;               written into the 28SF040.
;       es:di   DESTINATION address which will be written with the
;               data passed in for ds;si
;
; Output:
;       carry bit: SET means programming error
;       ;       carry bit: CLEAR means programmed O.K.
;       SI, DI:  Contains the original values
; ============================================================================
Program_28SF040             proc    near

        push    ax
        push    bx
        push    cx
        push    di
        push    si
        push                    ; preserve the "direction" flag in the FLAG
                                ; register
        cld                     ; clear "Direction" flag in the FLAG register
        mov     bx, di          ; save DI value in BX in order to use it from programming

; ============================================================================
;                               WRITE  OPERATION
;============================================================================

        mov     byte ptr es:[di], AUTO_PG_ERASE1    ; let's clear the page first
        mov     byte ptr es:[di}, AUTO_PG_ERASE2
        call    Check_Toggle_Ready  ; make sure the internal hardware finish
                                    ; the clear operation
        mov     cx, ROW_SIZE        ; check 256 bytes to make sure every byte is 0FFh
P2_0:
        mov     al, byte ptr es:[di]    ; read back the byte just eased
        cmp     al, 0ffh                ; is it erased?
        jnz     P2_1
        inc     di
        loop    P2_0
        jmp     short P2_3              ; let's start to program the part
P2_1:
        popf                            ; restore flag register value for stack
        stc                             ; return with error
        jmp     short P2_10
```

```
;-------------------------------------------------------------------------------------------------------
;                                        PROGRAM operation
;-------------------------------------------------------------------------------------------------------
P2_3
        mov     cx, ROW_SIZE            ; program 256 bytes
        mov     di, bx                  ; restore original destination address (DI)
WOS1_4:
        lodsb                           ; get the byte to be written
        comp    al, 0ffh                ; is it 0FFh?
        jz      WOS11_5                 ; yes, no need to program it
        push    as                      ; save the byte on the stack
        mov     byte ptr es:[di], AUTO_PGRM ;  issue the AUTO_PROGRAM command
        mov     byte ptr es:[di], al    ; program the byte
;
; Due to performance reason, we will implement "TOGGLE_BIT" test routine here.
;
        mov     al, byte ptr es:[di}    ; read back the byte just programmed
        and     al, 040h
Tx1:
        mov     ah,byte ptr es:[di]     ; read the same byte again
        and     ah, 040h
        cmp     al, ah                  ; do both reads produce the same result?
        jz      WOS1_5                  ; YES, then done because 'toggle_bit" stops
                                        ; toggling.
        xchg    ah, al                  ; NO, then keep trying until done...
        jmp     short Tx1
WOS1_5:
        pop     ax                      ; restore the byte just programmed
        cmp     al, byte ptr es:[di]    ; is it the same as original?
        je      WOS11_5
        popf                            ; the byte just programmed is NOT the same as
        stc                             ; original, return error to the caller
        jmp     shortP2_10
WOS11_5:
        inc     di
        loop    WOSI_4                  ; program next byte

        popf
        clc                             ; clear Carry bit  to indicate NO error

P2_10:
        pop     si
        pop     di
        pop     cx
        pop     bx
        pop     ax

        ret
Program_28SF040     endp
```

```
;=============================================================================
; PROCEDURE:                          Check_Toggle_Ready
;
; During the internal write cycle, any consecutive read operation
; on DQ6 will produce alternating O's and 1's, i.e. toggling between
; 0 and 1.  When the write cycle is completed, the DQ6 data will
; stop toggling.  After the DQ6 data stops toggling, the device is ready
; for the next operation.
;
; Input:
;       es:di    must already set-up by the calller
;
; Output:
;       None
;=============================================================================

Check_Toggle_Ready   proc    near

        push    ax
        mov     al, es:[di]                 ; read a byte form the chip
        and     al,40h                      ; mask out the TOGGLE bit (DQ6)
CTR_Tog2:
        mov     ah,es:[di]                  ; read the same byte from the chip again
        and     ah, 40h                     ; mask out the TOGGLE BIT (DQ6)
        cmp     al, ah                      ; is DQ6 still toggling?
        je      CTR_Tog3                    ; NO, then the programming is done
        xchg    ah, al                      ; YES, then continue checking...
        jmp     short CTR_Tog2
CTR_Tog3:
        pop     ax

        ret

Check_Toggle_Ready   endp
```

```
;=============================================================================
; PROCEDURE:                    Check_Data_Polling
;
; During the internal write cycle, any attemp to read DQ7 of the last byte loaded during
; the page/byte-load cycle will receive the complement of the true data.  Once the
; write cycle is completed, DQ7 will show  true data.
;
; Input:
;       es:di     must  already set-up  by the caller
;       bl        contains the original (true) data
;
; Output:
;       None
;=============================================================================

Check_Data_Polling      proc    near

        push    ax

        an      bl, 80h                 ; mask out the DQ7 bit
CDP_Tog2:
        mov     al, es:[di]             ; read a byte from the chip
        and     al,80h                  ; mask out the DQ7 bit
        camp    al,bl                   ; is DQ7 still complementing?
        jne     CDP_Tog2

        pop     ax

        ret

Check_Data_Polling      endp
```

```
;=============================================================================
; PROCEDURE:                    Disable_Chip_Data_Protection
;
;This procedure DISABLES the data protection feature on the 28SF040
;4 Mbit SuperFlash EEPROM.  After calling the routine, the chip can be written
; without  any additional commands.
;
; Input:
:         None
;
; Output:
;         None
;=============================================================================

Disable_Chip_Data_Protection   proc     near

        push    ax
        push    ds

        cli
        mov     ax, ABS_SEGMENT
        mov     ds, ax

        mov     al, byte ptr ds:[1823h]         ; issue the 7-byte read sequences to the chip
        mov     al, byte ptr ds:[1820h]         ; to unprotect the chip
        mov     al, byte ptr ds:[1822h]
        mov     al, byte ptr ds:[0418h]
        mov     al, byte ptr ds:[041Bh]
        mov     al, byte ptr ds:[0419h]
        mov     al, byte ptr ds:[041Ah]

        pop     ds
        pop     ax

        ret

Disable_Chip_Data_Protection endp
```

```
;=============================================================================
; PROCEDURE:          Enable_Chip_Data_Protection
;
;This procedure ENABLES the data protection feature on the 28SF040
;4 Mbit SuperFlashEEPROM.  After calling the routine, the chip cannot be written
; without disabling SDP first.  Disabling the SDP can be done by call ing the
; "Disable_Chip_Data_Protection" routine.
;
; Input::
:       None
;
; Output:
;       None
;=============================================================================

Enable_Chip_Data_Protection    proc    near

        push    ax
        push    ds

        cli
        mov     ax, ABS_SEGMENT
        mov     ds, ax

        mov     al, byte ptr ds:[1823h]         ; issue the 7-byte read sequences to the chip
        mov     al, byte ptr ds:[1820h]         ; to protect the chip from inadvertent program
        mov     al, byte ptr ds:[1822h]         ; operations
        mov     al, byte ptr ds:[0418h]
        mov     al, byte ptr ds:[041Bh]
        mov     al, byte ptr ds:[0419h]
        mov     al, byte ptr ds:[040Ah]

        pop     ds
        pop     ax

        ret

Enable_Chip_Data_Protection endp
```

```
;=====================================================================
; PROCEDURE:                    Check_SST_28SF040
;
; This procedure decides whether a physical hardware device has a SST's
; 28SF040 4 Mbit SuperFlash EEPROM installed or not.
;
; Input:
;       None
;
; Output:
;       carry bit:  SET means no SST 28SF040 installed
;       carry bit:  CLEARED means a SST 28SF040 is installed
;=====================================================================

Check_SST_28SF040   proc    near

        push    ax
        push    bx
        push    ds

        cli
        mov     ax, ABS_SEGMENT
        mov     ds, ax
        mov     bl, ds:byte ptr [0]         ; save original memory content
        mov     ds:byte ptr [0h], RESET; reset the 28SF040 chip
        mov     ds:byte ptr [0h], READ_ID       ; issue READ_ID command to the chip
;
;Now, Check the SST 28SF040 Manufacture's ID and Internal Die Code
;
        mov     al, ds:byte ptr[0]
        cmp     al, SST_ID                      ; is this a SST part?
        jne     CSC5                            ; NO, then return Carry set
        mov     al,ds:byte ptr[1]
        cmp     al, SST_28SF040                 ; Is it 28SF040?
        jne     CSC5                            ; NO, then Non-SST part
CSC4:
        mov     ds:byte ptr [0], RESET          ; issure RESET command to the chip
        clc                                     ; return with NO error
        jmp     short CSC6
CSC5:
        mov     ds:byte ptr [0], RESET          ; issue RESET command to the chip
        mov     ds:byte ptr [0], bl     ; restore original memory content
        stc                                     ; return with error
CSC6:
        pop     ds
        pop     bx
        pop     ax

        ret
Check_SST_28SF040   endp
```

Software Drivers

28PC040 / 28LP040
4 Megabit PCMCIA Interface EEPROM

July 1996

28PC040 / 28LP040
Software Drivers

ABOUT THE SOFTWARE

This application note provides example software code for controlling sector erasing and byte programming SST's 28PC040 4 Mbit PCMCIA EEPROM. Two programming languages are provide: high-level "C" for broad platform support and an optimized 8086 assembly language. In many cases, the software driver routines can be inserted "as is " into the main body of code being developed by the system software engineers. Extensive comments are included in each routine to facilitate adapting to code to specific applications. "C" language code can be used with many microprocessors and microcontrollers, while the 8086 assembly language code provides an solution optimized for 8086 microprocessors and embedded processors.

NOTE:

The 28PC040 is for 5 volt applications, the 28LP040 is for 3.3 volts applications. Device functionality is identical for application of this software. For convenience, only the 28PC040 will be referenced in the example codes provided.

ABOUT THE 28PC040

Companion product datasheets for the 28PC040 should be reviewed in conjunction with this application note for a complete understanding of the device.

The 28PC040 features high performance program and sector (256 bytes) erase capability. A command register is incorporated on chip to facilitate interface and control of the 28PC040. Device Read, Erase, Program, and other essential operations are accomplished via the command register. Commands are written to the command register using standard microprocessor write timings. The register contents serve as input to an internal state machine, which controls the erase and program circuitry. Address and data are latched for program and erase operations. The command register does not occupy an addressable memory location. It is a latch used to store the command, along with address and data information needed to execute the command.

Provisions are made to prevent inadvertent writes through a software approach. In order to perform the functions of sector erase or program, users must issue a series of seven byte-read sequence to the 28PC040 to unprotect the chip. After the device is unprotected, users can then erase and program the device. A byte must be erased prior to programming, i.e., do not program an already programmed byte. The Sector_Erase operation is initiated by a setup command and an execute command. The setup command(022h) stages the device for electrical erasing of all bytes within a sector and the execute command(0DDh) executes the sector-erase operation. The erase operation begins with the rising edge of the -WE pulse and terminates by the Reset command. After the erase operation, programming is done on a byte-by-byte basis for a total of 256 bytes. The end of each byte program cycle can be detected by two means, namely by monitoring either DATA# Polling or Toggle Bit.

Both the C and 8086 assembly code in the document contain the following routines, in this order:

Name	Function
Write_28PC040	Alter data
Check_Toggle_Ready	End of write detection using Toggle bit
Check_Data_Polling	End of write detection using Data# polling
Disable_Chip_Data_Protection	Diables software data protection
Enable_Chip_Data_Protection	Enable software data protection
Check_SST_28PC040	Check manufacturer and device ID

"C" LANGUAGE DRIVERS

```
/*****************************************************************************************************/
/* Copyright Silicon Storage Technology, Inc. (SST), 1994, 1995                                      */
/* EXAMPLE "C" language Driver of 28PC040 4 Mbit PCMCIA EEPROM                                       */
/* Chi Chung Yin, Silicon Storage Technology                                                         */
/*                                                                                                   */
/* Revision 1.0, August 1, 1994                                                                      */
/* Revision 1.1, March  1, 1995                                                                      */
/*                                                                                                   */
/* This file requires these external "timing" routines:                                              */
/*                                                                                                   */
/*       1.) Time_Delay(MicroSeconds)                                                                */
/*       2.) Delay_1_MicroSecond                                                                     */
/*       3.) Delay_4_MicroSeconds                                                                    */
/*                                                                                                   */
/*****************************************************************************************************/

#define FALSE                   0
#define TRUE                    (~FALSE)

#define ROW_SIZE                256             /* Must be 256 bytes for 28PC040  */

#define SST_ID                  0xBF            /* SST Manufacture's ID code */
#define SST_28PC040             0x11            /* SST 28PC040 device code */

#define AUTO_PG_ERASE1          0x22
#define AUTO_PG_ERASE2          0xDD
#define AUTO_PGRM               0x11
#define RESET                   0xFF
#define READ_ID                 0x99
#define ERASE_VERIFY            0xAA

#define MAX_INCREMENT           0x7
#define ERASE_RETRY_CNT         157             /* 7 + 150 */

typedef unsigned char           BYTE;
typedef unsigned int            WORD;

/*************************************************************/
/*                  EXERNAL ROUTINES                         */
/*************************************************************/

extern void     Time_Delay(WORD MicroSeconds);
extern void     Delay_1_MicroSecond();
extern void     Delay_4_MicroSecond();

void Check_Toggle_Ready (BYTE far *);
void Check_Toggle_Ready (BYTE far *, BYTE);
```

```
/*****************************************************************************************************/
/* PROCEDURE:                    Program_28PC040                                                     */
/*                                                                                                   */
/* This procedure can be used to write a total of 256 bytes at one write cycle to the                */
/* SST's 28PC040 4 Mbit PCMCIA EEPROM.                                                               */
/*                                                                                                   */
/* Input:                                                                                            */
/*        SRC    SOURCE address containing the data which will be                                    */
/*               written into the 28PC040.                                                           */
/*        Dst    DESTINATION address which will be written with the                                  */
/*               data passed in from ds:si                                                           */
/*        Tape   Inital Tape value (used for Page_Erase command)                                     */
/*                                                                                                   */
/* Out put:                                                                                          */
/*         return - 1 : indicates an error in programming the 28PC040                                */
/*         return  0  : indicates no error in programming the 28PC040                                */
/*****************************************************************************************************/

int Program_28PC040 (BYTE far *Src,   BYTE far *Dst,        WORD Tape)
{
        BYTE far *Temp;
        BYTE far *SourceBuf;
        BYTE far *DestBuf;
        int Index;
        int Count;
        int ErrorRetry = 0;
        WORD Delay;
        BYTE SourceByte;
        BYTE ProgrammedBYTE;
        BYTE Continue

        SourceBuf = Src;
        Delay = Tape;
        /*************************************************************************************/
        /*                          ERASE OPERATION                                          */
        /*                                                                                   */
        /*************************************************************************************/
        do
        {
                /****** must disable interup here ******/
                DestBuf = Dst;
                *DestBuf = AUTO_PG_ERASE1;        /* erase the page before programming */
                *DestBuf = AUTO_PG_ERASE2;
                Time_Delay(Delay);
                *DestBuf = REST;
                Delay_4_MircoSecond();
                /****** must enable interrupt here******/
      /* verify the sector just  erased,  It must be all 0xFF */
```

```
        Count = 0;
        Continue = TRUE;
        while (( Count < ROW_SIZE_) && (Continue))
        {
                *DestBuf = ERASE_VERIFY;
                Delay_1_MicroSecond();
                SourceByte = *DestBuf:
                if (SourceByte == 0xFF)
                {
                        Count ++;
                        DestBuf++;                      /* point to next byte */
                }
                else
                {
                        if (ErrorRetry < MAX_INCREMENT)
                           Delay = Delay << 1;
                        Continue = FALSE;
                        ErrorRetry++;
                }
        }
} while (( ErrorRetry <= ERASE_RETRY_CNT) && (Count < ROW_SIZE));

if (!Continue)
   return(TRUE);          /* return with error */
```

```
/*****************************************************************************************************/
/*                          PROGRAM  OPERATION                                                       */
/*                                                                                                   */
/*****************************************************************************************************/

SourceBuf = Src;
DestBuf = Dst;

for (Index = 0; Index < ROW_SIZE; Index++){
        SourceByte = *SourceBuf++;
        if (SourceByte != 0xFF{                    /* If the data is 0xFF, don't program it */
                *DestBuf = AUATO_PGRM;             /*issue AUTO PROGRAM command */
                *DestBuf = SourceByte;             /* program the data */
                Check_Toggle_Ready(Dst);           /* wait for Toggle bit ready */
                 ProgrammedByte = *DestBuff++; /* read back the data pragrammed */
                 if (SourceByte != ProgrammedByte){
                        Continue = FALSE;
                        break;
                 }
        }
}
if (!Continue)
        return(TRUE);                              /* return with error */
else
        return(TURE);                              /* return with NO error */
}
```

```
/*****************************************************************************************************/
/*PROCEDURE:                    Check_Toggle_Ready                                                   */
/*                                                                                                   */
/*During the internal  write cycle, any consecutive read operation                                   */
/*on DQ6 will produce alternating 0's and 1's i.e. toggling between                                  */
/* 0 and 1.  When the write cycle is completed, DQ6 of the data  will                                */
/* stop toggling.  After the DQ6 data bit stops toggling, the device is ready                        */
/* for next operation.                                                                               */
/*                                                                                                   */
/* Input:                                                                                            */
/*       Dst             must  already set-up by the caller                                          */
/*                                                                                                   */
/* Output:                                                                                           */
/*       None                                                                                        */
/*****************************************************************************************************/

void Check_Toggle_Ready (BYTE far  *Dst)
{
        BYTE Loop = TRUE;
        BYTE PreData;
        BYTE CurrData;
        unsigned long TimeOut = 0;

        PreData = *Dst;
        PreData = PreData & 0x44;
        while ((Timeout< 0x07FFFFFF) && (Loop))
        {
                CurrData = *Dst;
                CurrData = CurrData & 0x44;
                if (PreData == CurrData)
                        Loop = FALSE;           /* ready to exit the while loop */
                PreData = CurrData;
                TimeOut++;
        }
}
```

```
/*****************************************************************************************************/
/* PROCEDURE:                Check_Data_Polling                                                      */
/*                                                                                                   */
/* During the internal write cycle, any attempt to read DQ7 of the byte loaded during                */
/* the byte-load cycle will receive the complement of the true data.  Once the  write                */
/* cycle is completed, DQ7 will show true data.                                                      */
/*                                                                                                   */
/* Input:                                                                                            */
/*       Dst             must already set-up by the caller                                           */
/*       TrueData        this is the original (true) data                                            */
/*                                                                                                   */
/* Output:                                                                                           */
/*       None                                                                                        */
/*****************************************************************************************************/

void Check_Data_Polling (BYTE FAR  *Dst,        BYTE TrueData)
{
        BYTE Loop = TRUE;
        BYTE PreData;
        BYTE CurrData;
        unsigned long TimeOut = 0;

        TrueData = TrueData &  0x88;
        while ((Timeout< 0x07FFFFFF) && (Loop))
        {
                CurrData = *Dst;
                CurrData = CurrData & 0x88;     /* mask out the DQ3 & DQ7 bit */
                if (TrueData == CurrData)
                        Loop = FALSE;           /* ready to exit the while loop  */
                TimeOut++;
        }
}
```

```
/*****************************************************************************************************/
/*PROCEDURE:                Disable_Chip_Data_Protection                                             */
/*                                                                                                   */
/* This procedure DISABLES the data  protection feature on the 28PC040                               */
/* 4 Mbit PCMCIA EEPROM.  After calling this routine, the chip can be written                        */
/*  without  any additional commands.                                                                */
/*                                                                                                   */
/* Input:                                                                                            */
/*        None                                                                                       */
/*                                                                                                   */
/* Output:                                                                                           */
/*        None                                                                                       */
/*****************************************************************************************************/

void Disable_Chip_Data_Protection()
{
        BYTE  far  *Temp;
        BYTE    TempByte;

        Temp  = (BYTE far *)0xE0001823;      /* set up address to be E000:1823h    */
        TempByte = *Temp;                    /* read data from the address         */
        Temp  = (BYTE far *)0xE0001820;      /* set up address to be E000:1820h    */
        TempByte = *Temp;                    /* read data from the address         */
        Temp  = (BYTE far *)0xE0001822;      /* set up address to be E000:1822h    */
        TempByte = *Temp;                    /* read data from the address         */
        Temp  = (BYTE far *)0xE0000418;      /* set up address to be E000:0418h    */
        TempByte = *Temp;                    /* read data from the address         */
        Temp  = (BYTE far *)0xE000041B;      /* set up address to be E000:041Bh    */
        TempByte = *Temp;                    /* read data from the address         */
        Temp  = (BYTE far *)0xE0000419;      /* set up address to be E000:0419h    */
        TempByte = *Temp;                    /* read data from the address         */
        Temp =  (BYTE far *)0xE000041A;      /* set up address to be E000:041Ah    */
        TempByte = *Temp;                    /* read data from the address         */

}
```

```
/*****************************************************************************************************/
/*PROCEDURE:              Enable_Chip_Data_Protection                                                */
/*                                                                                                   */
/* This procedure ENABLES the data protection feature on the 28PC040                                 */
/* 4 Mbit PCMCIA EEPROM.  After calling this routine, the chip cannot be written                     */
/* without disabling SDP first.  Disabling the SDP can be done by calling the                        */
/*  "Disable_Chip_Data_Protection" routine.                                                          */
/*                                                                                                  */
/* Input:                                                                                            */
/*        None                                                                                       */
/*                                                                                                   */
/* Output:                                                                                           */
/*        None                                                                                       */
/*****************************************************************************************************/

void Enable_Chip_Data_Protection()
{
        BYTE  far  *Temp;
        BYTE    TempByte;

        Temp  = (BYTE far *)0xE0001823;       /* set up address to be E000:1823h    */
        TempByte = *Temp;                     /* read data from the address         */
        Temp  = (BYTE far *)0xE0001820;       /* set up address to be E000:1820h    */
        TempByte = *Temp;                     /* read data from the address         */
        Temp  = (BYTE far *)0xE0001822;       /* set up address to be E000:1822h    */
        TempByte = *Temp;                     /* read data from the address         */
        Temp = (BYTE far *)0xE0000418;        /* set up address to be E000:0418h    */
        TempByte = *Temp;                     /* read data from the address         */
        Temp = (BYTE far *)0xE000041B;        /* set up address to be E000:041Bh    */
        TempByte = *Temp;                     /* read data from the address         */
        Temp = (BYTE far *)0xE0000419;        /* set up address to be E000:0419h    */
        TempByte = *Temp;                     /* read data from the address         */
        Temp = (BYTE far *)0xE000040A;        /* set up address to be E000:040h     */
        TempByte = *Temp;                     /* read data from the address         */
}
```

```
/*****************************************************************************************************/
/*PROCEDURE:                    Check_SST_28PC040                                                    */
/*                                                                                                   */
/* This procedure decides whether a  physical hardware device has a SST                              */
/* 28PC040 4 Mbit PCMCIA  EEPROM installed or not..                                                  */
/*                                                                                                   */
/* Input:                                                                                            */
/*       None                                                                                        */
/*                                                                                                   */
/* Output:                                                                                           */
/*       return -1:  indicates no SST 28PC040 installed                                              */
/*       return 0:   indicates a SST  28PC040 is installed                                           */
/*****************************************************************************************************/

int Check_SST_28PC040()
{
        BYTE far  *Temp;
        BYTE SST_id1;
        BYTE SST_id2;
        int   ReturnStatus;
        BYTE OriginalByte;

        Temp  = (BYTE far *)0xE0000000;
        OriginalByte = *Temp;                   /* save the original memory contents   */
        *Temp = RESET;                          /* reset tje 28PC040 chip first        */
        *Temp = READ_ID;                        /* issue the READ_ID command           */

        Temp  = (BYTE far *)0xE0000000;         /* set up address to be E000:0000h     */
        SST_id1 = *Temp                         /* get first ID byte                   */
        Temp  = (BYTE far *)0xE0000001;         /* set up address to be E000:0001h     */
        SST_id2 = *Temp;                        /* get second ID byte                  */

        If ((SST_id1 == SST_ID) && (SST_id2 == SST_28PC040))
                ReturnStatus = 0;
        else
                ReturnStatus = -1;
        Temp  = (BYTE far *)0xE0000000;
        *Temp = RESET;                          /* issue RESET command to 28PC040   */
        if (ReturnStatus ==-1)
                *Temp = OriginalByte;           /* if not 28PC040, restore original contents  */
        return(ReturnStatus);
}
```

8086 ASSEMBLY LANGUAGE DRIVERS

```
; ==========================================================================
; Copyright Silicon Storage Technology, Inc. (SST), 1994, 1995
; EXAMPLE 8086 assembly Drivers for 28PC040 4 Mbit EEPROM
;  Chi Chung Yin,  Silicon Storage Technology
;
; Revision 1.0, August 1, 1994
; Revision 1.1,  March 1, 1995
;
; This file requires these external "timing" routines:
;
;    1.) Time_Delay (delay "x" no. of  microseconds as supplied in DX register)
;    2.) Delay_1_MicroSecond
;    3.) Delay_4_MicroSecond
;==========================================================================

ROW_SIZE            EQU   256           ;Must be 256bytes for 28PC040

SST_ID              EQU   0BFh          ;SST Manufacture's ID code
SST_28PC040         EQU   011h          ;SST 28PC040 internal code

AUTO_PG_ERASE1      EQU   022h
AUTO_PG_ERASE2      EQU   0DDh
AUTO_PGRM           EQU   011h
ERASE_VERIFY        EQU   0AAh
RESET               EQU   0FFh
READ_ID             EQU   099h

ABS_SEGMENT         EQU   0E000h

extrn   Time_Delay:near
extrn   Delay_1_MicroSecond:near
extrn   Delay_4_MicroSecond:near
```

```
; ============================================================================
; PROCEDURE:                    Program_28PC040
;
; This procedure can be used to write a total of 256 bytes to the
;  28PC040 4 Mbit PCMCIA EEPROM.
;
; Input:
;       ds:si   SOURCE address containing the data which will be
;               written into the 28PC040.
;       es:di   DESTINATION address which will be written with the
;               data passed in for ds;si
:       dx      contains the Tape value passed in from caller
;
; Output:
;       carry bit: SET means programming error
;       carry bit: CLEAR means programmed O.K.
;       SI, DI:  Contains the original values
; ============================================================================
ERASE_RETRY_CNT   EQU   157     ; maximum no. of retry loop
MAX_INCREMENT     EQU   7

Program_28PC040           proc    near

        push    ax
        push    bx
        push    cx
        push    di
        push    si
        pushf                   ; preserve the "direction" flag in the FLAG
                                ; register

        cld                     ; clear "Direction" flag in the FLAG register

        mov     bx, di          ; save DI value in BX in order to use it later

; ============================================================================
;                       ERASE  OPERATION
;============================================================================

        mov     CX, ERASE_RETRY_CNT
WORS1:
        push    cx              ; save the current value of "Erase_Retry_Cnt"
        mov     di,bx           ; get the original address back from what was saved in BX at
                                ; the beginning of this routine
        mov     byte ptr es:[bx], AUTO_PG_ERASE1
        mov     byte ptr es:[bx], AUTO_PG_ERASE2

        call    Time_Delay      ; delay "x" no. of microseconds as supplied in DX register
        mov     byte ptr es:[bx], RESET
        call    Delay_4_MicroSecond
```

```
;
; Verify the sector just erased.  It must be all 0FFh
;

        mov     cx, ROW_SIZE
WOS1_1:
        mov     BYTE PTR ES:[DI], ERASE_VERIFY; execute ERASE_VERIFY command
        call    Delay_1_MicroSecond
        mov     al,byte ptr es:[di]             ; read the byte from destination address
        cmp     al, 0FFh                        ; is it erased?
        jnz     WOS1_2                          ; NO, then erase again with longer delay
        inc     di                              ;YES, then check the next byte
        loop    WOS1_1

;
; All the bytes in this page have been erased. (equal to 0FFh)
;

        pop     cx                              ; throw away "Erase_Retry_Cnt" from stack
        jmp     short WOS1_3

WOS1_2:
        pop     cx                              ; restore "Erase_Retry_Cnt" from stack
        cmp     cx,MAX_INCREMENT                ; do we need to double the Delay time?
        jae     WOS11_2
        shl     dx, 1                           ; put in longeer delay for the "ALGO_ERASE"
                                                ; command
WOS11_2:
        loop    WOS1

;
; Some bytes in the page just erased are NOT 0ffh.  Return the routine
; with Carry bit set to indicate error during erase operation.

        popf                                    ; restore original Flag register value
        stc                                     ; set Carry bit ot indicate error
        jmp     short WOS1_6
```

```
;-------------------------------------------------------------------------------------------------------------
;                                        PROGRAM operation
;-------------------------------------------------------------------------------------------------------------
WOS1_3:
        mov     cx, ROW_SIZE            ; program 256 bytes
        mov     di, bx                  ; restore original destination address (DI)
WOS1_4:
        lodsb                           ; get the byte to be written
        comp    al, 0FFh                ; is it 0FFh?
        jz      WOS11_5                 ; yes, no need to program it
        push    ax                      ; save the byte on the stack
        mov     byte ptr es:[di], AUTO_PGRM ;  issue the AUTO_PROGRAM command
        mov     byte ptr es:[di], al    ; program the byte
;
; Due to performance reason, we will implement "TOGGLE_BIT" test routine here.
;
        mov     al, byte ptr es:[di}    ; read back the byte just programmed
        and     al, 040h
Tx1:
        mov     ah,byte ptr es:[di]     ; read the same byte again
        and     ah, 040h
        cmp     al, ah                  ; do both reads produce the same result?
        jz      WOS1_5                  ; YES, then done because 'toggle_bit" stops
                                        ; toggling.
        xchg    ah, al                  ; NO, then keep trying until done...
        jmp     short Tx1
WOS1_5:
        pop     ax                      ; restore the byte just programmed
        cmp     al, byte ptr es:[di]    ; is it the same as original?
        je      WOS11_5
        popf                            ; the byte just programmed is NOT the same as
        stc                             ; original, return error to the caller
        jmp     short WOS1_6
WOS11_5:
        inc     di
        loop    WOSI_4                  ; program next byte

        popf
        clc                             ; clear Carry bit  to indicate NO error
WOS1_6:
        pop     si
        pop     di
        pop     cx
        pop     bx
        pop     ax

        ret
Program_28PC040     endp
```

```
;=====================================================================
; PROCEDURE:                    Check_Toggle_Ready
;
; During the internal write cycle, any consecutive read operation
; on DQ6 will produce alternating O's and 1's, i.e. toggling between
; 0 and 1.  When the write cycle is completed, the DQ6 data will
; stop toggling.  After the DQ6 data stops toggling, the device is ready
; for the next operation.
;
; Input:
;       es:di    must already set-up by the calller
;
; Output:
;       None
;=====================================================================

Check_Toggle_Ready   proc    near

        push    ax
        mov     al, es:[di]             ; read a byte form the chip
        and     al,44h                  ; mask out the TOGGLE bit (DQ2 & DQ6)
CTR_Tog2:
        mov     ah,es:[di]              ; read the same byte from the chip again
        and     ah, 44h                 ; mask out the TOGGLE BIT (DQ2 & DQ6)
        cmp     al, ah                  ; is DQ6 still toggling?
        je      CTR_Tog3                ; NO, then the programming is done
        xchg    ah, al                  ; YES, then continue checking...
        jmp     short CTR_Tog2
CTR_Tog3:
        pop     ax

        ret

Check_Toggle_Ready   endp
```

```
;=============================================================================
; PROCEDURE:                    Check_Data_Polling
;
; During the internal write cycle, any attemp to read DQ7 of the byte loaded during
; the byte-load cycle will receive the complement of the true data.  Once the
; write cycle is completed, DQ7 will show  true data.
;
; Input:
;       es:di     must already set-up by the caller
;       bl        contains the original (true) data
;
; Output:
;       None
;=============================================================================

Check_Data_Polling      proc    near

        push    ax

        an      bl, 88h                 ; mask out the  DQ3 & DQ7 bit
CDP_Tog2:
        mov     al, es:[di]             ; read a byte from the chip
        and     al,88h                  ; mask out the DQ3 & DQ7 bit
        camp    al,bl                   ; is DQ7 still complementing?
        jne     CDP_Tog2

        pop     ax

        ret

Check_Data_Polling      endp
```

```
;=============================================================================
; PROCEDURE:                    Disable_Chip_Data_Protection
;
;This procedure DISABLES the data protection feature on the 28PC040
;4 Mbit PCMCIA EEPROM.  After calling the routine, the chip can be written
; without any additional commands.
;
; Input:
:       None
;
; Output:
;       None
;=============================================================================

Disable_Chip_Data_Protection   proc    near

        push    ax
        push    ds

        cli
        mov     ax, ABS_SEGMENT
        mov     ds, ax

        mov     al, byte ptr ds:[1823h]         ; issue the 7-byte read sequences to the chip
        mov     al, byte ptr ds:[1820h]         ; to unprotect the chip
        mov     al, byte ptr ds:[1822h]
        mov     al, byte ptr ds:[0418h]
        mov     al, byte ptr ds:[041Bh]
        mov     al, byte ptr ds:[0419h]
        mov     al, byte ptr ds:[041Ah]

        pop     ds
        pop     ax

        ret

Disable_Chip_Data_Protection endp
```

```
;=============================================================================
; PROCEDURE: Enable_Chip_Data_Protection
;
;This procedure ENABLES the data protection feature on the 28PC040
;4 Mbit PCMCIA EEPROM.  After calling the routine, the chip can be written
; without disabling SDP first.  Disabling the SDP can be done by calling the
; "Dlisable_Chip_Data_Protection" routine.
;
; Input:
:       None
;
; Output:
;       None
;=============================================================================

Disable_Chip_Data_Protection   proc    near

        push    ax
        push    ds

        cli
        mov     ax, ABS_SEGMENT
        mov     ds, ax

        mov     al, byte ptr ds:[1823h]         ; issue the 7-byte read sequences to the chip
        mov     al, byte ptr ds:[1820h]         ; to protect the chip from program operation
        mov     al, byte ptr ds:[1822h]
        mov     al, byte ptr ds:[0418h]
        mov     al, byte ptr ds:[041Bh]
        mov     al, byte ptr ds:[0419h]
        mov     al, byte ptr ds:[040Ah]

        pop     ds
        pop     ax

        ret

Disable_Chip_Data_Protection endp
```

```
;=============================================================================
; PROCEDURE:                    Check_SST_28PC040
;
; This procedure decides whether a physical hardware device has a SST's
; 28PC040 4 Mbit PCMCIA EEPROM installed or not.
;
; Input:
;       None
;
; Output:
;       carry bit:  SET means no SST 28PC040 installed
;       carry bit:  CLEARED means a SST 28PC040 is installed
;=============================================================================

Check_SST_28PC040   proc    near

        push    ax
        push    bx
        push    ds

        cli
        mov     ax, ABS_SEGMENT
        mov     ds, ax
        mov     bl, ds:byte ptr [0]         ; save original memory content
        mov     ds:byte ptr [0h], RESET         ; reset the 28PC040 chip
        mov     ds:byte ptr [0h], READ_ID       ; issue READ_ID command to the chip
;
;Now, Check the SST 28PC040 Manufacture's ID and Internal Die Code
;
        mov     al, ds:byte ptr[0]
        cmp     al, SST_ID                      ; is this a SST part?
        jne     CSC5                            ; NO, then return Carry set
        mov     al,ds:byte ptr[1]
        cmp     al, SST_28PC040                 ; Is it 28PC040?
        jne     CSC5                            ; NO, then Non-SST part
CSC4:
        mov     ds:byte ptr [0], RESET          ; issure RESET command to the chip
        clc                                     ; return with NO error
        jmp     short CSC6
CSC5:
        mov     ds:byte ptr [0], RESET          ; issue RESET command to the chip
        mov     ds:byte ptr [0], bl         ; restore original memory content
        stc                                     ; return with error
CSC6:
        pop     ds
        pop     bx
        pop     ax

        ret
Check_SST_28PC040   endp
```

Technical Paper

SuperFlash EEPROM Technology

July 1996

1.0 Introduction

The following paper describes the patented and proprietary Silicon Storage Technology, Inc. (SST) CMOS SuperFlash EEPROM technology and the SST field enhancing tunneling injector split-gate memory cell. The SuperFlash technology and memory cell have a number of important advantages for designing and manufacturing flash EEPROMs, when compared with the thin oxide stacked gate or two transistor approaches. These advantages translate into significant cost and reliability benefits for the user.

The SST SuperFlash technology typically uses a simpler process of 13 masking layers, compared to 19 or more layers for other flash EPROM or EEPROM approaches. The fewer masking steps significantly reduces the cost of manufacturing a wafer. Reliability is improved by reducing the latent defect density, i.e., fewer layers are exposed to possible defect causing mechanisms.

The SST split gate memory cell is comparable in size to the single transistor stacked gate cell (for a given level of technology), yet provides the performance and reliability benefits of the traditional two transistor byte alterable EEPROM cell. By design, the SST split gate memory cell eliminates the stacked gate issue of "overerase", by isolating each memory cell from the bit line. "Erase disturb" cannot occur because all bytes are simultaneously erased in the same page and each page is completely isolated from every other page during any high voltage operation.

2.0 Field Enhancing Tunneling Injector EEPROM Cell

The field enhancing tunneling injector EEPROM cell is a single transistor split gate memory cell using poly-to-poly Fowler-Nordheim tunneling for erasing and source side channel hot electron injection for programming. Poly-to-poly tunneling is from a field enhancing tunneling injector formed on the floating gate using industry standard oxidation and dry etching techniques. Source side channel hot electron injection is very efficient, thus allowing the use of a small on-chip charge pump from a single low voltage power supply, e.g., 5 or 3 volts. Cells are normally erased prior to programming.

The split gate memory cell size is comparable to traditional stacked gate memory cells using the same process technology. This is possible because:

a) the tunneling injector cell does not need the extra spacing to isolate the higher voltages and currents required for programming the stacked gate array, and

b) floating gate extensions are not needed to achieve the required stacked gate coupling ratios.

Additionally, the simplicity of the structure eliminates many of the peripheral logic functions needed to control erasing of the stacked gate device. The tunneling injector cell can be part of a standard CMOS process of 13 masks, instead of the 19 or more masking layers required for stacked gate structures.

Memory arrays may use either random access or sequential access peripheral architectures.

3.0 Cell Structure

3.1 Cell Cross Sections and Layout

A top view and a cross-sectional view along the word line are presented in Figures 1a and 1b (note drawings are not to scale).

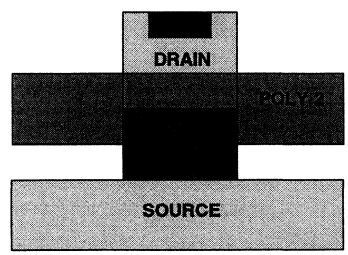

Figure 1a: Top View of the Cell

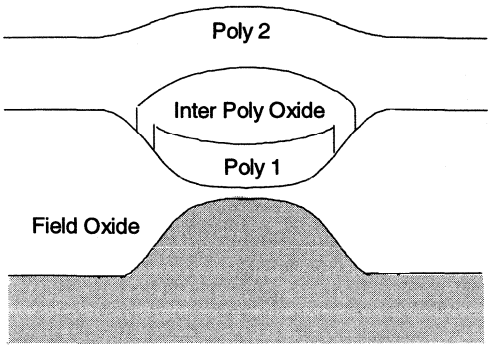

Figure 1b: Cross-section along the Word Line

A cross-sectional view along the bit line and a SEM cross-section are presented in Figures 2a and 2b. Polysilicon or polysilicon with silicide is used to connect control gates along the word line (row). Metal is used to connect the drain of each memory cell along the bit line (column). A common source is used for each page, i.e., each pair of bits sharing a common source along a row pair (even plus odd row). A single word line is referred to as a row; the combination of the even and odd rows form a page, which is erased as an entity. Programming may be either byte by byte individually or for all bytes within the same page simultaneously.

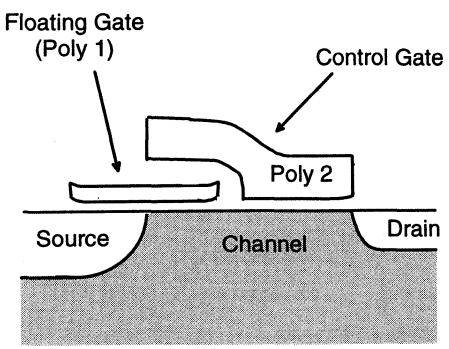

Figure 2a: Cross-section along the Bit Line

The drain region consists of an n+ S/D diffusion, which is aligned with the edge of the Poly 2 control gate. The source region consists of an n+ S/D diffusion, which overlaps the floating poly. A cell implant beneath the floating gate is used to control the intrinsic cell threshold (V_T) and the punch through voltage.

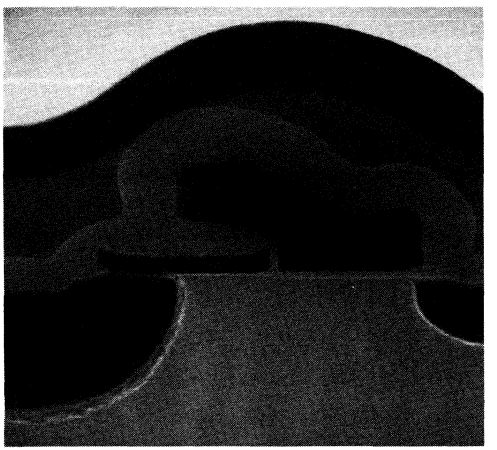

Figure 2b: Cross-section SEM Picture

The select gate is separated from the channel by a 40 nm oxide (note all the values are for a generic 1 µ technology). The floating gate is separated from the channel and source diffusion by a thermally grown 15 nm gate oxide. The floating gate is separated from the control gate by a 40 nm oxide on the sidewall and a 200 nm oxide vertically between the gates . The tunneling injector on the floating gate is formed by oxidation of the polysilicon, similar to the formation of the field oxide "bird's beak" on single crystal silicon, followed by a reactive ion etching of polysilicon. A silicide or policide can be formed on the control gate to reduce the poly word line resistance.

3.2 Cell Array Schematic

The cell schematic is presented in Figure 3a, showing the logical organization of the memory array. An equivalent circuit representation used to illustrate capacitive coupling is presented in Figure 4.

For the split gate memory cell, the channel between the source and drain is split and controlled by the series combination of the select gate transistor and the memory gate transistor. The memory transistor is either in high or low/negative threshold state depending on the amount of stored electric charge on the floating gate. See Figure 3b.

During the read operation, this reference voltage is applied to the control gate and the select gate, via the word line. The reference voltage will "turn on" the select gate portion of the channel. If the floating gate is programmed (high threshold state), the memory transistor portion of the channel will not conduct. If the floating gate is erased (low or negative threshold state), this memory cell will conduct.

Figure 3a represents a section of a typical cross-point memory array, arranged as 8 memory cells in 2 columns (bit lines), 2 source lines, and 4 word lines. Note, the word line is split into an even and odd row, which isolates the source line from all other source lines. Figure 3b is an equivalent memory cell, showing how the split gate cell provides the logical equivalent of a select transistor and a memory transistor. The voltage applied to each terminal during normal operations is listed in Table 1.

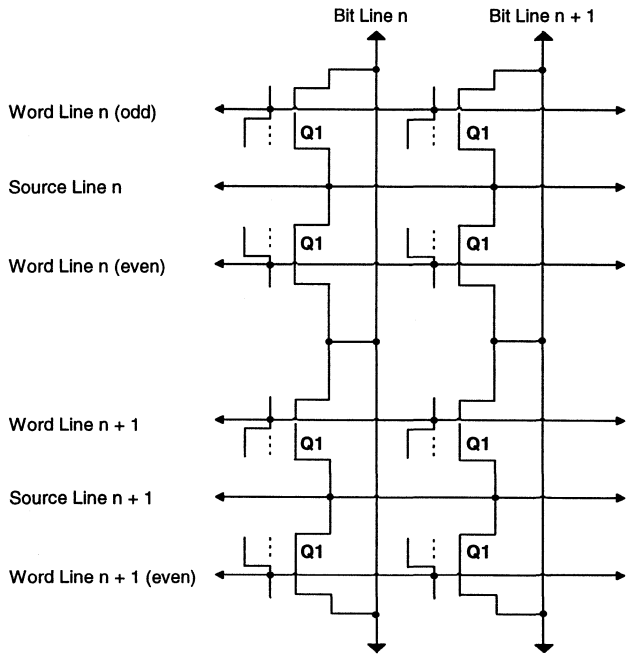

Figure 3a: Cell Array Schematic

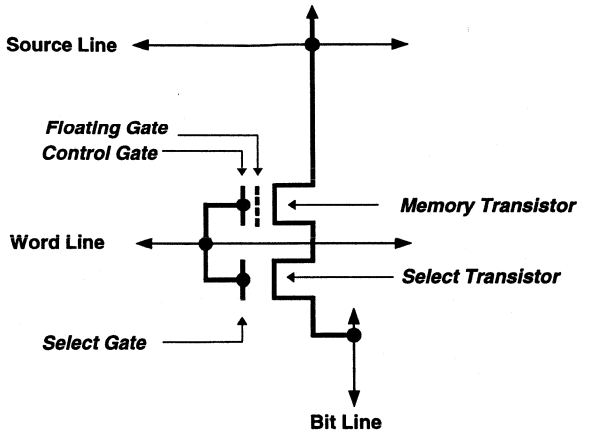

Figure 3b: Equivalent Memory Cell Structure for Q1

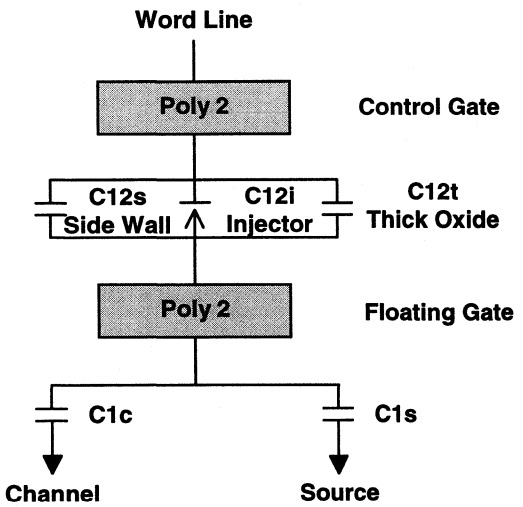

Figure 4: Equivalent Capacitive Coupling Circuit

C10 = C1c + C1s; C12 = C12s + C12i + C12t

Coupling Ratios (CR) are defined as:

1. CR10 = CR (poly 1 to substrate)
   = C10/ (C10 + C12)
2. CR12 = CR (poly 1 to poly 2)
   = C12/(C10 + C12)
3. CR10 + CR12 = 1.

During erasing, the channel is in inversion due to the word line voltage. This increases the value of C1c. During Programming the channel is in depletion; thus, C1c is negligible. Therefore, the coupling ratios are different during erasing and programming.

During programming, the coupling capacitance ratio between the source and the floating gate is ≈ 80%. This means ≈ 80% of the voltage at the source will be coupled to the floating gate, e.g., if the source is at 12 volts, the floating gate will be at 9.6 volts, given no charge on the floating gate.

The following Table 1 gives the conditions for the memory cell terminals during the erase, program, and read operations. These are nominal conditions for a generic 1 u process. V_{CC} is the power supply, nominal 3.0, 3.3, or 5 volts, V_{SS} is ground. V_T is the cell threshold. V_{REF} is the reference voltage used to access the memory cell during the read cycle The high voltages on the word line during erase and the source line during programming are generated by an on-chip charge pump.

Table 1 Operating Conditions

	ERASE	PROGRAM	READ
WORD LINE	≈15 volts	V_T	V_{REF}
BIT LINE	V_{SS}	≈ V_{CC} →"1" ≈ V_{SS} →"0"	≈ 2 volts
SOURCE LINE	V_{SS}	≈ 12 volts	V_{SS}

4.0 Charge Transfer Mechanisms

4.1 Erasing

The cell erases using floating gate to control gate Fowler-Nordheim tunneling. The floating gate poly oxidation process provides a uniform field enhanced tunneling injector along the edges of the floating gate. This repeatable manufacturing process provides consistent oxide integrity that minimizes endurance induced degradation, i.e., charge trapping or oxide rupture.

During erasing, the source and drain are grounded and the word line is raised to ≈ 15 volts. The conditions for erasing are in Table 1, reference Figure 2 for identification of terminals. The low coupling ratio between the control gate and the floating gate provides a significant Δ V across the interpoly oxide, which is the same everywhere between Poly 1 and Poly 2. A high field is generated primarily along the edge of the tunneling injector. Charge transfer is very rapid and is eventually limited by the accumulation of positive charge on the floating gate. This positive charge raises the floating gate voltage until there is insufficient Δ V to sustain Fowler-Nordheim tunneling.

The removal of negative charge leaves a net positive charge on the floating gate. The positive charge on the floating gate decreases the memory cell's threshold voltage, such that the memory cell will conduct ≈ 100 μA when the reference voltage is applied to the memory cell during a read cycle. The reference voltage is sufficient to turn on both the select transistor and the memory transistor in the addressed memory cell.

Erasing can either be by fixed erase pulses generated by an internal timer or algorithmically generated by an external controller in order to optimize erase performance. Internal verify circuits will assure adequate erase margin.

4.2 Erase Disturb

The enhanced field tunneling injector devices are internally organized by pairs (pages) of even and odd rows. Each row pair (page) shares a common source line and each row pair has the word line at the same voltage potential during erasing. Thus, all bytes are simultaneously erased along the common word lines. All other word lines (pages) do not receive the erasing high voltage. Therefore, erase disturb is not possible. The column leakage phenomena caused by "overerase" in stacked gate cells is not possible, because the split gate provides a integral select gate to isolate each memory cell from the bit line.

4.3 Programming

The cell programs using high efficiency source-side channel hot electron injection. The conditions for programming are in Table 1, reference Figure 2 for identification of terminals. The intrinsic (i.e., UV erased) floating gate threshold is positive; thus, the memory cell is essentially non-conducting, with the word line at the reference voltage during a read cycle.

During programming, a voltage, approximately equaling the threshold V_T of the select transistor, is placed on the control gate, via the word line. This is sufficient to turn on the channel under the select portion of the control gate. The drain is at ≈ V_{SS}, if the cell is to be programmed. If the drain is at V_{CC}, programming is inhibited. The drain voltage is transferred across the select channel because of the voltage on the control gate. The source is at ≈ 12 volts. The source to drain voltage

differential (i.e., 12 volts - ≈ V_{SS}) generates channel hot electrons. The source voltage is capacitively coupled to the floating gate. The field between the floating gate and the channel very efficiently (≈ 100%) sweeps to the floating gate those channel hot electrons that cross the Si-SiO_2 barrier height of ≈ 3.2 ev.

The programming effect is eventually self limiting as negative charge accumulates on the floating gate. The programming source-drain current is very low; thus, the source voltage can be generated by a charge pump internal to the die. The program time is fast because of the high efficiency of source side injection. The addition of negative charge to the floating gate neutralizes the positive charge generated during erasing; thus, the cell is nonconducting when the reference voltage is applied during a read cycle.

Programming can either be by fixed program pulses generated by an internal timer or generated by an external controller to optimize program conditions. Internal verify circuits will assure adequate program margin.

4.4 Program Disturb

The memory cells are arranged in a true cross point array, using a word line and bit line for address location selection; thus, unselected cells within a page will see the programming voltages. There are two types of possible program disturbs with the field enhanced tunneling injection cell, which are described in the following paragraphs. Both mechanisms are preventable by proper design and processing. Defects are screenable with testing. Devices with this memory architecture do not have program disturb caused by accumulated erase/programming cycles because each page is individually isolated. Each cell is only exposed to high voltage within the selected page along the row or source line, there is no high voltage on the bit line.

4.4.1 Reverse Tunnel Disturb

Reverse tunnel disturb can occur for unselected erased cells sharing a common source line, but on the other row of the selected page to be programmed; thus, the word line is grounded. The source voltage is capacitively coupled to the floating gate of the unselected erased cell. If there is a defect in the oxide between the control gate and the floating gate, Fowler-Nordheim tunneling may occur. This could program the unselected erased cell. Proper design and processing assures the reverse tunnel voltage is significantly higher than any applied voltage. Defects are eliminated by including a reverse tunnel voltage screen in the 100% testing operations. Forward tunneling is defined as occurring when electrons are transferred from poly 1 (the floating gate) to poly 2 (the control gate), thereby erasing the cell. Reverse tunneling is defined as occurring when electrons are transferred from poly 2 to poly 1, thereby programming the cell.

4.4.2 Punch through Disturb

Punch through disturb can occur for selected erased cells, i.e., those sharing a common source line and bit line, in an adjacent inhibited word line. An inhibited word line is grounded to prevent normal channel hot electron injection. If there is a defect that reduces channel length and creates punch through along the select gate channel, there could be hot electrons available to program the inhibited erased cell. Proper design and processing assures the punch through voltage is significantly higher than any applied voltage. Defects are eliminated by including a punch through voltage screen in the 100% testing operation.

5.0 Other Reliability Considerations

5.1 Oxide Integrity

All oxides are subject to time dependent breakdown (TDDB), i.e., for a given oxide and electric field, eventually the oxide will breakdown. The lower the electric field and the less time the field is applied, the longer the time to breakdown. For oxides used in normal TTL voltage circuits, this time is essentially infinite; however, in flash memories that use high voltages, the time of oxide exposure to high electric fields can contribute to the intrinsic device reliability.

SST memory cell uses an ≈ 4 MV/cm electric field during erasing and programming. This value is significantly lower than the 8-10 MV/cm used by stacked gate flash approaches or the ≥ 10 MV/cm used by the thin oxide EEPROM and NAND flash approaches. Since the oxide time dependent

approaches. Since the oxide time dependent breakdown rate is an exponential function of the field strength, the SST memory cell intrinsically has a much lower failure rate than stacked gate cell for oxide breakdown. Note, the SST cell is exposed to the lower electric field for the same length of time during programming and for significantly less time for erase, compared with stacked gate approaches.

5.2 Contact Integrity

All memory arrays contain metal to silicon contacts, typically from the metal bit line to the diffused drain of the memory cell. Stacked gate and the SST memory cells use a standard cross-point array, whereby a contact is shared by every two memory cells; thus, there are many contacts in a large memory array, e.g., a 4 Megabit chip contains over 2,000,000 contacts. Contacts must have a very low failure rate because there are so many of them. Contacts and associated metal lines are subject to failure based on the current density passing through the contact and metal line. The lower the current density, the lower the potential failure rate due to contact damage or electromigration mechanisms.

The source-side channel hot electron injection current used in programming SST cells is significantly lower than the drain-side channel hot electron injection current used in programming stacked gate cells. During programming, SST cells use less than 1 μA of source-drain current; this is much less than the read cell current. In contrast, a stacked gate cell requires 500 to 1,000 μA of source-drain current during programming; which is much higher than the read cell current. The high programming current density in stacked gate cells results in a higher probability of failure due to contact damage or electromigration. Since the programming current for the SST cell is much lower than the read current, there is no increase in the reliability failure rate due to programming induced current density failure mechanisms.

Fowler-Nordheim tunneling used for erase is intrinsically a low current operation. Therefore, both the SST and stacked gate cells are not measurably affected by current density during the erase operation.

5.3 Data Retention

The field enhancing tunneling injector cell uses relatively thick oxides, compared with other EEPROM or flash cells; therefore, intrinsic data retention is robust. The thicker oxides minimize initial and latent oxide defects; thus, improving yield and oxide integrity. The lower voltages used for erase and programming combined with the relatively thicker oxides reduce the endurance related extrinsic data retention failure rate.

5.4 Endurance

Since the field enhancing tunneling injector cell uses a relatively thick oxide for the Fowler-Nordheim tunneling transfer oxide, the primary endurance limitation is due to charge trapping in the interpoly oxide. Since both erasing by tunneling and the source-side channel hot electron programming utilize relatively weaker electric fields across the poly 1 insulating oxides, the oxide rupture failure rate is low.

Trapping occurs in an ≈ 20 angstroms shallow region adjacent to the tunneling injector. Within this distance, direct tunneling de-trapping occurs in the quiescent times between erase/program cycles. In practice, this means the endurance of the device in real world applications will be greater than the endurance demonstrated in a test environment, where the device is being erase/program cycled at the maximum possible frequency.

A major concern of reprogrammable nonvolatile memories is that of "disturb" phenomena, i.e., where a different location than the one being erased or programmed is altered. "Disturbs" can occur whenever a high voltage is applied to the gate, source, or drain of a memory cell that is not being intentionally erased or programmed. The SST cell has several design advantages to reduce the possibilities for a disturb:

a) There is no high voltage placed on the bit line, as is common for stacked gate approaches. In addition, the split gate cell isolates each memory storage node from all other nodes along the bit line. Thus, a disturb via the bit line (connected to the drain) is not possible.

b) The device uses a page erase, whereby, all bytes in the page are erased simultaneously, i.e., see the same high voltage at the same

time. Since each page is isolated from every other page by the word line selection circuitry, disturbs along the word line (connected to the gate) during erasing are not possible.

c) The device uses a unique source line for each page, unlike most stacked gate devices that have the source line common to large sectors or the entire array. This limits exposure to disturb conditions to only the cells within a page during the time that page is being programmed. This greatly reduces the probability of a disturb and eases the detection, i.e., only the page being programmed need be verified after any programming operation.

5.5 Life Test (Dynamic Burn-in)

The field enhancing tunneling injector cell uses standard CMOS technology in both the periphery and memory array; therefore, the life test results will be comparable to other devices built with the same process technology. As with all floating gate reprogrammable nonvolatile memories, life test results for a given technology will generally be better than other memories, e.g., SRAM's, built with the same technology because of the standard endurance and data retention infant mortality screening.

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Technical
Paper

Technical Comparison of Floating Gate Reprogrammable Nonvolatile Memories

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Technical Comparison of Floating Gate Reprogrammable Nonvolatile Memories

1.0 Introduction

Floating gate reprogrammable EEPROMs, whether called flash memories, PEROMs, or byte alterable EEPROMs, can be compared on performance, cost, reliability, and technology. Performance, cost, and reliability are directly related to the design and wafer process technology. This paper will compare the three major approaches to producing these various EEPROMs: the thin oxide stacked gate approach; the thin oxide two transistor cell; and the thick oxide split gate cell patented by SST. These are all random access approaches, e.g., NOR. A variation of the two transistor cell is used by some manufacturers for sequential access approaches, e.g., NAND. The SST cell may also be used for sequential access architectures. This paper will review the basic technology for each approach and show the impact on performance, cost, and reliability.

2.0 Background

Nonvolatile storage is required to operate microprocessors and controllers. Historically, the program code was stored in ROM. UV-EPROM became a practical solution, as the need to update code just prior to system manufacturing became more important. Byte alterable EEPROMs were developed to provide in-situ reprogrammability, i.e., 5 volt only with standard interfaces to controllers. This solution reduced the time to market for new products and to upgrade existing designs, but cost too much for many commercial program storage applications. Low density byte alterable EEPROMs became widely used for parameter or configuration storage, where the user must frequently update customizing information. With the advent of "user friendly plug-and-play" high performance systems and the increasing need for frequent changes, a more cost effective alterable program storage solution was needed. This solution is the single transistor cell, page or sector alterable EEPROM, that combines the cost advantages of the UV-EPROM, with the performance advantages of the byte alterable EEPROM.

The purpose of EEPROMs is to provide reprogrammable nonvolatile storage of information. Reprogrammability requires the device be able to be altered in system, with minimal hardware or software difficulty. The number of times the device must be altered determines the endurance requirement of the device. Nonvolatility requires the device to retain data without power applied for the lifetime of the application. The lifetime of the application determines the data retention requirement of the device. Both of the reliability requirements of endurance and data retention have associated failure rates, which must be minimized. By definition, the endurance and data retention failure rates are nonzero and critical; therefore, their characteristics must be quantified.

3.0 Memory Cell Operation

All floating gate structures use the same basic concept to function, charge stored on the floating gate sets the memory transistor to a logical "1" or "0". Depending on the whether the memory structure is an enhancement or depletion transistor, when the floating gate is neutral or contains electrons (negative charge), the memory cell will not conduct during read. When the floating gate is neutral or has an absence of negative charge, the memory cell will conduct during read. The conducting or nonconducting state is output as the appropriate logical level. Erasing is transferring electrons off the floating gate; programming is transferring electrons on to the floating gate. Each of the 3 major memory cells erases and programs somewhat differently as summarized in Table 1. See also Figures 1-6. The oxides insulating the floating gate are eventually damaged by the transfer of electrons on and off the floating gate through these oxides. The nature and extent of the damage is assessed by the failure rates associated with endurance and data retention. The properties of erasing and programming may change as a function of how long or how many times each cell is altered.

3.1 The Stacked Gate Cell

To erase, the stacked gate cell transfers charge off the floating gate through the thin oxide underneath the floating gate, the oxide is about 10 nm thick. An electric field of approximately 10 MV/cm is placed across this oxide by either a high voltage placed on the source or a combination of a positive high voltage on the source and negative high voltage on the control gate, initiating the Fowler-Nordheim tunneling charge transfer mechanism.

Table 1: Erase/Program Comparisons

	Stacked Gate	Two Transistor	SST
Erase Method	Fowler-Nordheim Tunneling Through Thin Oxide	Fowler-Nordheim Tunneling Through Thin Oxide	Fowler-Nordheim Tunneling Through Thick Oxide
Program Method	Drain-Side CHE Injection Through Thin Oxide	Fowler-Nordheim Tunneling Through Thin Oxide	Source-Side CHE Injection Through Thick Oxide
Program Efficiency	Low	Very High	High
Program Current	≈1 mA	≈10 pA	≈1 uA

To program, the stacked gate cell transfers electrons to the floating gate through the 10 nm oxide under the floating gate using drain-side channel hot electrons (CHE). The high voltage on the drain and control gate creates channel hot electrons. A fraction of the channel hot electrons with the correct orientation and sufficient energy to cross over the silicon and gate oxide interface are injected into the gate oxide. Although many channel hot electrons enter the insulating oxide, relatively few are transferred to the floating gate, causing a low programming efficiency. The majority are pushed back to the silicon substrate and are collected at the drain. With this low efficiency, a source-drain current of approximately 1 mA is required to generate sufficient channel hot electrons to charge the floating gate to the programmed state.

3.2 The Two Transistor Thin Oxide Cell

To erase and program, the thin tunneling oxide cell transfers electrons off and on the floating gate through a small area of very thin oxide, about 8.5 nm thick. To erase, the drain is connected to high voltage, creating an electric field of about 11 MV/cm, Fowler-Nordheim tunneling transfers the electrons off the floating gate. To program, the control gate is connected to high voltage, the Fowler-Nordheim tunneling mechanism transfers electrons to the floating gate. The tunneling current is in the picoamp per cell range.

3.3 The SST Cell

To erase, the thick oxide split gate cell transfers electrons off the floating gate through an approximate 40 nm interpoly oxide. The high voltage on the control gate establishes a localized strong electric field that initiates the Fowler-Nordheim tunneling mechanism. Electrons transfer off the floating gate from the field enhancing injection edges on the floating gate. The local field near the injector is strong enough to initiate Fowler-Nordheim tunneling; however, the average field across the interpoly oxide is only ≈ 4 MV/cm. This average field is much lower than is required by the stacked gate and two transistor thin oxide cells that require the entire thin oxide volume to be subjected to a uniform high electric field.

To program, the thick oxide split gate cell transfers electrons to the floating gate through an approximate 40 nm oxide by source-side channel hot electron injection. The hot electrons are generated in the high electric field region of the split gate channel underneath the gap between the floating gate and the control gate. A fraction of the channel hot electrons with the correct orientation and sufficient energy to cross over the silicon and gate oxide interface are injected into the gate oxide. All electrons that cross the interface are swept to the floating gate by the attractive electric field. With this high efficiency of 100%, a source-drain current of only approximately 1 μA is required to generate sufficient channel hot electrons to charge the floating gate to the programmed state.

4.0 Failure Mechanisms

The critical failure mechanisms to consider for reprogrammable nonvolatile floating gate memories are data retention and endurance.

There is lot-to-lot and within-lot variability for these failure mechanisms. The relative frequency of the failure mechanisms is technology dependent;

thus, each manufacturer must address through design, process targeting, process control, and testing those mechanisms that affect the applicable technology. The basic technology will drive the success and cost of eliminating failures due to data retention and endurance. A comparison of the failure mechanisms for the stacked gate, two transistor, and SST's split gate cell is given in Table 2.

4.1 The Stacked Gate Cell

Trapped charge can create dispersion in the erase threshold, leading to the overerase condition. Erratic erase can occur due to uncontrollable quantum-mechanical effects in the injection oxide, again causing overerase. Overerase causes single columns of memory cells to be stuck "1" during read and these columns cannot be programmed. Overerase cannot be recovered by using data sheet conditions. The high source-drain current during programming can cause electromigration, interface trapping, and contact spiking problems at the source and drain of the memory transistor, resulting in single bit, row, or column failures.

4.2 The Two Transistor Thin Oxide Cell

The passage of electrons, in the presence of a high electric field, through the thin oxide causes damage to the oxide lattice structure such that charge can be trapped at these sites. The trap sites are distributed throughout the entire volume of the thin oxide. Electrons can hop from site to site from the floating gate to the substrate, which causes leakage of the charge off the floating gate. These "leaky bits" cause data retention failures after some amount of erase/program cycling. Eventually, sufficient stress is accumulated in the oxide to cause an oxide rupture and an immediate discharge of the floating gate.

4.3 The SST Cell

The strong localized field in the immediate neighborhood of the edge injector will create electron trap sites. Eventually enough electrons are trapped in this localized region, preventing single bits from erasing. The amount of charge trapped is dependent on the total charge transferred and the amount of de-trapping occurring. De-trapping of electrons back to the floating gate occurs during the intervals between erases. SST device failures can be recovered by additional erase cycles or waiting the natural interval between erase/program cycles before reusing the affected cell.

The SST cell has a very high programming efficiency; therefore, there are few interface trap sites generated and few charges trapped in the oxide. Since SST has a low source-drain current during programming, the concerns with high current flows are minimized. Devices that have a high source-drain current, e.g., stacked gate cells, must include additional area in the layout and extra processing steps to attempt to alleviate concerns with electromigration, contact spiking, and junction ruptures.

Table 2: Failure Mechanisms Comparisons

Failure Mechanisms	Stacked Gate	Two Transistor	SST
Leaky Bit	Medium	High	Low
Oxide Rupture	Low	High	Low
Overerase	High	N/A	N/A
Electromigration	High	Low	Low
Contact Spiking	High	Low	Low
Interface Trapping	High	Low	Low

5.0 Manufacturing Technologies

The manufacturing technology drives the cost and reliability of the device. The fewer the operational steps in the process, the lower the variable cost of manufacturing and the higher the resulting product reliability (lower total defect density). See Table 3.

5.1 The Stacked Gate Cell

The stacked gate cell requires extremely tight process control and oxide integrity of the thin oxide below the floating gate. Circuit functionality requires the use of a variety of transistor types; thus, the number of masking layers is at least 19 (or 21 layers if two level metal is used).

5.2 The Two Transistor Thin Oxide Cell

The two transistor thin oxide cell requires the formation of a very thin oxide, i.e., about 8.5 nm. The oxide must be of very high integrity and low defect density; thus, is difficult to manufacture. Circuit functionality requires the use of a variety of transistor types; thus, the number of masking layers is at least 19 (or 21 layers if two level metal is used).

5.3 The SST Cell

SST uses a 13 mask CMOS process, very similar to a single metal, single poly CMOS logic process, to manufacture the EEPROM memory cell. The only alteration from standard CMOS processing is the formation of the field enhancing tunneling injector, which uses standard CMOS oxidation techniques and the thick interpoly oxidation between the floating gate and the control gate. Only the standard high and low voltage P- and N-channel transistors are required for circuit functions.

6.0 Memory Array Architecture

All device types use a standard cross-point array for random access, whereby, the memory location is accessed during reading by a combination of voltages on the selected word line and bit line. The source line provides a ground reference to the voltages on the word line and bit line during reading. During erasing and programming, depending on cell architecture, some combination of high voltages and a ground reference are applied for charge transfer. See Table 4.

6.1 The Stacked Gate Cell

The stacked gate devices are organized by mutually connected rows and columns. For sectored devices there may be isolation of some combination of word lines, bits lines, or source lines. High voltage is present on all three lines; therefore, memory cell size must include the appropriate high voltage design rules at each memory transistor terminal. In addition, the high current used for drain channel hot electron injection requires additional spacing to reduce potential reliability concerns.

6.2 The Two Transistor Thin Oxide Cell

The two transistor thin oxide devices are generally organized by pages, using a common word line. There is a separate select transistor, which isolates floating gate transistor from the bit line. High voltages are present on the bit line and the word line. The select transistor is constrained by photolithography limits; however, the memory transistor must be large enough with the appropriate capacitive coupling to generate the sufficient electric field strength that is required for Fowler-Nordheim tunneling mechanism for both erasing and programming.

Table 3: Manufacturing Process Comparisons

	Stacked Gate	Two Transistor	SST
# Masking Layers	19-21	19-21	13
CMOS Logic Compatible	Difficult	Difficult	Easy
Standard Oxide Process	No	No	Yes
Fab Transferable	Very Difficult	Difficult	Moderate

6.3 The SST Cell

SST EEPROM devices are organized by pages or sectors, using common source and word lines. Thus, every page is isolated from every other page, which eliminates the possibility of disturbs between pages. The split gate isolates each floating gate from the bit line; thus, overerase is architecturally eliminated. No high voltage is ever present on the bit line, thus reducing field isolation requirements. With low current source-side channel hot electron injection for programming and no high voltage on the bit line, the memory cell size is only constrained by photolithography limits and high voltage design rules for the word line and source line.

7.0 Performance Comparisons

Read speed: All three memory transistor types have the same inherent read speed capability. Differences arise because of various peripheral architecture's and the use of two level metal by some manufacturers. (See Table 5)Currently SST devices are not designed for maximum possible speed (although the memory cell is intrinsically capable of high speed), because that requirement directly competes with the need for low cost and low power for many applications. Future SST devices will have faster read speeds, as appropriate for the new application requirements.

Power supply current: Read current is a function of the architecture and the read speed. SST devices are designed to minimize read current commensurate with reasonable read speeds. Write current is a function of the number of power supplies and the output of the charge pumps. Since SST devices use both an erasing and a programming mechanisms that are inherently low current and SST uses no external high voltage, SST write currents are the same or lower than the alternate approaches, especially when considering the page write capability.

Write functionality: The minimum erase element size is a function of device architecture. SST devices are organized to optimize the effective page size for user flexibility and speed of writing.

8.0 Summary

The SST cell architecture and process offers the optimal solution for reliability, cost, and performance. The split gate design eliminates the possibility of overerase. The field enhancing tunneling injector minimizes the average electric field across the interpoly oxide; thus, improves endurance and data retention. The 13 masking layers comprise a CMOS logic compatible process, which assures low cost and high reliability. The small page architecture provides optimum flexibility and performance at the system level for data alteration.

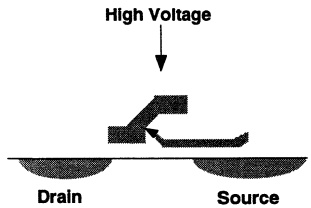
Table 4: Architecture Comparisons

	Stacked Gate	Two Transistor	SST
# Transistors per Cell	1	2	1
Cell Area/ Technology	X	3X	X
Cell Type	Stacked Poly	Stacked Poly	Split Gate Poly
# Terminals per Cell	3	4	3
# High Voltage Connections per cell	3	3	2
Addressing	NOR	NOR	NOR
Page/Sector Size	Very Large	Small	Small
Page Write Capability	No	Yes	Yes
Very Low Voltage Operation	No	Yes	Yes
Low Current Operation	No	Yes	Yes
High Speed Operation	Yes	Yes	Yes

Table 5: Performance Comparisons

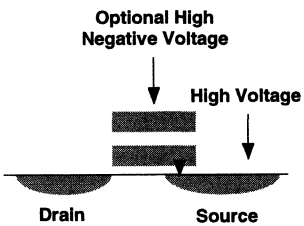
Function	Stacked Gate	Two Transistor	SST
Cell Read Speed	Same	Same	Same
I_{CC}/Isb	High (12/5 volt)	Average	Low
Page/Sector Size	Very Large	Small	Small
Write Speed	Poor	Good	Good
Data Retention	Very dependent upon supplier	Poor	Excellent
Cost	Low	High	Low
Manufacturability	Low	Low	High
Overerase	Possible	Not Possible	Not Possible

Erasing Floating Gate Memories



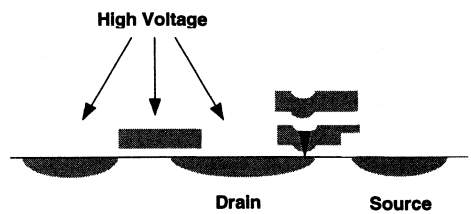
Electric Field ≈ 4 MV/cm
Tunnel Oxide ≈ 400Å
Method: Interpoly FN Tunneling

Figure 1: SST Split Gate Cell



Electric Field ≈ 10 MV/cm
Tunnel Oxide ≈ 100Å
Method: Source-Poly FN Tunneling

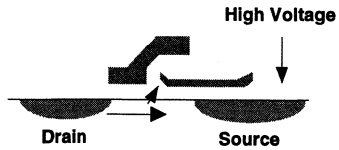
Figure 2: Stacked Gate Cell



Electric Field ≈ 11 MV/cm
Tunnel Oxide ≈ 85Å
Method: Drain-Poly FN Tunneling

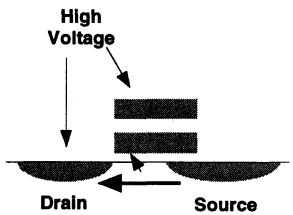
Figure 3: 2 Transistor Thin Oxide Cell

Programming Floating Gate Memories



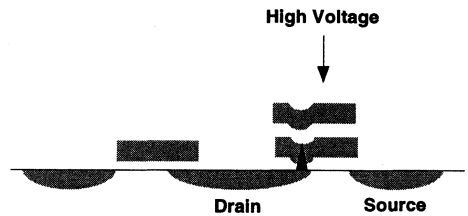
Drain - Source Electron Current ≈ 1 μA
Injection Oxide ≈ 400Å
Method: Source-Side CHE Injection

Figure 4: SST Split Gate Cell



Source - Drain Electron Current ≈ 1 mA
Injection Oxide ≈ 100Å
Method: Drain-Side CHE Injection

Figure 5: Stacked Gate Cell



Electric Field ≈ 11 MV/cm
Tunnel Oxide ≈ 85Å
Method: Drain FN Tunneling

Figure 6: 2 Transistor Thin Oxide Cell

CHE = Channel Hot Electron
FN = Fowler-Nordheim

Technical
Paper

Reliability Considerations for Reprogrammable Nonvolatile Memories

July 1996

Reliablility Considerations for Reprogrammable Nonvolatile Memories

1.0 Introduction

When acquiring a microcircuit, many considerations above and beyond the purchase price are important. Among these are quality, reliability, delivery, service, and product assurance. The lowest cost of ownership for the user is a result of the proper balance and specification of the above considerations. Reprogrammable nonvolatile memories, i.e., EEPROMs, contain the reliability considerations of endurance and data retention that can significantly affect the cost of ownership if the EEPROM is incorrectly used in the application.

2.0 Reliability

For EEPROMs, reliability is the summation of the factors of operating life (read), data retention, and endurance.

$$F.R._{Total} = F.R._{Read} + F.R._{Data\ Retention} + F.R._{Endurance}$$

F.R. is the failure rate. Read, Data Retention, and Endurance define the failure factor.

2.1 Read Failure Rate

Read is the typical failure rate associated with dynamic high temperature life test. In general, EEPROMs have lower, i.e., better read failure rates, because of the screening required to assure low data retention and endurance failure rates.

2.2 Data Retention Failure Rate

Data Retention is the ability of the EEPROM to retain data. For most floating gate structures, the intrinsic data retention duration is so great, e.g., 100's to 1,000's of years, that for all practical purposes the intrinsic data retention failure rate is negligible. Extrinsic data retention duration is a function of endurance and may degrade with accumulated endurance cycles. The extrinsic data retention failure rate is included in the endurance failure rate.

2.3 Endurance Failure Rate

Endurance is the most important failure factor because the endurance reliability is a direct function of the application, i.e., the number of times the device is rewritten during system operation. In other words, the total system life can be compromised by the endurance capability of the EEPROM. (See figure 1). The correct endurance value of the EEPROM must be selected to optimize the system performance. For applications not requiring many rewrites, e.g., BIOS program storage, EEPROMs with a low number of guaranteed endurance cycles provide the best combination of cost and reliability. For applications requiring many rewrites, e.g., data storage or configuration, EEPROMs with a high number of guaranteed endurance cycles provide the best combination of cost and reliability. For all applications, quality, delivery, service, and product assurance are identical for SST EEPROMs.

Endurance is defined as: "The measure of the ability of a nonvolatile memory device to meet its data sheet specifications as a function of accumulated nonvolatile data changes", per the IEEE Std 1005-1991 "IEEE Standard Definitions and Characterization of Floating Gate Semiconductor Arrays". The data sheet specifications include write functionality, data retention, and read access time. For an SST EEPROM, a nonvolatile data change is the completion of an erase/program cycle for each cell, i.e., transferring charge from and to the floating gate in the memory storage transistor.

All floating gate memory cells are subject to 9 possible endurance failure mode major categories (see Table 1). Endurance is unlike other MOS reliability concerns in that the device can be operated within the data sheets limits and eventually an endurance failure will occur. This is because the oxides through which the charge is transferred on and off the floating gate are nominally insulators; however, are subject to electrical stress from the erase and programming operations. The basic endurance failure mechanisms of oxide damage and charge trapping are caused by the cumulative effects of passing a current through the oxide and placing a high electric field across the oxide.

The thickness and quality of the oxide are the primary factors in determining the endurance capability of the device. Thicker oxides have a greater likelihood of measurable charge trapping. Thinner oxides require greater care in processing to reduce defects; initial defects cause yield loss, latent defects cause endurance failures. Erase/program cycling over the lifetime of the system will cause random oxide damage and charge trapping at some constant low level. Design must be such to minimize the stress on the affected oxides; thus, reducing the generated defect and charge trapping rates. Processing must

be such to minimize initial defects and reduce latent defects to the lowest possible level.

Although all floating gate memory cells are subject to the same failure modes, some of the failure modes can be eliminated though process architecture or logic design. SST has patented a memory cell design and associated SuperFlash fabrication process that is less subject to endurance failure modes than competing architectures. In all cases, stressing and testing must assure that defects are identified prior to shipping. The following table summarizes the susceptibility of the major types of flash EEPROMs to the various endurance failure modes:

3.0 Endurance Failure Modes:

The failure modes are defined as follows:

3.1 Stuck Bit

A bit is unable to change and can be stuck in either logic state. Can be caused either by charge trapping or oxide rupture. If caused by charge trapping, the trapped charge may disperse after some time (which can be accelerated by temperature) and the device will regain functionality. The device will go to its intrinsic state (i.e.., no charge on the floating gate) for oxide ruptures. Sometimes referred to a "fast leaky bits". Verified by extended endurance cycling.

3.2 Retention Degradation

The loss of charge of the floating gate caused by either trapped charge or damage in the insulating oxide. Sometimes referred to as "slow leaky bits". This extrinsic data retention duration is verified by a data retention bake after the specified number of endurance cycles.

Table 1: Endurance Failure Modes

Fail Mode	Thin Oxide Stacked Gate	Thin Oxide Two Transistor	Thick Oxide Split Gate (SST)
Stuck Bit	Lo	Hi	Lo
Retention Degradation	Hi	Hi	Lo
Read Time Degradation	Lo	Hi	Lo
Erase Time Degradation	Hi	Lo	Hi
Program Time Degradation	Hi	Lo	Lo
Disturbs			
Overerase	Hi	N/A	N/A
Erase	Hi	Lo	N/A
Program	Lo	Lo	Lo
Read	Lo	Lo	Lo

Note:

1. "Hi" means the technology is comparatively susceptible to the identified failure mode
2. "Lo" means the technology is not
3. "N/A" means the failure mode is "Not Applicable" to that technology

3.3 Read Time Degradation

The gradual decrease in the read access time caused by accumulated trapped charge reducing the cell current or gradual charge loss changing the cell current. Verified by worst case speed testing after endurance and dynamic high temperature life stressing.

3.4 Erase Time Degradation

The gradual increase in the time required to erase the memory caused by accumulated trapped charge. Degradation effects may be avoided by proper guardbanding of erase times or use of iterative erase algorithms with an erase threshold reference circuit.

3.5 Program Time Degradation

The gradual increase in the time required to program the memory caused by accumulated trapped charge. Degradation effects may be avoided by proper guardbanding of program times or use of iterative program algorithms with a program threshold reference circuit.

3.6 Disturbs

Disturbs are an intrinsic phenomena of all memory arrays. A disturb occurs when reading, erasing, or programming one location causes an unwanted change in another location. Floating gate arrays require special considerations in design and processing to minimize unwanted effects of the high voltage used for Fowler-Nordheim tunneling and Channel Hot Electron Injection.

3.6.1 Overerase

A device is unable to read or program correctly because of excessive memory transistor source-drain current, which grounds the bit line read or programming voltage. Overerase is eliminated in two transistor or split gate memory cells by the isolation of the memory transistor from the bit line. Overerase is caused by hole trapping in the oxide, which increases the normal variation in the erase threshold distribution of memory transistors in large arrays, both initially and after erase/program cycling.

3.6.2 Erase Disturb

Unintentionally changing the contents in a non-accessed location, while erasing another location. This occurs because the high voltage required to erase may not be isolated from the non-accessed locations. Erase disturb is impossible to occur in SST devices because all locations, subject to the erase high voltage, are erased simultaneously.

3.6.3 Program Disturb

Unintentionally changing the contents in a non-accessed location, while programming another location. This occurs because the high voltage required to program may not be isolated from the non-accessed locations. Program disturb is minimized by proper design and processing, defects are eliminated through screening.

3.6.4 Read Disturb

Unintentionally changing the contents in a location, while reading that location or another location. This occurs because the voltage required to read may affect other locations. Read disturb is minimized for SST devices by clamping or regulating the word line.

4.0 Summary

An extremely important benefit of the SST SuperFlash EEPROM is the complete elimination of the possibility of "overerase" by use of the split gate isolation or "erase disturb" by use of the page erase feature.

Endurance follows the "bathtub" curve, with a known infant mortality region, a useful life region, and a predictable wearout region. Endurance cycling for screening and for periodic qualification testing has historically been considered the preferred means of verifying capability. Cycling can be performed in real time and may use the actual operating mode of the device or a test mode. Cycling is often combined with voltage or temperature stressing to accelerate infant mortality failures. A significant disadvantage of stacked gate memory devices is the long time required to erase/program; thus, the time to gather reliability and process improvement data is greatly extended.

Although intrinsic data retention duration is essentially infinity, the extrinsic data retention duration is a function of endurance. The endurance failure rate contains the extrinsic data retention failure rate induced by endurance. The intrinsic data retention failure fate is reported independent of endurance.

Test Method 1033 of MIL-STD-883 describes the procedures to be used when performing endurance cycling for screening or endurance performance verification. Various means exist to eliminate infant mortality, which will be a function of product design and the dominant failure mechanism of the process. For example, all EEPROM manufacturing flows contain an infant mortality data retention screen, which is typically an unbiased bake.

Random defects, occurring naturally in the wafer fabrication process, will cause infant mortality endurance or data retention failures. An explicit relationship does not exist that correlates infant mortality with performance in the useful life or wearout regions. Extra memory, called redundancy, improves yields by repairing infant mortality failures in large memory arrays. The localized nature of the random defects causing infant mortality failures, assures the reliability of repaired and non-repaired devices is equivalent.

The endurance failure rate of the EEPROMs in a system will increase in importance as a function of the number of times the system rewrites the EEPROM during system life. System reliability is a function of the failure rate in the specified useful life region of the device, not when the onset of wearout occurs. Given the operating life failure rate of a typical MOS memory is in the order of 100 FITs (.01%/1000 hours), the endurance failure rate contribution should be more than an order of magnitude lower, see figure 1. SST EEPROMs will meet system reliability requirements by providing the lowest endurance and total device failure rate for the specified system lifetime. The greater system reliability lowers the cost of ownership of a SST EEPROM.

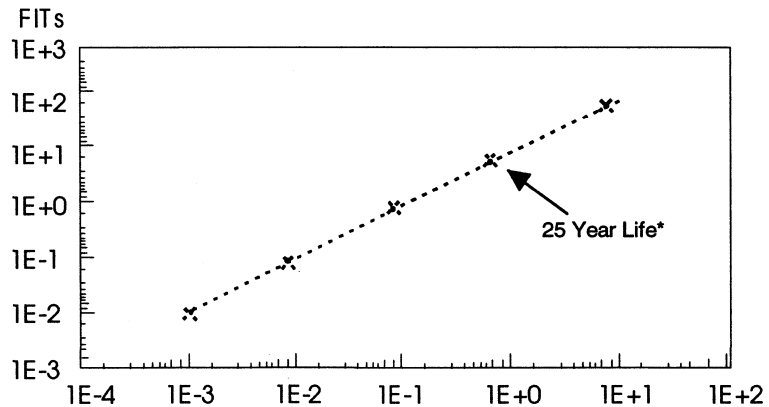


Figure 1: Converting the Endurance Failure Rate in %/1K Cycles to a Failure Rate in Time (FITs)

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Technical Paper

Endurance Testing of EEPROMs

July 1996

Endurance Testing of EEPROMs

1.0 Introduction

Endurance is the cumulative number of erase/program cycles before the device fails a data sheet parameter. Reprogrammable nonvolatile memories, such as flash EEPROMs, have a failure rate associated with endurance that is best represented by the classical "bathtub curve". There are the "infant mortality", "useful life", and "wearout" regions. When attempting to describe the endurance of a device, manufacturers typically claim some number of cycles. In terms of the classical "bathtub" curve, this level is the cumulative number of cycles through the "useful life" region where the cumulative failures are less than a guaranteed value, e.g., 1% for 10,000 cycles. The number of cycles is supposed to be less than the value at the knee of the curve separating the "useful life" region from the "wearout" region. In practice, the stated level should be significantly less than the actual value at the onset of wearout. During the "useful life" region, there will be a small, but constant failure rate. The issue facing manufacturers is to assure each device has been screened to eliminate "infant mortality", has an endurance value greater than the stated level, and the failure rate in the "useful life" region meets industry standards, reference IEEE Std 1005-1991 "Definition and Characterization of Floating Gate Semiconductor Arrays" for additional information.

2.0 Failure Mechanisms

There is lot-to-lot and within-lot variability for endurance failure mechanisms; thus, determination of the individual device endurance value is desirable. Devices can fail during erase/program cycling for a variety of failure mechanisms. In general, the causes for these mechanisms can be grouped into 4 major categories:

2.1 Initial defects

Physical anomalies that cause the device to fail during initial testing or "infant mortality" screening; generally caused by wafer processing defects.

2.2 Latent defects

Physical anomalies that cause the device to fail after some period of operation; generally caused by wafer processing defects.

2.3 Generated defects

Physical anomalies that cause the device to fail after some period of operation, e.g., data retention failures, generally caused by operation of the device, e.g., the TDDB (Time-Dependent-Dielectric-Breakdown) characteristics of thin transfer oxides and the imposed electric fields for erasing or programming.

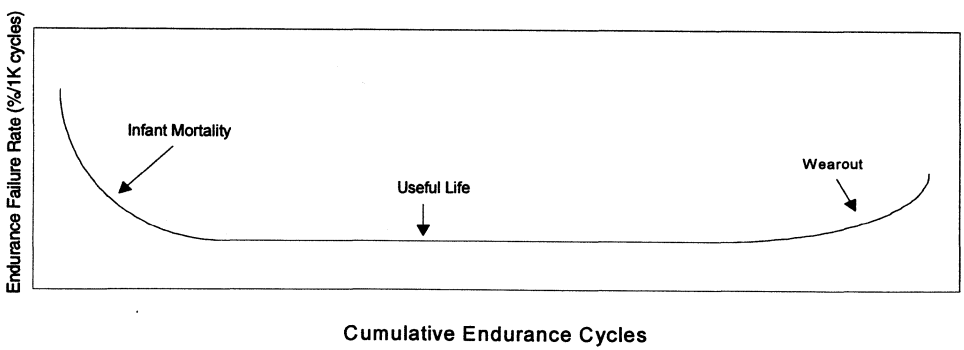

Figure 1: Classical "Bathtub" Curve for Endurance

2.4 Uniform degradation

A steady decline in the performance of a given characteristic that causes the device to fail after some period of operation; generally caused by the deterioration in some physical structure, e.g., from charge trapping.

Initial defects determine the duration and failure rate in the "infant mortality" region. Latent defects establish the failure rate in the "useful life" region. Generated defects and uniform degradation determine the onset of the "wearout" region. Latent and generated defects are random events that are difficult to measure and predict, so that specific devices with different intrinsic endurance values are difficult to identify. Uniform degradation is strongly correlated with explicit memory cell performance characteristics; thus, specific device endurance can be predicted from measurements of each memory cell in the array, and devices can be segregated by endurance values.

The relative frequency of the 4 categories is technology dependent. For example the thin oxide approaches used by Intel, AMD, and Atmel are most susceptible to latent and generated defects, while the thick oxide approach used by SST is most susceptible to uniform degradation.

This means the thin oxide manufacturers have significantly more unpredictability in device-to-device endurance performance and significantly more risk in producing devices or lots with unacceptable endurance values. SST's SuperFlash Technology provides the ability to accurately predict endurance on a device by device basis; thus, segregate by desired endurance levels.

3.0 SST Testing

SST includes erase/program cycling, high voltage and high temperature stressing during the test flow to eliminate the "infant mortality" failures. Additionally, due to the patented unique nature of the SST memory cell, SST includes test routines to compare each memory cell's performance to empirically generated criteria to verify the device meets SST specifications for uniform degradation. This assures each SST lot meets the guaranteed endurance level. The process is very similar to the separation of devices into various speed grades, i.e., device performance is compared to a standard and segregated appropriately. Thus, SST can offer different guaranteed levels of endurance, based on testing of each memory cell in each memory device. SST testing assures each lot meets the guaranteed endurance level and minimizes lot-to-lot variation in endurance performance for all devices shipped to customers.

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Application Note

PCMCIA Memory Cards Made Easy with SST 28PC040

July 1996

PCMCIA Memory Cards Made Easy with SST 28PC040

1.0 Introduction

The emerging mobile computing and communications markets such as palm top, sub-notebook, and PDA (Personal Data Assistant) require rugged and compact storage of data. Different types of storage devices exist; therefore, a standard interface is necessary for intersystem compatibility. The Personal Computer Memory Card International Association (PCMCIA) develops the standard and promotes PCMCIA standard compliant products worldwide. The Association was founded in 1989.

The PCMCIA standard initially was developed for memory cards including RAM, ROM, and flash memory devices. I/O cards standards were included in 1991. The PCMCIA standard defines card physical dimensions, environmental requirements, pin assignments, electrical interface specifications, and software infrastructures. The range of products includes from memory cards and disk drives to fax/modem cards.

A PC Card is a small form-factor card compliant with PCMCIA standards. The size is about that of a credit card with three different thickness':

- Type I (3.3 mm)
- Type II (5 mm)
- Type III (10.5 mm).

Unlike most peripheral cards, PC Cards can be inserted or removed while the system power is on.

The SST 28PC040 is designed for PCMCIA memory card applications and meets all PCMCIA standard electrical requirements. All the required elements built-in on chip, only a few additional passive components are required to assemble a card.

2.0 PCMCIA Memory Card Requirements

A PCMCIA memory card must be compliant with all PCMCIA standards. An electrical requirement is for the card to provide four different bus access modes (see Table 1). Three of the bus access modes are for 8 bits operation. The other bus access mode is for 16 bits operation. A data bus multiplex (mux) function is required on the card to provide all four bus access modes. Usually, a separate multiplexer chip on the card performs this function.

Table 1: PCMCIA Bus Access Mode

Mode	-CE1	-CE2	A_0	D_{15-8}	D_{7-0}
byte	0	1	0	X	even byte
byte	0	1	1	X	odd byte
byte	1	0	X	odd byte	X
word	0	0	X	odd byte	even byte

Note: X is high impedance during a read operation and don't care during a write operation

Another PCMCIA standard requirement is for the PCMCIA memory card to electronically contain information, such as manufacturer name, type of card, and access speed. This is known as the CIS (Card Information Structure). CIS is located in Attribute Memory in the card address space, which is different from the common memory space for storing user data. Usually, a separate low density nonvolatile memory is used for this purpose.

Some nonvolatile PCMCIA memory cards use a battery for SRAM or require a high voltage circuitry for flash memory to achieve nonvolatility and reprogrammability. These require additional components and assembly operations.

All of these requirements must be met within the compact dimensions of the card volume. Thus, board design and component selection becomes a major challenge.

3.0 PCMCIA Flash Memory Cards Built with the SST 28PC040

3.1 The SST 28PC040

The SST 28PC040 is designed for PCMCIA memory card applications. The 28PC040 meets all PCMCIA standard electrical requirements. The data bus multiplexers and CIS storage area are on chip. The SST 28PC040 is a single power supply EEPROM; therefore, does not require a battery or high voltage circuitry to achieve nonvolatility and reprogrammability. The 10x14 TSOP package meets the PCMCIA form factor requirement.

1, 2, and 4 Mbytes memory cards built with the SST 28PC040 tremendously reduce complexity in both hardware and software design because of:

a) the small sector size (512 byte)

b) the single power supply operation (5V-only or 3.3V-only)

c) the built-in address decoder (identified with a different suffix in part number)

d) the build-in data multiplexer

Thus, only a few additional passive components are required to assemble a card. These passive components are resistors (for pull-ups), capacitors (for power decoupling), a connector (to the PCMCIA slot), and a switch (for write protect).

The following table provides some helpful conversions.

Table 2: SST 28PC040 Equivalents

Unit	Equivalent in the 28PC040
1 nibble	4 bits
1 byte	2 nibbles
1 page	256 bytes
1 sector	512 bytes
1 device	2048 pages
1 Mega byte	2048 sectors

3.2 PCMCIA Flash Memory Card Construction

To build a PCMCIA memory card, pairs of 28PC040s are used. The 28PC040 is a nibble organized device, that is the chip has nibble access capability. When the PCMCIA bus executes a byte access to the card, the byte address goes to a pair of chips. Each chip contributes a nibble. When executing a 16 bits bus cycle, each chip provides two nibbles for each byte.

Note, the address and data bus line connecting sequence on PCMCIA connector do not one to one correspond to the connecting sequence on the chip. The interconnection between the PCMCIA connector and a pair of 28PC040 is illustrated in Figure 1.

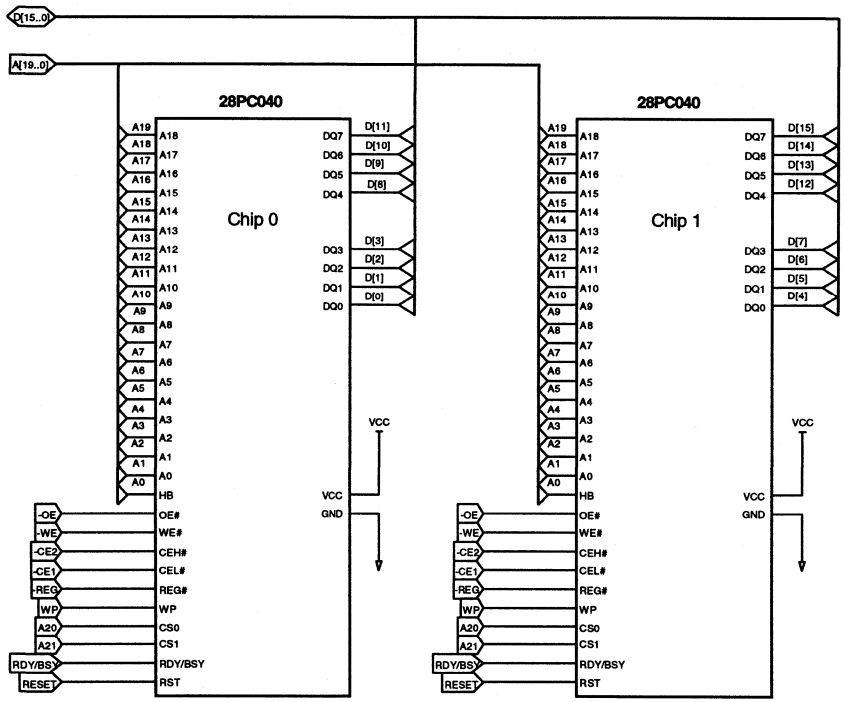

Figure 1: Interconnection between PCMCIA Connector and SST 28PC040

3.3 Pin Descriptions

The table below describes the pins on a SST flash memory card.

Table 3: SST 28PC040 to PCMCIA Card Pinouts

PCMCIA Card Pin	28PC040 Pin	Description
A21	CS1	Chip select, to select one of four pairs of chips.
A20	CS0	Chip select, to select one of four pairs of chips.
A19-A1	A18-A0	Address lines to select a word. The word is provided from two chips. Each chip provides a byte.
A0	HB	Signal to select a byte from a word. A0 on the card is connect to HB (Half Byte) on the chip.
-REG	REG#	Attribute memory space is accessed if this pin is low.
D15-D12	DQ7-DQ4 (chip 1)	Data bits, high order.
D11-D8	DQ7-DQ4 (chip 0)	Data bits, high order.
D7-D4	DQ3-DQ0 (chip 1)	Data bits, low order.
D3-D0	DQ3-DQ0 (chip 0)	Data Bits, low order.
-CE1	CEL#	Chip enable, CEL# will enable DQ3 to DQ0. Since both chips' CEL# are connected to -CE1, D7 to D0 are enabled if -CE1 is asserted.
-CE2	CEH#	Chip enable, CEH# will enable DQ7 to DQ4. Since both chip's CEH# are connected to -CE2, D15 to D8 are enabled if -CE2 is asserted.
-OE	OE#	Output enable, to gate the output buffers for a read operation
-WE	WE#	Write enable, to control the write operation.
RDY/BSY	RDY/BSY	Indicates device is busy, active low.
RESET	RST	Hardware reset
VCC	VCC	Power supply
GND	GND	Ground

3.4 Nonconforming Page Map

Due to the finite endurance of any flash device, each sector will eventually fail. Therefore, dynamic reassignment of nonconforming sectors is an important function to achieve a reliable flash memory card. The nonconforming sector management for a flash file system becomes an essential function.

(Note a sector consists of one page from each 28PC040 in the pair.)

3.4.1 Nonconforming Page Map on an SST 28PC040 Chip

The nonconforming maps in a 28PC040 chip provide a map of those sectors that are not conforming to specifications. On each chip, there are two nonconforming maps. One map is for all the even pages. The other map is for all the odd pages (see Tables 2 and 3). The maps are located in Attribute Memory space address 200 (hex) to 2FF (hex) and 300 (hex) to 3FF (hex) respectively. Note, only data bits D3 to D0 are used. Data bits D7 to D4 are reserved by SST for future usage. A data bit in the map represents the status of the corresponding page in Common Memory space. A bit in the map with a '0' means the corresponding page is not recommended to use.

A Sum of the number of Nonconforming Pages (SNP) is also provided and is calculated by summing the "0's" in the last 254 nibbles of the nonconforming page map. Since the SNP occupies the first 8 bits of the map, the status of the first 8 even pages as well as the first 8 odd pages are not reflected in the nonconforming maps. These pages are guaranteed to be good pages when the chips are shipped.

For example, if there are three nonconforming pages on a chip, located at page 10 (hex), 11 (hex) and 12 (hex). On the even page nonconforming map, a "0" will be at attribute memory byte 202 (hex) bit D0 and another "0" will be at attribute memory byte 202 (hex) bit D1 (refer to Table 4). On the odd page nonconforming map, a "0" will be at attribute memory byte 302 (hex) bit D0 (refer to Table 5). There are two even nonconforming pages. The SNP for even pages is 2, i.e., SNP byte 200 (hex) will be xxxx0010 (binary) and SNP byte 201 (hex) will be xxxx0000 (binary). The SNP for odd page is 1, i.e., SNP byte 300 (hex) will be xxxx0001 (binary) and SNP 301 (hex) will be xxxx0000 (binary). Whenever the nonconforming map is referenced, the SNP should be compared to the sum of the "0's" in the remaining nibbles of the nonconforming map. If they do not match, the chip is in an unknown state and should not be used. (Note, the nonconforming maps are for use of manufacturing only and the end user should not alter these maps.)

Table 4: Nonconforming Page Map For Even Pages on SST 28PC040

Attribute Memory Byte Address	Data Bit Each bit represents corresponding EVEN page status (page number in hex)							
	D7	D6	D5	D4	D3	D2	D1	D0
200	x	x	x	x	SNP[3:0]			
201	x	x	x	x	SNP[7:4]			
202	x	x	x	x	16	14	12	10
203	x	x	x	x	1E	1C	1A	18
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
2FE	x	x	x	x	7F6	7F4	7F2	7F0
2FF	x	x	x	x	7FE	7FC	7FA	7F8

Table 5: Nonconforming Page Map For Odd Pages on SST 28PC040

Attribute Memory Byte Address	Data Bit Each bit represents corresponding ODD page status (page number in hex)							
	D7	D6	D5	D4	D3	D2	D1	D0
300	x	x	x	x	SNP[3:0]			
301	x	x	x	x	SNP[7:4]			
302	x	x	x	x	17	15	13	11
303	x	x	x	x	1F	1D	1B	19
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
3FE	x	x	x	x	7F7	7F5	7F3	7F1
3FF	x	x	x	x	7FF	7FD	7FB	7F9

3.4.2 Nonconforming Page Map on the PCMCIA Card

After the 28PC040 chips are assembled to become a PCMCIA memory card, the non-conforming maps in 28PC040 chips can be utilized by a file system software to perform sector reassignment or by a data base software to avoid using these sectors. Because the address and data lines on the card are reassigned (see Figure 1), the nonconforming maps read from the PCMCIA interface must be interpreted. Since address lines are shifted by one bit on the card, the nonconforming maps are located at 400 (hex) and 600 (hex) in the Attribute Memory on the card. Since data lines on the card are arranged in a nibble (4 bits) fashion, the nonconforming maps are located in even bytes only and each nibble for a byte is contributed by two different chips (see Table 6 and Table 7). A sector (512 bytes) is formed by two pages (256 bytes each) contributed from the two paired chips. Therefore, a good sector on the card must have both pages good on a pair of chips, i.e., a good even sector must have both even pages good, a good odd sector must have both odd pages good. The file system software must reassign sectors or avoid using sectors when either page in the nonconforming page map contains a "0".

For example, if 512 bytes are read from Attribute Memory space at 400 (hex) to 5FF (hex) on the card. In these 512 bytes, there are two nonconforming maps. By separating the upper nibbles and lower nibbles into two groups and combining nibbles into bytes, two even page nonconforming maps are obtained. One from chip 0 is formed by the lower nibbles. The other one from chip 1 is formed by the upper nibbles. They have the same format shown as Table 4. Following the same procedure for Attribute Memory space at 600 (hex) to 7FF (hex), two odd page nonconforming maps can be obtained shown as Table 5. To determine a good sector, both pages in that sector must be good. For example, if Attribute Memory byte 404 (hex) data bit D0 and D4 both are "1", sector 10 (hex) on the card is a good sector. On the other hand, either of these bits is "0" then sector 10 (hex) should not be used. Whenever the nonconforming map is referenced, the SNP should be compared to the sum of the "0's" in the remaining nibbles of the nonconforming map. If they do not match, the chip is in an unknown state and should not be used.

Table 6: Nonconforming Page Map for Even Pages on a PCMCIA Card

Attribute Memory Byte Address	Data Bit Read From PCMCIA Interface Each bit represents corresponding chip's EVEN page status (page number in hex)							
	Contributed by Chip 1				Contributed by Chip 0			
	D7	D6	D5	D4	D3	D2	D1	D0
400	SNP[3:0]				SNP[3:0]			
401	x	x	x	x	x	x	x	x
402	SNP[7:4]				SNP[7:4]			
403	x	x	x	x	x	x	x	x
404	16	14	12	10	16	14	12	10
405	x	x	x	x	x	x	x	x
406	1E	1C	1A	18	1E	1C	1A	18
407	x	x	x	x	x	x	x	x
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
4FC	7F6	7F4	7F2	7F0	7F6	7F4	7F2	7F0
4FD	x	x	x	x	x	x	x	x
4FE	7FE	7FC	7FA	7F8	7FE	7FC	7FA	7F8
4FF	x	x	x	x	x	x	x	x

Table 7: Nonconforming Page Map for Odd Pages on a PCMCIA Card

Attribute Memory Byte Address	Data Bit Read From PCMCIA Interface Each bit represents corresponding chip's ODD page status (page number in hex)							
	Contributed by Chip 1				Contributed by Chip 0			
	D7	D6	D5	D4	D3	D2	D1	D0
600	SNP[3:0]				SNP[3:0]			
601	x	x	x	x	x	x	x	x
602	SNP[7:4]				SNP[7:4]			
603	x	x	x	x	x	x	x	x
604	17	15	13	11	17	15	13	11
605	x	x	x	x	x	x	x	x
606	1F	1D	1B	19	1F	1D	1B	19
607	x	x	x	x	x	x	x	x
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
6FC	7F7	7F5	7F3	7F1	7F7	7F5	7F3	7F1
6FD	x	x	x	x	x	x	x	x
6FE	7FF	7FD	7FB	7F9	7FF	7FD	7FB	7F9
6FF	x	x	x	x	x	x	x	x

3.4.3 Dynamic Error Mapping

Standard error mapping techniques may be used to identify and map nonconforming sectors generated during normal operation of the card. Storage of this information is separate from the nonconforming page mapping performed during 28PC040 and PCMCIA card manufacturing.

4.0 PCMCIA Software Requirements

In order to simplify and isolate software interface design efforts, the PCMCIA standard defines two software layers: Socket Services and Card Services.

4.1 Card Services

The Card Services provide an interface that allows PC Cards and sockets to be shared by multiple clients. Clients are the programs that access Card Services. They may be device drivers, configuration utilities, or application programs. (see Figure 2)

4.2 Socket Services

The Socket Services provide both the hardware and software interfaces for the host computer to use the PC Cards and sockets. Thus, Card Services do not need to directly interrogate the PC Cards or sockets for configuration or functionality information (see Figure 2).

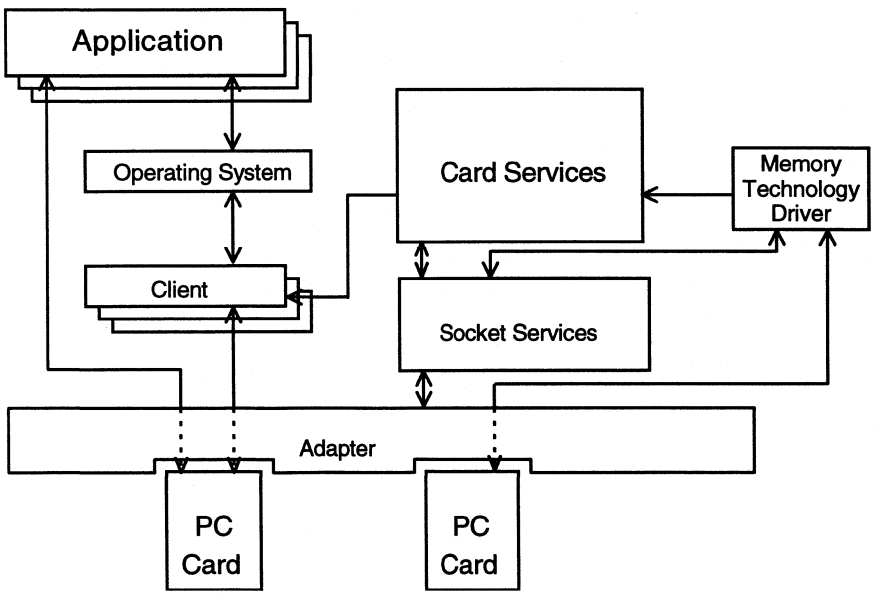

Figure 2: PCMCIA Software Architecture (Courtesy of PCMCIA Standard Card Services pp. 3-3)

4.3 Software Support for Card and Socket Services

Card services and Socket Services software are supported by major software companies. The following table lists some of the software vendors that provide Card Services and Socket Services and the appropriate contact person to answer questions (see Table 8).

4.4 Software Support for Flash Memory Cards

While most memory cards may be read using static-RAM (SRAM) read instructions and timing, special programming algorithms are required to program or erase a flash memory card. Card Services hides the details of what is required to write the flash memory card from the client through use of the Memory Technology Drivers (MTD). MTD implements the specific erase and programming algorithms required to alter flash memory devices.

For the latest information on support of Memory Technology Drivers for the 28PC040, please contact SST.

Since some flash memory devices have a larger block than a traditional file system can handle, special file systems have been developed to accommodate this difference, such as the Flash File System (FFS, FSS II), or Flash Translation Layer (FTL). These programs not only can handle a larger data block but also implement some features to improve flash memory device performance and reliability such as wear leveling and sector reassignment.

Note, the SST 28PC040 uses a small sector size; therefore, many of these special routines are not required for efficient operation of a 28PC040 PCMCIA card.

Table 9 lists a software vendor that provide FTL flash file system for SST 28PC040 and the appropriate contact person to answer questions.

For the latest information on support of FFS or FLT for the 28PC040, please contact SST.

5.0 Summary

By using the SST 28PC040 EEPROM memory chip, a PCMCIA flash memory card can be easily built with the least number of components. The 28PC040 PCMCIA flash memory card requires no external address decoders, data multiplexers, or additional EEPROM. Software support, conforming with all PCMCIA standards, is available. The card manufacturer can license software from those suppliers, and can bundle the software with the card for "user friendly" operation.

Table 8: Card Services and Socket Services Vendors

Vendor Name	Product Name	Contact person	Phone Number
AMI	CardZ	Mark Huffman	770-246-8625
Award	CardWare	Bill Goodrich	415-968-4433
Phoenix	PCM+	Margaret Kahnke	714-440-8052
Systemsoft	CardSoft+	Peter Wansick	508-647-2921

Table 9: FLT Vendor

Vendor Name	Product Name	Contact person	Phone Number
Datalight	CardTrick	Tim Gillman	1-800-221-6630

Application Note

SST EEPROM—29EE010
An Ideal Solution to Plug and Play BIOS

July 1996

SST EEPROM—29EE010
An Ideal Solution to Plug and Play BIOS

1.0 Introduction To Plug and Play

PCs are being used in a wide variety of applications and have become the primary business tool. Configuring PC hardware and software to work with different networks and with different peripheral devices is a significant problem. Changing the hardware configuration of a machine is a task that few end-users attempt and even trained technicians find this a difficult, time consuming, and frustrating task. A broad base of companies within the computer industry is addressing these problems with a technology known as the Plug and Play architecture.

A Plug and Play system has the following characteristics.

a) Any installation is a simple fail-safe operation, because users simply plug a new device in, turn on the system, and the device works.

b) Users do not need to modify expansion card jumper settings or modify operating system configuration files.

c) Plug and Play systems accommodate dynamic configuration changes. This characteristic is critical for mobile systems, since users of laptops and notebook computers need the ability to plug into corporate networks via docking stations without turning the computer off to reconfigure hardware and software.

For the next few years, there will be a transition period during which systems will contain both non-Plug and Play adapter cards ("legacy cards") and Plug and Play adapter cards. The Plug and Play BIOS must have the capability to handle the configuration of systems using both types of cards. This flexibility requires the use of reprogrammable nonvolatile memory for the implementation of the necessary Plug and Play BIOS routines.

2.0 Plug and Play BIOS Requirements

During the transition period, reprogrammable nonvolatile memory is required to implement Plug and Play BIOS. The three critical areas needing the reprogrammable nonvolatile memory that are addressed by the Plug and Play BIOS are:

- resource management
- run-time configuration
- extended configuration services

2.1 Resource Management

Resource management provides the ability to manage the fundamental system resources, which include DMA, Interrupt Request Lines (IRQs), I/O and Memory addresses. A Plug and Play BIOS plays a vital role in managing these system resources and ensuring a successful launch of the operating system. As a resource manager, the Plug and Play BIOS is responsible for configuring Plug and Play cards and system board devices during power-up. System board devices include the Programmable Interrupt Controller (PIC), DMA Controller, System Timer, Keyboard Controller, Integrated Video Controller, and Floppy Controller.

2.2 Run-time Configuration

Run-time configuration is a new feature incorporated into the Plug and Play BIOS, which provides the ability to dynamically change the resources allocated to system board devices after the operating system has been loaded.

2.3 Extended Configuration

Extended configuration services are mechanisms whereby the system software specifies the system resources assigned to various devices that have been installed in the system. There are two ways of implementing such services depending on whether the user wants to store information on "overall" resource usage, or whether the user wants to store specific "individual" resource usage for every device in the system.

2.3.1 "Overall" Resource Usage Support

"Overall" resource usage support describes the cumulative usage of system resources by all legacy cards, but does not identify the specific resources used by each card. Only summary resource usage information by the legacy cards must be stored in nonvolatile memory.

2.3.2 "Individual" Resource Usage Support

"Individual" resource usage support detailed configuration information for all devices is stored in nonvolatile memory. The Extended System Configuration Data (ESCD) structure format allows the storage of detailed configuration information on a per device basis. The ESCD format describes every device in the system. A typical platform requires 4K bytes of reprogrammable nonvolatile memory to store the ESCD

information. The storage of the detailed configuration information allows the BIOS configuration software to work together with configuration utilities to provide robust support for non-Plug and Play as well as Plug and Play devices.

3.0 Plug and Play BIOS Implementation

About 100K bytes of nonvolatile memory are required to store the BIOS code for a typical desktop system. Plug and Play BIOS implementation requires 4K bytes of nonvolatile memory with ***in-system reprogrammability*** to store ESCD.

There are various implementation options for storing Plug and Play BIOS and ESCD. These options are separated into two categories:

- multiple chip solution (see Figure 1)
- single chip solution (see Figure 2)

3.1 Multiple Chip Solution

The multiple chip solution involves using two different types of nonvolatile memories, traditional UV EPROM with some type of in-system reprogrammable nonvolatile memory.

3.1.1 UV-EPROM or Bulk Erasable Flash EPROM with a 4K byte EEPROM

This implementation uses one UV-EPROM or bulk eras-able flash EPROM to store the BIOS code. In addition, at least a 4 K byte EEPROM is used to store the ESCD. If a bulk erasable flash EPROM is used, a high voltage power supply is required to update the BIOS code in-system.

3.1.2 UV-EPROM or Bulk Erasable Flash EPROM with a 4K Byte Battery Backed-up SRAM

This implementation uses one UV-EPROM or bulk eras-able flash EPROM to store the BIOS code. In addition, a 4K byte battery backed-up SRAM is used to store the ESCD. A custom Real Time Clock(RTC) chip with 4K bytes of SRAM may be used. If a bulk erasable flash EPROM is used, a high voltage power supply is required to update the BIOS code in-system.

Currently and for the foreseeable future, there will be frequent changes to the BIOS. Thus, the UV-EPROM is not practical because the BIOS cannot be updated in-system. The multiple chip solution is not cost effective because of the cost of the 2 required devices and the development of a special well regulated 12 volt power supply.

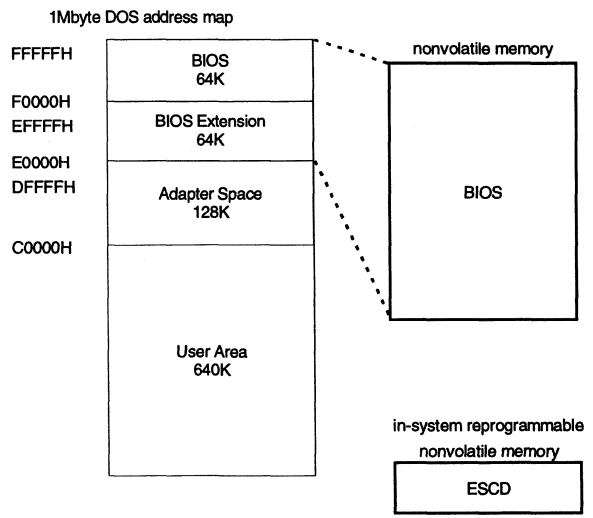

Figure 1: Multiple Chip Solution

3.2 Single Chip Solution

In traditional PC design, the BIOS code stored in nonvolatile memory is copied into system DRAM during system boot up to improve system performance. This DRAM space is known as shadow memory. The shadow memory windows can be selected either by the user or application program. For normal operation, BIOS and ESCD may be shadowed. In order to update the BIOS or ESCD data in the nonvolatile memory, the BIOS or ESCD data area can not be shadowed. The BIOS and ESCD update codes must be executed from system DRAM during the nonvolatile memory programming period. By having the ability to unshadow the BIOS or ESCD data area during programming, a single chip solution can be realized to store both BIOS code and ESCD data on the same nonvolatile memory chip (see Figure 3).

3.2.1 Boot Block Flash EPROM

This implementation uses a boot block flash EPROM for both BIOS and ESCD. A 4K parameter block is used to store the ESCD while rest of the space is used to store the BIOS code. The boot block flash EPROM requires an additional well regulated 12 volt power supply to update the BIOS in-system. The software programmer must rigorously group the BIOS subroutine in order to obtain the flexibility for a BIOS update. This rigorous grouping generates many unused memory fragments and delays the time-to-market. The boot block flash EPROM requires the ESCD data area to be restricted to specific locations. The complexity of the grouping and identification of the specific ESCD location significantly increases software development costs and time compared with using a page alterable EEPROM.

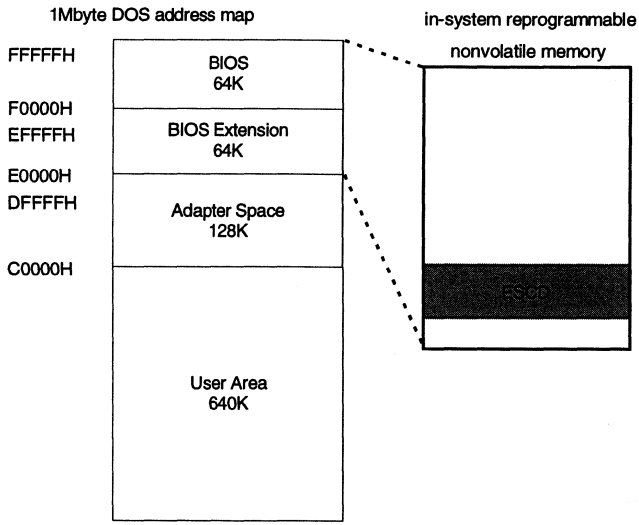

Figure 2: Single Chip Solution

3.2.2 SST 1M bit EEPROM (29EE010)

This implementation uses an SST 1M bit page alterable EEPROM(29EE010) for both BIOS and ESCD. This EEPROM provides a low cost single chip solution featuring 128 byte page writeability with a single 5 volt or single 3.3 volt power supply. Unlike the boot block device, the software programmer has full flexibility to utilize any of the 1024 pages to store BIOS or ESCD data. Each 128 byte page of the SST 29EE010 is a completely secure block(sector). The 29EE010 is pin compatible with existing BIOS hardware implementations; therefore, no hardware changes are required to replace the existing nonvolatile memory. The 29EE010 simplifies design and enhances system performance for BIOS or ESCD updating.

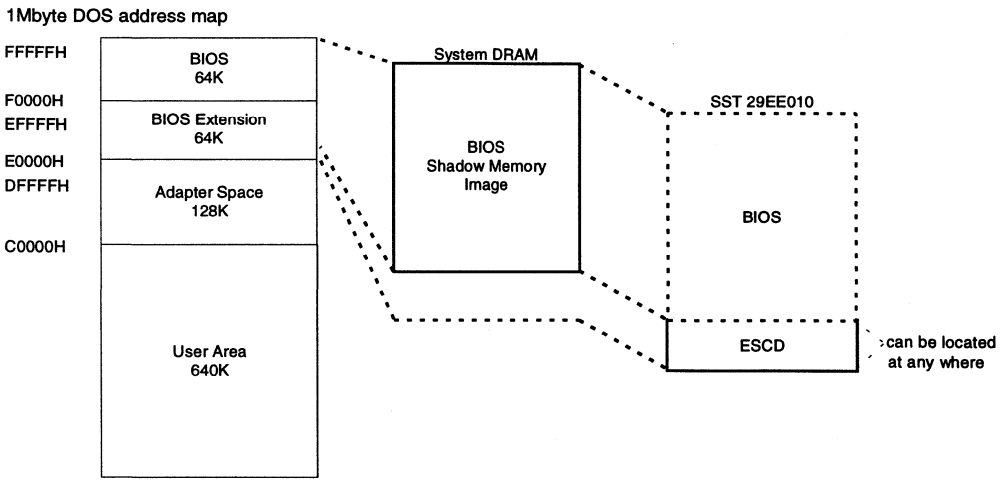

Figure 3: Shadow Memory Scheme During ESCD Updating

4.0 SST 29EE010 — The Superior Choice

The SST's 29EE010 outperforms all other implementations. The small page size (128 byte) and the single power supply (5V or 3.3V) provide a low cost, flexible, and effective system implementation for the Plug and Play BIOS application. Software can have the flexibility to use any of the 1024 page locations to store ESCD data or BIOS code.

The device provides Software Data Protection to prevent inadvertent writes. Setting the Software Data Protection makes every single page as secure as a "boot block".

This JEDEC standard Software Data Protection method has been fully proven by the acceptance of more than 100 million EEPROM devices shipped by several vendors over the past 9 years. SST's single chip solution provides reliability, flexibility, and manufacturability.

Table 1: BIOS Plug and Play Comparison for Different Implementations

Features	SST EEPROM 29EE010	Bulk Erasable flash EPROM + EEPROM	Bulk Erasable flash EPROM + RTC chip (w/SRAM)	Boot block flash EPROM
Additional cost to implement Plug and Play BIOS	**None**[1]	Yes	Yes	Yes[2]
Requires additional PCB area	**No**	Yes	No	No
Flexibility of relocating ESCD address	**Yes**	Yes[3]	No	No
Flexibility of changing ESCD size	**Yes**	No[4]	No[4]	No
Protection of boot recovery code area	**Yes**	No	No	Yes
Requires well regulated 12 volt power supply	**No**	Yes	Yes	Yes
Software development complexity	**Low**	Very Low	Very Low	Moderate

Notes:

1. Systems previously using EPROM with /PGM connected to pin 31 do not have any hardware changes; i.e., the /PGM signal in now the /WE signal. If /PGM was not connected, e.g. the EPROM was an OTP, then a jumper is required from /WE to pin 31.
   Note: V_{PP} (pin 1) is a no connect for the SST 29EE010; Therefore, the presence of Vpp has no effect
2. Premium for boot block flash EPROM vs. bulk erasable flash EPROM
3. Only within the boundaries of the EEPROM address space
4. Must change EEPROM or RTC(w/SRAM) density

Application Note

Safe Updating With SST EEPROM Memory

July 1996

Safe Updating With SST EEPROM Memory

1.0 Introduction

A major advantage of flash memory is the ability to update BIOS and boot programs electronically in-system. A major concern is the minimum size of the erase element in the flash EPROM memory. A large erase element, e.g., 4K or more bytes, increases the risk of system failure, if the flash memory is erased and reprogrammed.

EEPROM memory as supplied by SST eliminates problems associated with the bulk flash or boot block flash EPROM devices.

2.0 Problems with Bulk Erasable Flash Memories

The stacked gate bulk-erase flash EPROM, e.g., 28F010, requires the entire memory to be erased prior to altering any programmed byte. This can take 10 or more seconds of system time and requires additional system memory of 131,072 or more bytes.

During the long time required for erasing and reprogramming, a power outage or other noise transient on the 5 volt or the flash specific specially regulated ± 5% 12 volt power supply, can mis-load or inadvertently write the flash.

A catastrophic system failure occurs when the system cannot re-start due to the loss of the boot program. The large amount of memory to be erased and reprogrammed necessitates additional system disk or RAM space to store existing and new programs during the altering of the flash memory contents. When reprogrammed, stacked gate devices are subject to "overerase", which causes a column to fail. For a bulk-erase device, this will affect the entire contents of the memory, including the boot program and cause nonrecoverable system failures.

3.0 Solutions with Block Erasable Flash Memories

The stacked gate sector or boot block flash EPROM, e.g., 28F001BX, is divided into several large erase sectors that are independent of each other. These erase sectors can provide a secure block., i.e., each individual sector should not be affected by erase, programming, or "overerase" in other sectors. "Overerase" can only occur in those sectors that are rewritten, which then fails a column in the rewritten sector; thus, the sector containing the boot code can be protected.

3.1 Problems with Block Erasable Flash Memories

These devices have very large sectors; therefore, the system must provide a comparable large buffer to hold the contents of the sector to be reprogrammed. These devices only program byte-by-byte; therefore, a long time is required for the buffer memory to store the new data. With the large sectors, even if only 100 bytes need to be altered, the entire sector must be erased and reprogrammed.

Some devices have a sector protection mode to prevent inadvertent erasing or programming of the sector contents. These devices use a high voltage to enter the protected mode. The use of a programmer to provide the high voltage requires an additional insertion during the board assembly process.

4.0 The SST Complete Solution

The SST 29EE010 single power supply split gate page mode EEPROM eliminates all of these problems with stacked gate bulk or block erasable flash memories:

4.1 Can't Be Overerased

The SST 29EE010 cannot "overerase" and lose an entire column; thus, there will be no catastrophic system failures caused by a bad column, as in either the bulk or sector erasable flash EPROM.

4.2 Single Power Supply

The SST single power supply 29EE010 is written, using an instruction with SRAM like timing signals, to individual pages, each consisting of 128 bytes. The 128 bytes are loaded at normal read rates, i.e., measured in nanoseconds; then, the page is typically written in less than 5 ms; therefore:

a) No additional system disk or RAM memory is needed, in order to alter and verify the flash memory contents.

b) The fast page load and write times minimize exposure to inadvertent power outages or noise transients; thus, increasing the reliability of the loaded data.

c) No special ± 5% regulated 12 volt power supply is required.

4.3 JEDEC Standard Software Data Protect

The use of JEDEC standard Software Data Protection (SDP) assures that memory contents are only altered when the specific desired page to be written is accessed; thus, every page is protected. This protection scheme uses a 3-byte sequence to protect the device and to enter the write mode for a given page. Every page is completely isolated from every other page and can only be altered when the 3-byte instruction is given. This JEDEC standard Software Data Protection method has been fully proven by the acceptance of more than 100 million EEPROM devices shipped by several vendors over the past nine years.

4.4 Global Protection

SDP is a global command that implements the every page protection scheme the first time the 3-byte sequence is issued. Recommended practice is not to disable SDP when performing a write, but to use the 3-byte sequence every time a page is to be altered. SDP is implemented with a single power supply using software instructions; therefore, the use of a programmer is not required, e.g., the 29EE010 can be written during the board testing process.

5.0 Summary

The SST 29EE010 **provides better security** than a boot block for protection against inadvertent write and "overerase", yet with increased user flexibility due to the small page size and use of the standard single 5 volt power supply.

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Application Note

Manufacturer ID Software Entry Considerations

July 1996

Manufacturer ID
Software Entry Considerations

1.0 Introduction

The increasing variety and availability of EEPROMs with different erase and program methods has necessitated a means of identifying the manufacturer and device in system. Historically, programmers used high voltage to interrogate for this information from the device, but high voltages are not practical for in-system applications. Thus, a software means of device identification was developed. Unfortunately, there is no JEDEC standard for software identification and multiple means of entry have been created.

The purpose of this note is to discuss the methods to ease the use of multiple means of software ID, with no impact on device performance or reliability.

2.0 Entry Methods

All 5 volt only EEPROM manufacturers use some form of the JEDEC standard optional Software Data Protection (SDP) sequence to initiate a software manufacturer's ID entry. SST 1 megabit devices use the 6 byte SDP-like sequence, while other manufacturers use a 3 byte SDP-like sequence.

3.0 Concerns

The three possible outcomes when entering the manufacturer's ID mode are:

a) The device correctly enters the mode.

b) The device becomes non-accessible (only Data Bar Polling or Toggle Bit function) for a period of time, then returns to the normal read mode.

c) The device inadvertently writes to a page address defined in the SDP-like sequence.

The last outcome is the only one to possibly impact device or system performance.

4.0 Prevention

The SDP feature should always be used with 5 volt only EEPROMs. When SDP is enabled, no write command will be executed, unless preceded by the SDP enable sequence. If a write command is executed without the SDP sequence, then the device will be non-accessible for some period of time. Additionally, SST will recognize an invalid SDP like sequence, i.e., the last byte is incorrect, and enter the non-accessible state. For SST, this non-accessible time is typically 300 µs. Other manufacturers have longer or shorter times. In no case, will the contents of the memory be altered. After the expiration of the non-accessible time, the device will read the contents of the location accessed by the address bus (assuming the device is placed in the normal read mode). This will be "FF" for devices as shipped.

5.0 Recommendation

All 5 volt EEPROMs should be used with SDP enabled (see Figure 1.) In order to maximize system efficiency when entering the manufacturer's ID mode, the device with the longest non-accessible time should be attempted first. If the output is not correct, then the device with the next longest non-accessible time should be attempted. For example, if brand A has a non-accessible time of 100 ns and SST has a time of 300 µs, then the system should use the SST method of manufacturer's ID entry first.

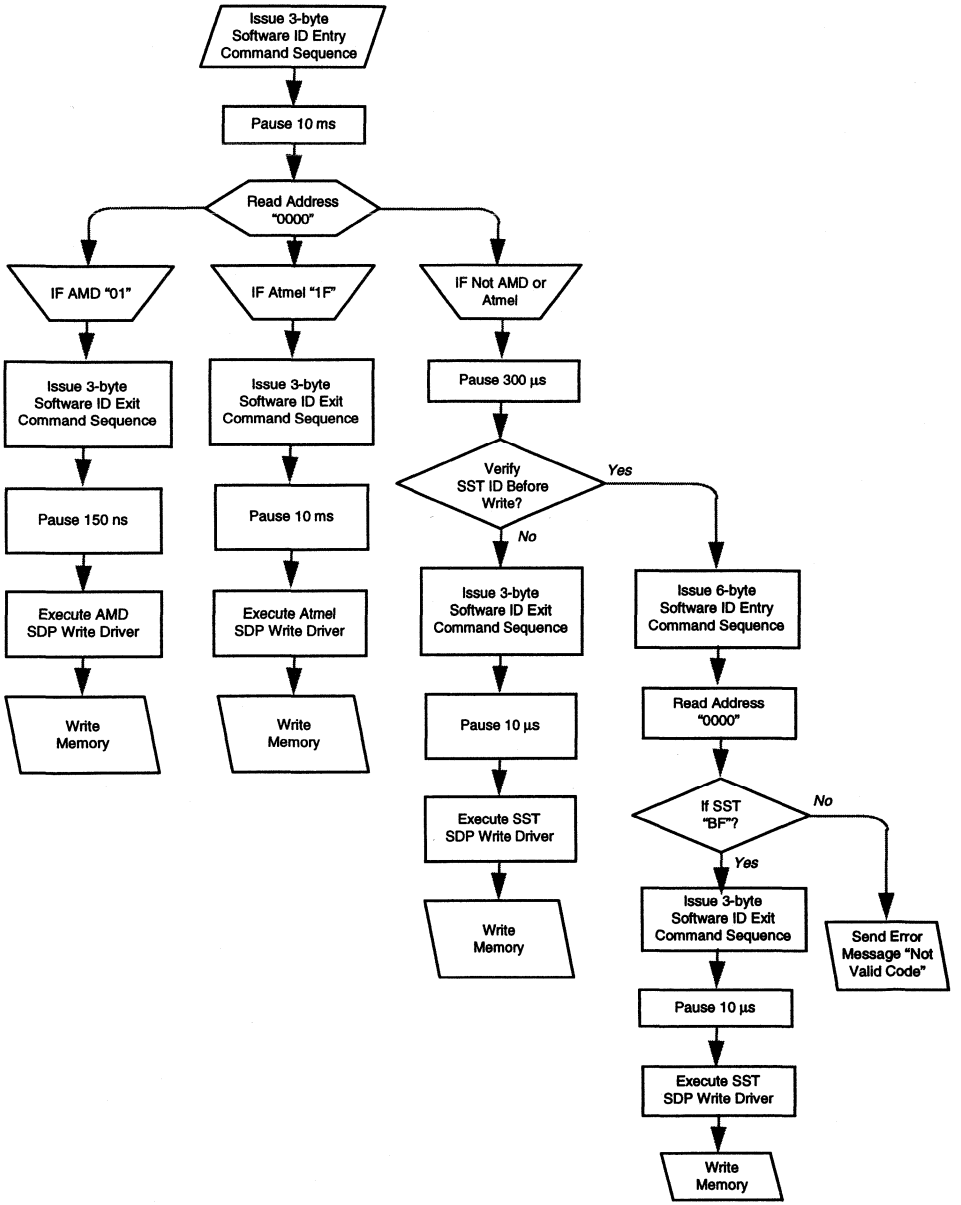

Figure 1: Manufacturer ID Selection Flow Chart

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Application Note

SST 28SF040
4 Megabit SuperFlash EEPROM
Command Interrupt Recovery

July 1996

SST 28SF040
4 Megabit SuperFlash EEPROM
Command Interrupt Recovery

1.0 Introduction

The SST 28SF040 SuperFlash EEPROM offers the ease of 5V-only reprogrammability along with the operational safety provided by the use of command registers. The command registers (non read) of the 12 volt flash EPROM devices require that 12 volts be present on Vpp for the registers to be active. The command registers of the 28SF040 are active in the normal V_{CC} operating range. Inadvertent commands or command sequence interrupts could cause the 28SF040 to be in a recoverable non-accessible state. The purpose of this application note is to provide a recognition method for this non-accessible state and a simple method to exit this state.

2.0 Device Operation

There are seven command operations used to initiate the memory operation functions of the device. They are 1) Sector_Erase, 2) Chip_Erase, 3) Byte_Program, 4) Reset, 5) Read_ID, 6) Software Data Protect, and 7) Software Data Unprotect.

The Software Data Protect and Unprotect command operations are read sequences. The device invokes these modes only upon the completion of seventh (last) byte. Any violation to the exact sequence of address cancels the mode and the 28SF040 remains in the read mode.

The Read_ID command operation has only one command to enter the mode and therefore cannot be in a non-accessible state. However the device will remain in the Read_ID mode until a Reset command has been issued. No main memory operation can be performed while in the Read_ID mode. The Reset command operation reinitializes the command registers and returns the device to the Read mode.

The Sector_Erase, Chip_Erase, and Byte_Program command operations can put the 28SF040 into a non-accessible state, if the command sequence is not properly carried out. These are two command operations, setup followed by execute, each with a specific sequence. An inadvertent command is defined as an erroneous command sequence (e.g., a setup command sent by the user for an operation not desired by the user, who wants to exit this operation without executing it).

2.1 Sector_Erase Operation

The Sector_Erase operation is initiated by a setup command and an execute command. The setup command stages the device for electrical erasing of all bytes within a sector (256 bytes). The setup command is performed by writing (20H) to the device. To execute the sector-erase operation, the execute command (D0H) must be written to the device. The erase operation begins with the rising edge of the WE# pulse and is terminated automatically by using an internal timer.

When the setup command is sent to the 28SF040, the device's I/Os enter a high impedance state and will only accept data. This normally is not an issue since an execute command will follow and the device will perform a sector erase. However if due to either a command sequence interrupt (e.g., a CPU interrupt) or an inadvertent command initiation, only the set-up command is sent, the 28SF040 will remain in the high impedance (non-accessible) state and the device cannot be read.

2.2 Chip_Erase

The Chip_Erase operation is initiated by a setup command and an execute command. The setup command stages the device for electrical erasing of all bytes within the 28SF040 (512K bytes). The setup command is performed by writing (30H) to the device. To execute the chip-erase operation, the execute command (30H) must be written to the device. The erase operation begins with the rising edge of the WE# pulse and is terminated automatically by using an internal timer.

When the setup command is sent to the 28SF040, the device's I/Os enter a high impedance state and will only accept data. This normally is not an issue since an execute command will follow and the device will perform a chip erase. However if due to either a command sequence interrupt (e.g., a CPU interrupt) or an inadvertent command initiation, only the set-up command is sent, the 28SF040 will remain in the high impedance (non-accessible) state and the device cannot be read.

2.3 Byte_Program Operation

The Byte_Program operation is initiated by writing the setup command (10H). Once the program setup is performed, programming is executed by the next WE# pulse. The address bus is latched on the falling edge of WE#, CE#, or the rising edge of OE#, whichever occurs last. The data bus is latched on the rising edge of WE#, CE#, whichever occurs first. The programming operation begins with either the rising edge of WE#, CE#, whichever occurs first. The program operation is terminated automatically by an internal timer.

When the setup command is sent to the 28SF040, the device's I/Os enter a high impedance state and will only accept data. This normally is not an issue since an execute operation (WE# toggling) will follow and the device will perform a byte program. However if due to either a command sequence interrupt (e.g. , a CPU interrupt) or an inadvertent command initiation, only the set-up command is sent, the 28SF040 will remain in the high impedance (non-accessible) state and the device cannot be read.

3.0 Non-Accessible State Detection

The 28SF040 enters into a non-accessible state when the I/Os are at high impedance (i.e., will read as "FF"). The 28SF040 will not read correctly in this state. When the application detects an unexpected "FF" state, reread the device twice more. If the device does not read correctly, then the device could be in the non-accessible state.

4.0 Reset Operation

A simple way to exit the 28SF040 from the non-accessible state is to issue a Reset command. When the CPU interrupts either a Sector_Erase, a Chip_Erase, or a Byte_Program sequence, a Reset should be sent before beginning any operation on the 28SF040. If a 28SF040 should be in the non-accessible state (as described in the previous paragraph), a Reset should be issued.

The Reset command is provided as a means to safely abort the erase or program command sequences. Following any setup command (erase or program) with a write of (FFH) will safely abort the operation. Memory contents will not be altered. The Reset command returns the device to the read mode. The Reset command does not enable Software Data Protect.

5.0 Software Data Protection

Provisions have been made to further prevent inadvertent writes through software. In order to perform the write functions of erase or program, a two-step command sequence consisting of a setup command followed by an execute command avoids inadvertent erasing or programming of the device.

The 28SF040 will default to Software Data Protect (SDP) after power-up. The 28SF040 must be SDP disabled (Unprotect) in order to execute a write (erase or program) operation. SST strongly recommends the 28SF040 have SDP enabled after the write operation is completed. Software Data Protect is a global command and has specific sequences for enabling and disabling.

A sequence of seven consecutive reads at specified device addresses will disable SDP (unprotect the device). The address sequence is 1823H, 1820H, 1822H, 0418H, 041BH, 0419H, 041AH. The address has to be latched in the rising edge of OE# or CE#, whichever occurs first. A similar seven read sequence of 1823H, 1820H, 1822H, 0418H, 041BH, 0419H, 040AH will enable SDP (protect the device).

When the 28SF040 is in the protected state a Sector_Erase, Chip_Erase, or Byte_Program operation will not alter memory. However the 28SF040 will enter the high impedance state for a period of time equal to T_{RST} (4 µs) after the execute command is sent. At the end of the 4 µs the 28SF040 can be read.

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Application Note

SST 28SF040 Compatibly Considerations Between 4 Megabit Flash Products

July 1996

SST 28SF040
Compatibly Considerations Between 4 Megabit Flash Products

INTRODUCTION

The SST 28SF040, Atmel 29C040 and AMD 29F040 **are not** 100% Program and Erase compatible for several reasons.

1. SST and AMD devices require a separate Erase command, where as the Atmel device automatically erases prior to programming.
2. SST and AMD devices program in the byte mode whereas the Atmel device programs in the page mode.
3. SST's 28SF040 has the smallest erase block (256 byte page), followed by Atmel's 29C040 (512 byte page.) AMD's 29F040 has the largest block by far (64K byte sector.)

As you can see, none of the 5 volt 4Mbit devices can be a direct second source/replacement for one another. The one recommendation to a customer looking for a second source is to read the device ID code and have an intelligent programming routine that would use the appropriate programming algorithm for each manufacturer. The drawbacks to this are 1) the hardware Read ID requires 12 volts on A9 and 2) the software Read ID are not standardized between manufacturers.

SST's Software ID requires six bytes whereas Atmel and AMD require only three bytes. The SST device can be interrogated using AMD's/Atmel's ID procedure without any ill effects, if Software Data Protect is enabled (the 28SF040 is powered up in the Protected state). With the 28SF040 in the Protected state, the device will issue an internal Reset. Due to the Reset, the I/O's will be in a high impedance state for 4 µs (T_{RST}), afterwards it will be in the read state. If the 28SF040 is in the Unprotected state then the device will write the command codes as data.

CONVERSION FROM AMD 29F040 TO SST 28SF040

To convert from AMD 29F040 to SST 28SF040 will require some software modifications. The purpose of this paper is to outline the changes needed.

Software Data Protection

The AMD 29F040 uses three and six byte write sequences to access the device for programming and erasing. The SST 28SF040 uses a seven byte read sequence for disabling Software Data Protect then a two step sequence for erase (chip or sector) and byte program, involving specific Command Codes for each function. The Software Data Protect Disable will disable the 28SF040 until the device is either powered down or the Software Data Protect Enable sequence is used. The Command Code is a single byte write of hex data (unique data for each function) prior to each function. Please refer to the 28SF040 for Command Code details.

This Software Data Protect Entry difference is assumed in the following discussions of device functions.

Sector Erase

The AMD 29F040 sector is 64K bytes with 8 total sectors in the device. The SST 28SF040 sector is 256 bytes with 2048 total sectors. The AMD sector address is controlled by A16 - A18. The SST sector address is controlled by A8 - A18. The AMD Sector Erase time is 1.5 seconds (minimum) and SST Sector Erase time is 4 ms (maximum). The SST 28SF040 does not have a Sector Erase Suspend feature. However this feature is not needed with the SST's smaller sector size and short erase time.

Chip Erase

The AMD Sector Erase time is 1.5 seconds (minimum) and SST Chip Erase time is 10 ms (maximum).

Byte Program

The AMD Byte Program time is 16 µs (minimum) and SST Byte Program time is 35 µs (maximum).

Software ID

The SST device can be interrogated using AMD's ID procedure without any ill effects if Software Data Protect is enabled (the 28SF040 is powered up in the Protected state). The 28SF040 will not recognize the commands and may write data depending upon the state of the Software Data Protect. With the 28SF040 in the Protected state, the device will issue an internal Reset and the 28SF040 will not write data. Due to the Reset, the I/O's will be in a high impedance state up to 4 µs (T_{RST}), afterwards it will be in the read state. If the 28SF040 is in the Unprotected state then the device could write the command codes as data.

Software Drivers

SST provides a software driver (in text format) for both C and X86 assembler languages, available in a 3.5 diskette (along with software drivers for all of the SST devices). The driver is also listed verbatim in the SST Flash Memory Databook. The driver functions as both, a starting block for new software or as a reference to existing software.

CONVERSION FROM ATMEL 29C040 TO SST 28SF040

To convert from Atmel 29C040 to SST 28SF040 will require some software modifications. The purpose of this paper is to outline the changes needed.

Software Data Protection

The Atmel 29C040 uses three and six byte write sequences to access the device for programming and erasing. The SST 28SF040 uses a seven byte read sequence for disabling Software Data Protect then a two step sequence for erase (chip or sector) and byte program, involving specific Command Codes for each function. The Software Data Protect Disable will disable the 28SF040 until the device is either powered down or the Software Data Protect Enable sequence is used. The Command Code is a single byte write of hex data (unique data for each function) prior to each function. Please refer to the 28SF040 for Command Code details.

This Software Data Protect Entry difference is assumed in the following discussions of device functions.

Sector Erase

The SST 28SF040 sector is 256 bytes with 2048 total sectors. The Atmel 29C040 is a page write device and does not have a separate erase function. The SST sector address is controlled by A8 - A18. SST Sector Erase time is 4 ms (maximum).

Chip Erase

The Atmel Chip Erase time is 20 ms (maximum) and SST Chip Erase time is 10 ms (maximum).

Byte Program

SST Byte Program time is 35 µs (maximum). Atmel uses a page write of 512 bytes with a write time of 10 ms (maximum). There are 1024 pages in the Atmel 29C040 and the page is controlled by A9 - A18.

Software ID

The SST device can be interrogated using Atmel's ID procedure without any ill effects if Software Data Protect is enabled (the 28SF040 is powered up in the Protected state). The 28SF040 will not recognize the commands and may write data depending upon the state of the Software Data Protect. With the 28SF040 in the Protected state, the device will issue an internal Reset and the 28SF040 will not write data. Due to the Reset, the I/O's will be in a high impedance state up to 4 µs (T_{RST}), afterwards it will be in the read state. If the 28SF040 is in the Unprotected state then the device could write the command codes as data.

Software Drivers

SST provides a software driver (in text format) for both C and X86 assembler languages, available in a 3.5 diskette (along with software drivers for all of the SST devices). The driver is also listed verbatim in the SST Flash Memory Databook. The driver functions as both, a starting block for new software or as a reference to existing software.

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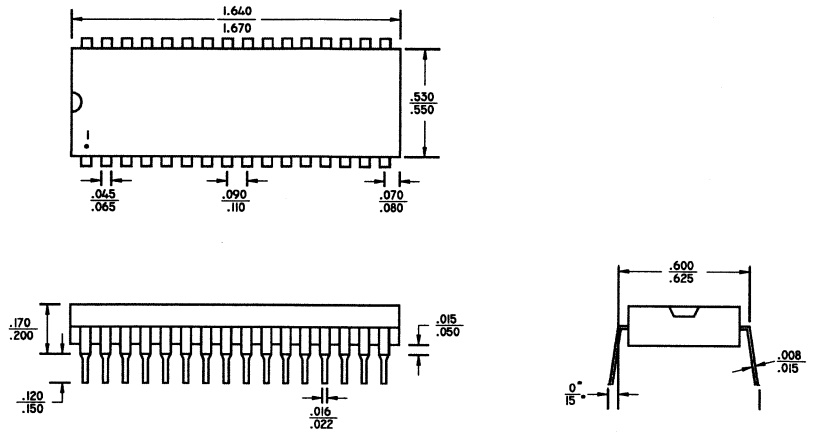
Package Mechanical Outlines

July 1996

32-Lead Plastic Dual-in-Line Package (PDIP)

SST Package Code: PH



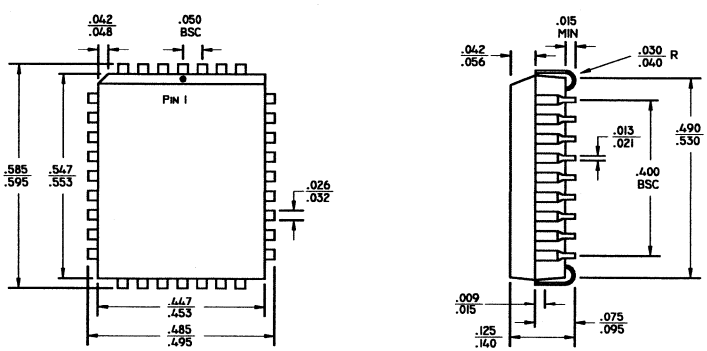
NOTE: 1. COMPLIES WITH JEDEC PUBLICATION 95 MO-015 AP DIMENSIONS, ALTHOUGH SOME DIMENSIONS MAY BE MORE STRINGENT.
2. ALL LINEAR DIMENSIONS ARE IN INCHES (MIN/MAX).
3. DIMENSIONS DO NOT INCLUDE MOLD FLASH. MAXIMUM ALLOWABLE MOLD FLASH IS .010 INCHES.

32-Lead Plastic Lead Chip Carrier (PLCC)

SST Package Code: NH

TOP VIEW

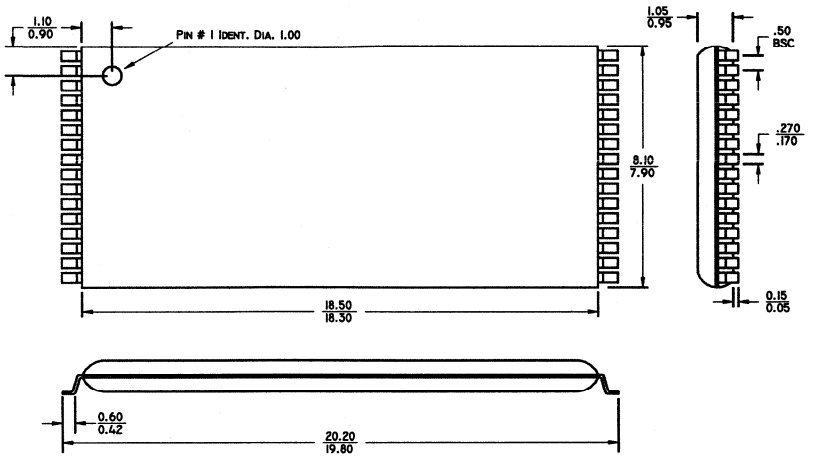
SIDE VIEW



NOTE: 1. COMPLIES WITH JEDEC PUBLICATION 95 MS-016 AE DIMENSIONS, ALTHOUGH SOME DIMENSIONS MAY BE MORE STRINGENT.
2. ALL LINEAR DIMENSIONS ARE IN INCHES (MIN/MAX).
3. DIMENSIONS DO NOT INCLUDE MOLD FLASH. MAXIMUM ALLOWABLE MOLD FLASH IS .008 INCHES.

32-Lead Thin Small Outline Package (TSOP)

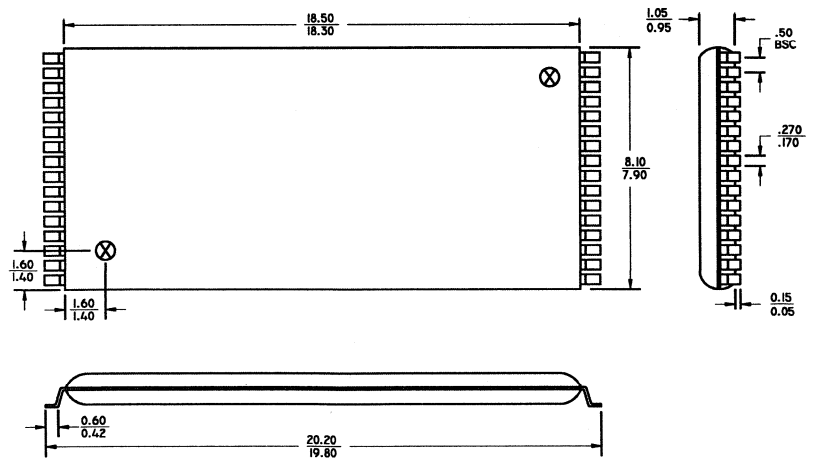
SST Package Code: EH



NOTE: 1. COMPLIES WITH JEDEC PUBLICATION 95 MO-142 CD DIMENSIONS, ALTHOUGH SOME DIMENSIONS MAY BE MORE STRINGENT.
2. ALL LINEAR DIMENSIONS ARE IN METRIC (MIN/MAX).
3. COPLANARITY: 0.1 (±.05) MM.

32-Lead Thin Small Outline Package (TSOP)

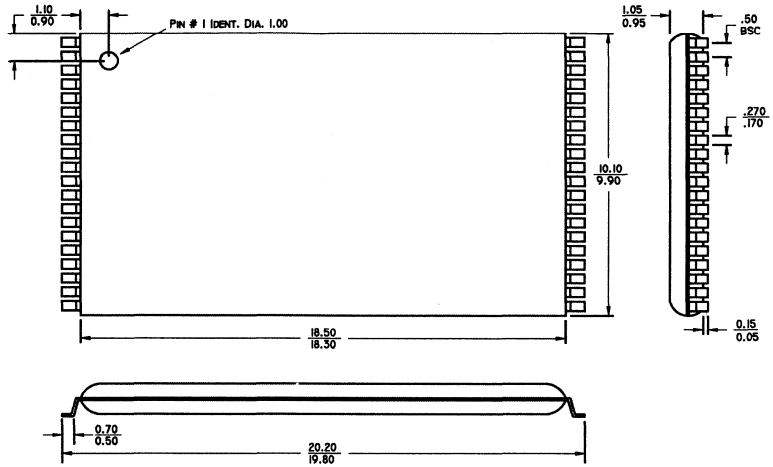
SST Package Code: FH



NOTE: 1. COMPLIES WITH JEDEC PUBLICATION 95 MO-142 CD DIMENSIONS, ALTHOUGH SOME DIMENSIONS MAY BE MORE STRINGENT.
2. ALL LINEAR DIMENSIONS ARE IN METRIC (MIN/MAX).
3. COPLANARITY: 0.1 (±.05) MM.

40-Lead Thin Small Outline Package (TSOP)

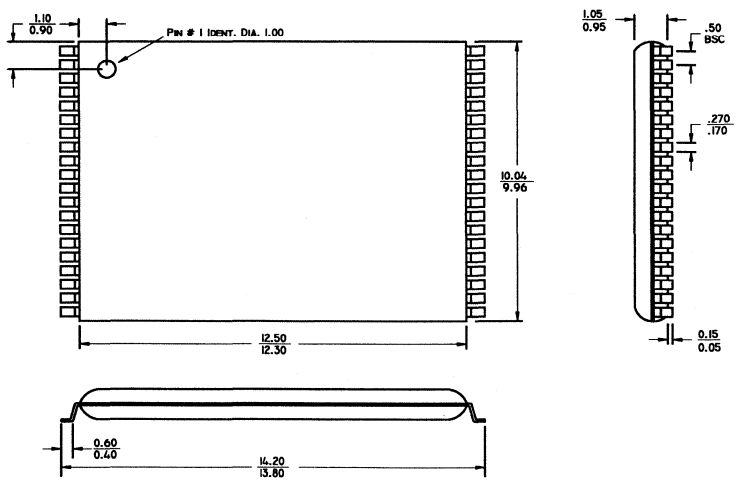
SST Package Code: EI



NOTE: 1. COMPLIES WITH JEDEC PUBLICATION 95 MO-142 BD DIMENSIONS, ALTHOUGH SOME DIMENSIONS MAY BE MORE STRINGENT.
2. ALL LINEAR DIMENSIONS ARE IN METRIC (MIN/MAX).
3. COPLANARITY: 0.1 (±.05) MM.

40-Lead Thin Small Outline Package (TSOP)

SST Package Code: WI



NOTE: 1. COMPLIES WITH JEDEC PUBLICATION 95 MO-142 CA DIMENSIONS, ALTHOUGH SOME DIMENSIONS MAY BE MORE STRINGENT.
2. ALL LINEAR DIMENSIONS ARE IN METRIC (MIN/MAX).
3. COPLANARITY: 0.1 (±.05) MM.

Old Part Number to New Part Number Cross-Reference Guide

Effective, August 5 1996, SST converted to a new part numbering system. The Part Numbering Guide presented on page 1.1 explains the meaning of each field in the new part numbering scheme. The following cross reference guide is provided to assist in converting from SST's previous part numbering system to the new scheme. There has been no change in fit or function of any SST product as a result of this change in part numbering.

Please note: In keeping with current industry standards, SST has also changed the description of it's low voltage products from nominal V_{CC} to lowest V_{CC}. Products previously designated as 3.3V are now designated as 3.0V products and products previously designated as 3.0V products are now designated as 2.7V products. There has been no electrical or mechanical impact on the products, this is merely a change in product description.

Old Part Number	New Part Number
29EE512 Family	
EH29EE512-90-3CF	SST29EE512-90-3C-EH
EH29EE512-90-3IF	SST29EE512-90-3I-EH
EH29EE512-90-4CF	SST29EE512-90-4C-EH
EH29EE512-90-4IF	SST29EE512-90-4I-EH
EH29EE512-120-3CF	SST29EE512-120-3C-EH
EH29EE512-120-3IF	SST29EE512-120-3I-EH
EH29EE512-120-4CF	SST29EE512-120-4C-EH
EH29EE512-120-4IF	SST29EE512-120-4I-EH
NH29EE512-90-3CF	SST29EE512-90-3C-NH
NH29EE512-90-3IF	SST29EE512-90-3I-NH
NH29EE512-90-4CF	SST29EE512-90-4C-NH
NH29EE512-90-4IF	SST29EE512-90-4I-NH
NH29EE512-120-3CF	SST29EE512-120-3C-NH
NH29EE512-120-3IF	SST29EE512-120-3I-NH
NH29EE512-120-4CF	SST29EE512-120-4C-NH
NH29EE512-120-4IF	SST29EE512-120-4I-NH
PH29EE512-90-3CF	SST29EE512-90-3C-PH
PH29EE512-90-4CF	SST29EE512-90-4C-PH
PH29EE512-120-3CF	SST29EE512-120-3C-PH
PH29EE512-120-4CF	SST29EE512-120-4C-PH
U29EE512-120-3CF	SST29EE512-120-3C-U*
U29EE512-120-4CF	SST29EE512-120-4C-U*
29LE512 Family	
EH29LE512-150-3CT	SST29LE512-150-3C-EH
EH29LE512-150-3IT	SST29LE512-150-3I-EH
EH29LE512-150-4CT	SST29LE512-150-4C-EH
EH29LE512-150-4IT	SST29LE512-150-4I-EH
EH29LE512-200-3CT	SST29LE512-200-3C-EH
EH29LE512-200-3IT	SST29LE512-200-3I-EH
EH29LE512-200-4CT	SST29LE512-200-4C-EH
EH29LE512-200-4IT	SST29LE512-200-4I-EH
NH29LE512-150-3CT	SST29LE512-150-3C-NH
NH29LE512-150-3IT	SST29LE512-150-3I-NH
NH29LE512-150-4CT	SST29LE512-150-4C-NH
NH29LE512-150-4IT	SST29LE512-150-4I-NH
NH29LE512-200-3CT	SST29LE512-200-3C-NH
NH29LE512-200-3IT	SST29LE512-200-3I-NH
NH29LE512-200-4CT	SST29LE512-200-4C-NH
NH29LE512-200-4IT	SST29LE512-200-4I-NH
PH29LE512-150-3CT	SST29LE512-150-3C-PH
PH29LE512-150-4CT	SST29LE512-150-4C-PH
PH29LE512-200-3CT	SST29LE512-200-3C-PH
PH29LE512-200-4CT	SST29LE512-200-4C-PH
U29LE512-200-3CT	SST29LE512-200-3C-U*
U29LE512-200-4CT	SST29LE512-200-4C-U*
29VE512 Family	
EH29VE512-200-3CV	SST29VE512-200-3C-EH
EH29VE512-200-3IV	SST29VE512-200-3I-EH
EH29VE512-200-4CV	SST29VE512-200-4C-EH
EH29VE512-200-4IV	SST29VE512-200-4I-EH
EH29VE512-250-3CV	SST29VE512-250-3C-EH
EH29VE512-250-3IV	SST29VE512-250-3I-EH
EH29VE512-250-4CV	SST29VE512-250-4C-EH
EH29VE512-250-4IV	SST29VE512-250-4I-EH
NH29VE512-200-3CV	SST29VE512-200-3C-NH

Old Part Number to New Part Number Cross-Reference Guide

Old Part Number	New Part Number
NH29VE512-200-3IV	SST29VE512-200-3I-NH
NH29VE512-200-4CV	SST29VE512-200-4C-NH
NH29VE512-200-4IV	SST29VE512-200-4I-NH
NH29VE512-250-3CV	SST29VE512-250-3C-NH
NH29VE512-250-3IV	SST29VE512-250-3I-NH
NH29VE512-250-4CV	SST29VE512-250-4C-NH
NH29VE512-250-4IV	SST29VE512-250-4I-NH
PH29VE512-200-3CV	SST29VE512-200-3C-PH
PH29VE512-200-4CV	SST29VE512-200-4C-PH
PH29VE512-250-3CV	SST29VE512-250-3C-PH
PH29VE512-250-4CV	SST29VE512-250-4C-PH
U29VE512-250-3CV	SST29VE512-250-3C-U*
U29VE512-250-4CV	SST29VE512-250-4C-U*

29EE010 Family

EH29EE010-90-3CF	SST29EE010-90-3C-EH
EH29EE010-90-3IF	SST29EE010-90-3I-EH
EH29EE010-90-4CF	SST29EE010-90-4C-EH
EH29EE010-90-4IF	SST29EE010-90-4I-EH
EH29EE010-120-3CF	SST29EE010-120-3C-EH
EH29EE010-120-3IF	SST29EE010-120-3I-EH
EH29EE010-120-4CF	SST29EE010-120-4C-EH
EH29EE010-120-4IF	SST29EE010-120-4I-EH
EH29EE010-150-3CF	SST29EE010-150-3C-EH
EH29EE010-150-3IF	SST29EE010-150-3I-EH
EH29EE010-150-4CF	SST29EE010-150-4C-EH
EH29EE010-150-4IF	SST29EE010-150-4I-EH
NH29EE010-90-3CF	SST29EE010-90-3C-NH
NH29EE010-90-3IF	SST29EE010-90-3I-NH
NH29EE010-90-4CF	SST29EE010-90-4C-NH
NH29EE010-90-4IF	SST29EE010-90-4I-NH
NH29EE010-120-3CF	SST29EE010-120-3C-NH
NH29EE010-120-3IF	SST29EE010-120-3I-NH
NH29EE010-120-4CF	SST29EE010-120-4C-NH
NH29EE010-120-4IF	SST29EE010-120-4I-NH
NH29EE010-150-3CF	SST29EE010-150-3C-NH
NH29EE010-150-3IF	SST29EE010-150-3I-NH
NH29EE010-150-4CF	SST29EE010-150-4C-NH
NH29EE010-150-4IF	SST29EE010-150-4I-NH
PH29EE010-90-3CF	SST29EE010-90-3C-PH
PH29EE010-90-4CF	SST29EE010-90-4C-PH
PH29EE010-120-3CF	SST29EE010-120-3C-PH
PH29EE010-120-4CF	SST29EE010-120-4C-PH
PH29EE010-150-3CF	SST29EE010-150-3C-PH
PH29EE010-150-4CF	SST29EE010-150-4C-PH
U29EE010-150-3CF	SST29EE010-150-3C-U*
U29EE010-150-4CF	SST29EE010-150-4C-U*

29LE010 Family

EH29LE010-150-3CT	SST29LE010-150-3C-EH
EH29LE010-150-3IT	SST29LE010-150-3I-EH
EH29LE010-150-4CT	SST29LE010-150-4C-EH
EH29LE010-150-4IT	SST29LE010-150-4I-EH
EH29LE010-200-3CT	SST29LE010-200-3C-EH
EH29LE010-200-3IT	SST29LE010-200-3I-EH
EH29LE010-200-4CT	SST29LE010-200-4C-EH
EH29LE010-200-4IT	SST29LE010-200-4I-EH
NH29LE010-150-3CT	SST29LE010-150-3C-NH
NH29LE010-150-3IT	SST29LE010-150-3I-NH
NH29LE010-150-4CT	SST29LE010-150-4C-NH
NH29LE010-150-4IT	SST29LE010-150-4I-NH
NH29LE010-200-3CT	SST29LE010-200-3C-NH
NH29LE010-200-3IT	SST29LE010-200-3I-NH
NH29LE010-200-4CT	SST29LE010-200-4C-NH
NH29LE010-200-4IT	SST29LE010-200-4I-NH
PH29LE010-150-3CT	SST29LE010-150-3C-PH
PH29LE010-150-4CT	SST29LE010-150-4C-PH
PH29LE010-200-3CT	SST29LE010-200-3C-PH
PH29LE010-200-4CT	SST29LE010-200-4C-PH
U29LE010-200-3CT	SST29LE010-200-3C-U*
U29LE010-200-4CT	SST29LE010-200-4C-U*

29VE010 Family

EH29VE010-200-3CV	SST29VE010-200-3C-EH
EH29VE010-200-3IV	SST29VE010-200-3I-EH
EH29VE010-200-4CV	SST29VE010-200-4C-EH

Old Part Number to New Part Number Cross-Reference Guide

Old Part Number	New Part Number
EH29VE010-200-4IV	SST29VE010-200-4I-EH
EH29VE010-250-3CV	SST29VE010-250-3C-EH
EH29VE010-250-3IV	SST29VE010-250-3I-EH
EH29VE010-250-4CV	SST29VE010-250-4C-EH
EH29VE010-250-4IV	SST29VE010-250-4I-EH
NH29VE010-200-3CV	SST29VE010-200-3C-NH
NH29VE010-200-3IV	SST29VE010-200-3I-NH
NH29VE010-200-4CV	SST29VE010-200-4C-NH
NH29VE010-200-4IV	SST29VE010-200-4I-NH
NH29VE010-250-3CV	SST29VE010-250-3C-NH
NH29VE010-250-3IV	SST29VE010-250-3I-NH
NH29VE010-250-4CV	SST29VE010-250-4C-NH
NH29VE010-250-4IV	SST29VE010-250-4I-NH
PH29VE010-200-3CV	SST29VE010-200-3C-PH
PH29VE010-200-4CV	SST29VE010-200-4C-PH
PH29VE010-250-3CV	SST29VE010-250-3C-PH
PH29VE010-250-4CV	SST29VE010-250-4C-PH
U29VE010-250-3CV	SST29VE010-250-3C-U*
U29VE010-250-4CV	SST29VE010-250-4C-U*

29EE020 Family	
EH29EE020-120-3CF	SST29EE020-120-3C-EH
EH29EE020-120-3IF	SST29EE020-120-3I-EH
EH29EE020-120-4CF	SST29EE020-120-4C-EH
EH29EE020-120-4IF	SST29EE020-120-4I-EH
EH29EE020-150-3CF	SST29EE020-150-3C-EH
EH29EE020-150-3IF	SST29EE020-150-3I-EH
EH29EE020-150-4CF	SST29EE020-150-4C-EH
EH29EE020-150-4IF	SST29EE020-150-4I-EH
NH29EE020-120-3CF	SST29EE020-120-3C-NH
NH29EE020-120-3IF	SST29EE020-120-3I-NH
NH29EE020-120-4CF	SST29EE020-120-4C-NH
NH29EE020-120-4IF	SST29EE020-120-4I-NH
NH29EE020-150-3CF	SST29EE020-150-3C-NH
NH29EE020-150-3IF	SST29EE020-150-3I-NH
NH29EE020-150-4CF	SST29EE020-150-4C-NH
NH29EE020-150-4IF	SST29EE020-150-4I-NH
PH29EE020-120-3CF	SST29EE020-120-3C-PH
PH29EE020-120-4CF	SST29EE020-120-4C-PH
PH29EE020-150-3CF	SST29EE020-150-3C-PH
PH29EE020-150-4CF	SST29EE020-150-4C-PH
U29EE020-150-3CF	SST29EE020-150-3C-U*
U29EE020-150-4CF	SST29EE020-150-4C-U*

29LE020 Family	
EH29LE020-200-4CT	SST29LE020-200-4C-EH
EH29LE020-200-4IT	SST29LE020-200-4I-EH
EH29LE020-250-4CT	SST29LE020-250-4C-EH
EH29LE020-250-4IT	SST29LE020-250-4I-EH
NH29LE020-200-4CT	SST29LE020-200-4C-NH
NH29LE020-200-4IT	SST29LE020-200-4I-NH
NH29LE020-250-4CT	SST29LE020-250-4C-NH
NH29LE020-250-4IT	SST29LE020-250-4I-NH
PH29LE020-200-4CT	SST29LE020-200-4C-PH
PH29LE020-250-4CT	SST29LE020-250-4C-PH
U29LE020-250-4CT	SST29LE020-250-4C-U*

29VE020 Family	
EH29VE020-250-4CV	SST29VE020-250-4C-EH
EH29VE020-250-4IV	SST29VE020-250-4I-EH
EH29VE020-300-4CV	SST29VE020-300-4C-EH
EH29VE020-300-4IV	SST29VE020-300-4I-EH
NH29VE020-250-4CV	SST29VE020-250-4C-NH
NH29VE020-250-4IV	SST29VE020-250-4I-NH
NH29VE020-300-4CV	SST29VE020-300-4C-NH
NH29VE020-300-4IV	SST29VE020-300-4I-NH
PH29VE020-250-4CV	SST29VE020-250-4C-PH
PH29VE020-300-4CV	SST29VE020-300-4C-PH
U29VE020-300-4CV	SST29VE020-300-4C-U*

28SF040 Family	
EH28SF040-150-3CF	SST28SF040-150-3C-EH
EH28SF040-150-3IF	SST28SF040-150-3I-EH
EH28SF040-150-4CF	SST28SF040-150-4C-EH
EH28SF040-150-4IF	SST28SF040-150-4I-EH
EH28SF040-200-3CF	SST28SF040-200-3C-EH

Old Part Number to New Part Number Cross-Reference Guide

Old Part Number	New Part Number
EH28SF040-200-3IF	SST28SF040-200-3I-EH
EH28SF040-200-4CF	SST28SF040-200-4C-EH
EH28SF040-200-4IF	SST28SF040-200-4I-EH
EI28SF040-150-3CF	SST28SF040-150-3C-EI
EI28SF040-150-3IF	SST28SF040-150-3I-EI
EI28SF040-150-4CF	SST28SF040-150-4C-EI
EI28SF040-150-4IF	SST28SF040-150-4I-EI
EI28SF040-200-3CF	SST28SF040-200-3C-EI
EI28SF040-200-3IF	SST28SF040-200-3I-EI
EI28SF040-200-4CF	SST28SF040-200-4C-EI
EI28SF040-200-4IF	SST28SF040-200-4I-EI
NH28SF040-150-3CF	SST28SF040-150-3C-NH
NH28SF040-150-3IF	SST28SF040-150-3I-NH
NH28SF040-150-4CF	SST28SF040-150-4C-NH
NH28SF040-150-4IF	SST28SF040-150-4I-NH
NH28SF040-200-3CF	SST28SF040-200-3C-NH
NH28SF040-200-3IF	SST28SF040-200-3I-NH
NH28SF040-200-4CF	SST28SF040-200-4C-NH
NH28SF040-200-4IF	SST28SF040-200-4I-NH
PH28SF040-150-3CF	SST28SF040-150-3C-PH
PH28SF040-150-3IF	SST28SF040-150-3I-PH
PH28SF040-150-4CF	SST28SF040-150-4C-PH
PH28SF040-150-4IF	SST28SF040-150-4I-PH
PH28SF040-200-3CF	SST28SF040-200-3C-PH
PH28SF040-200-3IF	SST28SF040-200-3I-PH
PH28SF040-200-4CF	SST28SF040-200-4C-PH
PH28SF040-200-4IF	SST28SF040-200-4i-PH
U28SF040-200-3CF	SST28SF040-200-3C-U*
U28SF040-200-4CF	SST28SF040-200-4C-U*

28LF040 Family

EH28LS040-200-3CT	SST28LF040-200-3C-EH
EH28LS040-200-3IT	SST28LF040-200-3I-EH
EH28LS040-200-4CT	SST28LF040-200-4C-EH
EH28LS040-200-4IT	SST28LF040-200-4I-EH
EH28LS040-250-3CT	SST28LF040-250-3C-EH
EH28LS040-250-3IT	SST28LF040-250-3I-EH
EH28LS040-250-4CT	SST28LF040-250-4C-EH
EH28LS040-250-4IT	SST28LF040-250-4I-EH
EI28LS040-200-3CT	SST28LF040-200-3C-EI
EI28LS040-200-3IT	SST28LF040-200-3I-EI
EI28LS040-200-4CT	SST28LF040-200-4C-EI
EI28LS040-200-4IT	SST28LF040-200-4I-EI
EI28LS040-250-3CT	SST28LF040-250-3C-EI
EI28LS040-250-3IT	SST28LF040-250-3I-EI
EI28LS040-250-4CT	SST28LF040-250-4C-EI
EI28LS040-250-4IT	SST28LF040-250-4I-EI
NH28LS040-200-3CT	SST28LF040-200-3C-NH
NH28LS040-200-3IT	SST28LF040-200-3I-NH
NH28LS040-200-4CT	SST28LF040-200-4C-NH
NH28LS040-200-4IT	SST28LF040-200-4I-NH
NH28LS040-250-3CT	SST28LF040-250-3C-NH
NH28LS040-250-3IT	SST28LF040-250-3I-NH
NH28LS040-250-4CT	SST28LF040-250-4C-NH
NH28LS040-250-4IT	SST28LF040-250-4I-NH
PH28LS040-200-3CT	SST28LF040-200-3C-PH
PH28LS040-200-3IT	SST28LF040-200-3I-PH
PH28LS040-200-4CT	SST28LF040-200-4C-PH
PH28LS040-200-4IT	SST28LF040-200-4I-PH
PH28LS040-250-3CT	SST28LF040-250-3C-PH
PH28LS040-250-3IT	SST28LF040-250-3I-PH
PH28LS040-250-4CT	SST28LF040-250-4C-PH
PH28LS040-250-4IT	SST28LF040-250-4I-PH
U28LS040-250-3CT	SST28LF040-250-3C-U*
U28LS040-250-4CT	SST28LF040-250-4C-U*

28VF040 Family

EH28VS040-250-3CV	SST28VF040-250-3C-EH
EH28VS040-250-3IV	SST28VF040-250-3I-EH
EH28VS040-250-4CV	SST28VF040-250-4C-EH
EH28VS040-250-4IV	SST28VF040-250-4I-EH
EH28VS040-300-3CV	SST28VF040-300-3C-EH
EH28VS040-300-3IV	SST28VF040-300-3I-EH
EH28VS040-300-4CV	SST28VF040-300-4C-EH
EH28VS040-300-4IV	SST28VF040-300-4I-EH
EI28VS040-250-3CV	SST28VF040-250-3C-EI

Old Part Number to New Part Number Cross-Reference Guide

Old Part Number	New Part Number	Old Part Number	New Part Number
EI28VS040-250-3IV	SST28VF040-250-3I-EI	NH28VS040-300-4CV	SST28VF040-300-4C-NH
EI28VS040-250-4CV	SST28VF040-250-4C-EI	NH28VS040-300-4IV	SST28VF040-300-4I-NH
EI28VS040-250-4IV	SST28VF040-250-4I-EI	PH28VS040-250-3CV	SST28VF040-250-3C-PH
EI28VS040-300-3CV	SST28VF040-300-3C-EI	PH28VS040-250-3IV	SST28VF040-250-3I-PH
EI28VS040-300-3IV	SST28VF040-300-3I-EI	PH28VS040-250-4CV	SST28VF040-250-4C-PH
EI28VS040-300-4CV	SST28VF040-300-4C-EI	PH28VS040-250-4IV	SST28VF040-250-4I-PH
EI28VS040-300-4IV	SST28VF040-300-4I-EI	PH28VS040-300-3CV	SST28VF040-300-3C-PH
NH28VS040-250-3CV	SST28VF040-250-3C-NH	PH28VS040-300-3IV	SST28VF040-300-3I-PH
NH28VS040-250-3IV	SST28VF040-250-3I-NH	PH28VS040-300-4CV	SST28VF040-300-4C-PH
NH28VS040-250-4CV	SST28VF040-250-4C-NH	PH28VS040-300-4IV	SST28VF040-300-4i-PH
NH28VS040-250-4IV	SST28VF040-250-4I-NH	U28VS040-300-3CV	SST28VF040-300-3C-U*
NH28VS040-300-3CV	SST28VF040-300-3C-NH	U28VS040-300-4CV	SST28VF040-300-4C-U*
NH28VS040-300-3IV	SST28VF040-300-3I-NH		

Old Part Number	New Part Number
28PC040 Family	
WI28PC040-150-5CF-S00A	SST28PC040-150-5C-WI-S00A
WI28PC040-250-5CF-S00A	SST28PC040-250-5C-WI-S00A
WI28PC040-150-5CF-S01B	SST28PC040-150-5C-WI-S01B
WI28PC040-250-5CF-S01B	SST28PC040-250-5C-WI-S01B
WI28PC040-150-5CF-S10C	SST28PC040-150-5C-WI-S10C
WI28PC040-250-5CF-S10C	SST28PC040-250-5C-WI-S10C
WI28PC040-150-5CF-S11D	SST28PC040-150-5C-WI-S11D
WI28PC040-250-5CF-S11D	SST28PC040-250-5C-WI-S11D
28LP040 Family	
WI28LP040-250-5CT-S00A	SST28LP040-250-5C-WI-S00A
WI28LP040-250-5CT-S01B	SST28LP040-250-5C-WI-S01B
WI28LP040-250-5CT-S10C	SST28LP040-250-5C-WI-S10C
WI28LP040-250-5CF-S11D	SST28LP040-250-5C-WI-S11D

* Numeric modifier (1 - 9) follows "U" to describe current die revision for unencapsulated die sales.

Old Part Number to New Part Number Cross-Reference Guide

Due to improvements in operating performance, SST is no longer offering certain speed grades for some products. The following list highlights those products which are now obsolete and identifies the closest available SST replacement product.

Obsolete Product	Replacement Product
29EE512 Family	
EH29EE512-150-3CF	SST29EE512-120-3C-EH
EH29EE512-150-3IF	SST29EE512-120-3I-EH
EH29EE512-150-4CF	SST29EE512-120-4C-EH
EH29EE512-150-4IF	SST29EE512-120-4I-EH
NH29EE512-150-3CF	SST29EE512-120-3C-NH
NH29EE512-150-3IF	SST29EE512-120-3I-NH
NH29EE512-150-4CF	SST29EE512-120-4C-NH
NH29EE512-150-4IF	SST29EE512-120-4I-NH
PH29EE512-150-3CF	SST29EE512-120-3C-PH
PH29EE512-150-4CF	SST29EE512-120-4C-PH
U29EE512-150-3CF	SST29EE512-120-3C-U*
U29EE512-150-4CF	SST29EE512-120-4C-U*
29LE512 Family	
EH29LE512-250-3CF	SST29LE512-200-3C-EH
EH29LE512-250-3IF	SST29LE512-200-3I-EH
EH29LE512-250-4CF	SST29LE512-200-4C-EH
EH29LE512-250-4IF	SST29LE512-200-4I-EH
NH29LE512-250-3CF	SST29LE512-200-3C-NH
NH29LE512-250-3IF	SST29LE512-200-3I-NH
NH29LE512-250-4CF	SST29LE512-200-4C-NH
NH29LE512-250-4IF	SST29LE512-200-4I-NH
PH29LE512-250-3CF	SST29LE512-200-3C-PH
PH29LE512-250-4CF	SST29LE512-200-4C-PH
U29LE512-250-3CF	SST29LE512-200-3C-U*
U29LE512-250-4CF	SST29LE512-200-4C-U*

Obsolete Product	Replacement Product
29LE010 Family	
EH29LE010-250-3CF	SST29LE010-200-3C-EH
EH29LE010-250-3IF	SST29LE010-200-3I-EH
EH29LE010-250-4CF	SST29LE010-200-4C-EH
EH29LE010-250-4IF	SST29LE010-200-4I-EH
NH29LE010-250-3CF	SST29LE010-200-3C-NH
NH29LE010-250-3IF	SST29LE010-200-3I-NH
NH29LE010-250-4CF	SST29LE010-200-4C-NH
NH29LE010-250-4IF	SST29LE010-200-4I-NH
PH29LE010-250-3CF	SST29LE010-200-3C-PH
PH29LE010-250-4CF	SST29LE010-200-4C-PH
U29LE010-250-3CF	SST29LE010-200-3C-U*
U29LE010-250-4CF	SST29LE010-200-4C-U*
28LF040 Family	
EH28LS040-300-3CF	SST28LF040-250-3C-EH
EH28LS040-300-3IF	SST28LF040-250-3I-EH
EH28LS040-300-4CF	SST28LF040-250-4C-EH
EH28LS040-300-4IF	SST28LF040-250-4I-EH
NH28LS040-300-3CF	SST28LF040-250-3C-NH
NH28LS040-300-3IF	SST28LF040-250-3I-NH
NH28LS040-300-4CF	SST28LF040-250-4C-NH
NH28LS040-300-4IF	SST28LF040-250-4I-NH
PH28LS040-300-3CF	SST28LF040-250-3C-PH
PH28LS040-300-4CF	SST28LF040-250-4C-PH
U28LS040-300-3CF	SST28LF040-250-3C-U*
U28LS040-300-4CF	SST28LF040-250-4C-U*

* Numeric modifier (1 - 9) follows "U" to describe current die revision for unencapsulated die sales.

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Clifton, NJ 07013
Tel: (201) 777-4100
Fax: (201) 777-6194

Nu Horizons Electronics Corp.
39 U.S. Route 46
Pine Brook, NJ 07058
Tel: (201) 882-8300
Fax: (201) 882-8398

NEW YORK

Bell Microproducts
1056 West Jericho Turnpike
Smithtown, NY 11787
Tel: (516) 543-2000
Fax: (516) 543-2030

Jaco Electronics, Inc.
145 Oser Ave.
Hauppauge, NY 11788
Tel: (516) 273-5500
Fax: (516) 273-5799

Nu Horizons Electronics Corp.
6000 New Horizons Blvd.
Amityville, NY 11701
Tel: (516) 226-6000
Fax: (516) 226-6140

Nu Horizons Electronics Corp.
333 Metro Park
Rochester, NY 14623
Tel: (716) 292-0777
Fax: (716) 292-0750

Reptron Corp.
95 Osor Avenue
Hauppauge, NY 11788
Tel: (516) 952-3196
Fax: (516) 952-3896

NORTH CAROLINA

Jaco Electronics, Inc.
5206 Greens Dairy Road
Raleigh, NC 27604
Tel: (919) 876-7767
Fax: (919) 876-6964

Nu Horizons Electronics Corp.
2920 Highwood Blvd.
Suite 125
Raleigh, NC 27604
Tel: (919) 954-0500
Fax: (919) 954-0545

Reptron Corp.
5954-A Six Forks Road
Raleigh, NC 27609-3895
Tel: (919) 870-5189
Fax: (919) 870-5210

OHIO

Nu Horizons Electronics Corp.
2208 Enterprise E. Prkwy.
Twinsburg, OH 44087
Tel: (216) 963-9933
Fax: (216) 963-9944

Reptron Corp.
4672 S. Boulevard NW, Suite #8
Canton, OH 44718
Tel: (330) 649-9115
Fax: (330) 649-9116

Reptron Corp.
31225 Bainbridge Road, Suite N
Solon, OH 44139-2230
Tel: (216) 349-1415
Fax: (216) 349-1634

North American Distributors

OREGON

Jaco Electronics, Inc.
4900 SW Griffith Drive, Suite 129
Beaverton, OR 97005
Tel: (503) 626-1439
Fax: (503) 626-0979

Reptron Corp.
1800 N.W. 169th Place,
Suite 300 B
Beaverton, OR 97006-7304
Tel: (503) 629-2082
Fax: (503) 629-8645

PENNSYLVANIA

Nu Horizons Electronics Corp.
18000 Horizon Wy., Suite 200
Mt.Laurel, NJ 08054
Tel: (609) 231-0900
(215) 537-6450 (PA)
Fax: (609) 231-9510

Reptron Corp.
179 Witmer Road
Horsham, PA 19044-2210
Tel: (215) 672-6055
Fax: (215) 672-4966

TEXAS

Axis Components, Inc.
9600 Great Hills Trail #150
Austin, TX 78759
Tel: (512) 502-3019
Fax: (512) 502-1956

Axis Components, Inc.
Dallas, TX
Tel: (800) 556-0225

Bell Microproducts
12701 B Research Blvd., Suite 301
Austin, TX 78759
Tel: (512) 258-0725
Fax: (512) 258-6517

Bell Microproducts, Inc.
1202 Executive Drive West
Richardson, TX 75081
Tel: (972) 783-4191
Fax: (972) 783-4192

Jaco Electronics, Inc.
2120-A Braker Lane
Austin, TX 78758
Tel: (512) 835-0220
Fax: (512) 339-9252

Jaco Electronics, Inc.
1209 N. Glenville Drive
Richardson, TX 75081
Tel: (972) 234-5565
Fax: (972) 238-7068

Nu Horizons Electronics Corp.
7801 North Lamar, Suite F-29
Austin, TX 78752
Tel: (512) 467-2292
Fax: (512) 467-2466

Nu Horizons Electronics Corp.
2081 Hutton Dr., Suite 119
Carrollton, TX 75006
Tel: (214) 488-2255
Fax: (214) 488-2265

VIRGINIA

Bell Microproducts
1039 Sterling Road, Suite 204
Herndon, VA 22021
Tel: (703) 834-3696
Fax: (703) 834-3698

WISCONSIN

Marsh Electronics
N1046 Towerview Drive
Greenville, WI 54942
Tel: (414) 757-0800
Fax: (414) 757-0804

Marsh Electronics,
1563 South 101st Street
Milwaukee, WI 53214
Tel: (414) 475-6000
Fax: (414) 771-2847

WASHINGTON

Bell Microproducts, Inc.
18210 Redmond Way, Suite 302
Redmond, WA 98052
Tel: (206) 861-5710
Fax: (206) 885-5399

Reptron Corp.
8312 154th Avenue NE
Redmond, WA 98052
Tel: (206) 702-9166
Fax: (206) 869-2663

International
Sales Representatives & Distributors

CHINA (86)

Actron Technology Co., Ltd.
4/F, Block 138, Langton District
Shenzhen, P. R. China
Tel: 755-573-2602
Fax: 755-573-2603

Actron Technology Co., Ltd.
Rm. 703, Hauzhing Tech. Centre
4, Zhong Cun Nan Lu
Haiden Road
Beijing, China
Tel: 010-6261-0042
Fax: 010-6262-6238

HONG KONG (852)

Actron Technology Co., Ltd.
Room A, 26/F, Lever Centre
69-71 King Yip Street
Kwun Tong, Kowloon,
Hong Kong
Tel: 2727-3978
Fax: 2727-4330

KOREA (82)

D & S Co., Ltd.
Rm. 807, Sungji Height 3 B/D
642-6, Yoksam-Dong, Kangnam-Gu
Seoul 135-080, Korea
Tel: 02 538-8431
Fax: 02 568-2008

JAPAN (81)

Hakuto Co., Ltd.
1-1-13 Shinjuku, Shinjuku-ku
Tokyo 160, Japan
Tel: (03) 3355-7617
Fax: (03) 3355-7680

Inno Micro Corporation
2-13-13 Shinyokohama
Kohoku-ku, Yokohama
Kanagawa 222, Japan
Tel: (045) 476-7508
Fax: (045) 476-7518

Silicon Storage Technology Co., Ltd.
2-2-16 YK Bld., Sangenjaya
Setagaya-Ku, Tokyo 154, Japan
Tel: (03) 3795-6461
Fax: (03) 3795-2425

SINGAPORE (65)

Serial System Pte. Ltd.
11 Jalan Mesin #06-00
Standard Industrial Building
Singapore 368813
Tel: 280-0200
Fax: 280-7923

TAIWAN (886)

GSS Award
Rm. 6, 9/F, No. 17, Sec. 1
Cheng Te Road
Taipei, Taiwan, R.O.C.
Tel: (02) 555-0880
Fax: (02) 555-4420

PCT Limited
6F-2, No. 15, Lane 174
Hsin Ming Road, Nei Hu
Taipei, Taiwan, R.O.C.
Tel: (02) 796-3738
Fax: (02) 794-6311

SST EAST ASIA MARKETING OFFICE (81)

Nisso #14 Bldg., 4/F
2-7-1, Shinyokohama, Kohoku-ku,
Yokohama 222, Japan
Tel: (045) 471-1851
Fax: (045) 471-3285

Please Note: All telephone and fax numbers include the proper city codes required to dial the number from within the specified country. If dialing from outside the specific country, please add the country code provided in parenthesis next to the country name.

International
Sales Representatives & Distributors

AUSTRALIA (61)
ACD
Unit 2, 17-19 Melrich Road
Baywater 3153
Australia
Tel: (03) 762 7644
Fax: (03) 762 5446

GEC Electronics Division
Locked Bag 29
PO Rydalmere NSW 2116
Unit 1, 38-46 South Street
Rydalmere NSW 2116
Australia
Tel: (02) 638 1888
Fax: (02) 638 1798

KC Electronics
Suite 3, 888 Doncaster Road
Doncaster, Victoria 3109
Australia
Tel: (03) 9848 1266
Fax: (03) 9848 1799

FINLAND (358)
OXXO OY AB
Malminkaari 10 B
FIN-00700 Helsinki
Finland
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Fax: (9*) 5842 6200

**Effective October 12, 1996, current area code is "0".*

FRANCE (33)
Tekelec Airtronic
5, Rue Carle Vernet
92315 Sevres Cedex
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Tel: 1 46.23.24.25
Fax: 1 45.07.21.91

GERMANY (49)
MSC Vertriebs GmbH
Industriestraße 16
76297 Stutensee
Germany
Tel: 0 72 49 / 910-0
Fax: 0 72 49 / 79 93

IRELAND (353)
Memec Ireland LTD
Block H, Lock Quay,
Clare Street, Limerick
EIRE
Tel: 061 411842
Fax: 061 411888

ISREAL (972)
Elina Electronics
14, Raoul Wallenberg St.
P. O. Box 13190
Tel-Aviv 51131
Israel
Tel: 3-649 8543
Fax: 3-649 8745

ITALY (39)
Tekelec Airtronic S.p.a.
Via G. Mameli 31
20129 Milano
Italy
Tel: 2 76 110.168
Fax: 2 73 854.62

NEW ZEALAND (64)
KC Electronics
1st Floor, "Southpark"
Cnr Lunns & Curletts Rds
ChristChurch
New Zealand
Tel: (03) 343 5160
Fax: (03) 343 5170

SPAIN (34)
Tekelec Espana S.A.
General Aranaz, 49
28027 Madrid
Spain
Tel: 13 20 41 60
Fax: 13 20 10 18

SWEDEN (46)
Pelcon Electronics AB
Girovägen 13
S-175 06 Järafälla
Sweden
Tel: 08.795 98 70
Fax: 08.760 76 85

UNITED KINGDOM (44)
Ambar Components, Ltd.
17 Thame Park Road
Thame, Oxfordshire OX9 3XD
England
Tel: 01844 261144
Fax: 01844 261789

METL
Countax House,
Haseley Trading Estate
Stadhampton Road
Great Haseley
Oxford OX44 7PF
England
Tel: 01844 278781
Fax: 01844 278746

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